Ordering number: EN 4232

SANYO

No.4232

2SJ256

P-Channel MOS Silicon FET

Very High-Speed Switching Applications

Features

- Low ON resistance.
- Very high-speed switching.
- Low-voltage drive.
- Micaless package facilitating mounting.

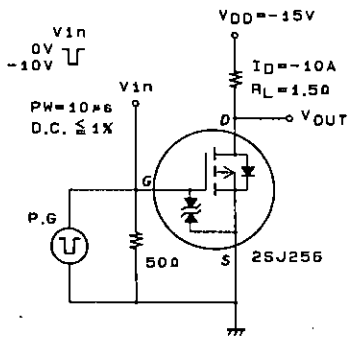
Absolute Maximum Ratings at Ta = 25°C

				unit
Drain to Source Voltage	V_{DSS}		−30	V
Gate to Source Voltage	V_{GSS}		±15	V
Drain Current(DC)	I_D		−18	A
Drain Current(Pulse)	I_{DP}	PW≦10μs, duty cycle≦1%	−72	A
Allowable Power Dissipation	P_D		2.0	W
		T_c = 25°C	30	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		−55 to +150	°C

Electrical Characteristics at Ta = 25°C

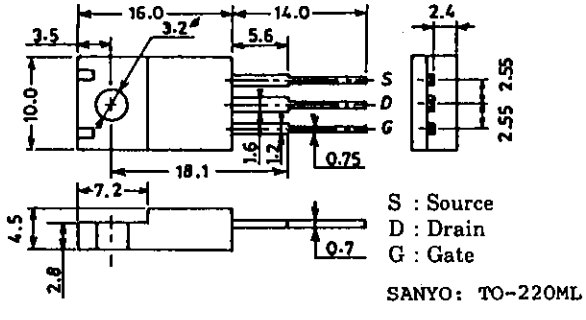
			min	typ	max	unit
D-S Breakdown Voltage	$V_{(BR)DSS}$	I_D = −1mA, V_{GS} = 0	−30			V
G-S Breakdown Voltage	$V_{(BR)GSS}$	I_G = ±100μA, V_{DS} = 0	±15			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −30V, V_{GS} = 0			−100	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±12V, V_{DS} = 0			±10	μA
Cutoff Voltage	$V_{GS(off)}$	V_{DS} = −10V, I_D = −1mA	−1.0		−2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = −10V, I_D = −10A	8.5	14		S
Static Drain to Source on State Resistance	$R_{DS(on)}$	I_D = −10A, V_{GS} = −10V		40	55	mΩ
	$R_{DS(on)}$	I_D = −10A, V_{GS} = −4V		55	75	mΩ
Input Capacitance	C_{iss}	V_{DS} = −10V, f = 1MHz		2000		pF
Output Capacitance	C_{oss}	V_{DS} = −10V, f = 1MHz		1200		pF
Reverse Transfer Capacitance	C_{rss}	V_{DS} = −10V, f = 1MHz		440		pF
Turn-ON Delay Time	$t_{d(on)}$	See specified Test Circuit.		18		ns
Rise Time	t_r	〃		50		ns
Turn-OFF Delay Time	$t_{d(off)}$	〃		400		ns
Fall Time	t_f	〃		400		ns
Diode Forward Voltage	V_{SD}	I_S = −18A, V_{GS} = 0		−1.0	−1.5	V

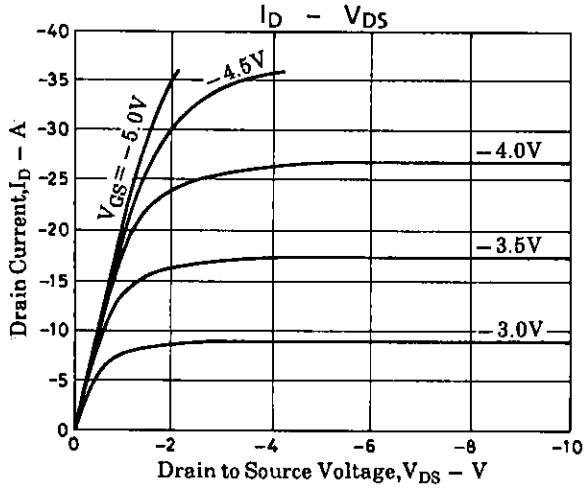
Switching Time Test Circuit

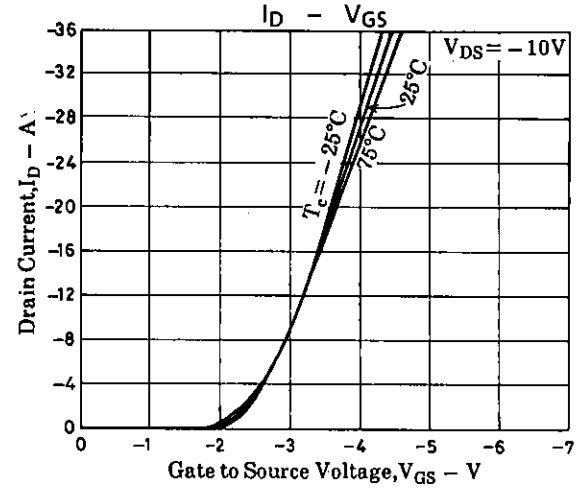


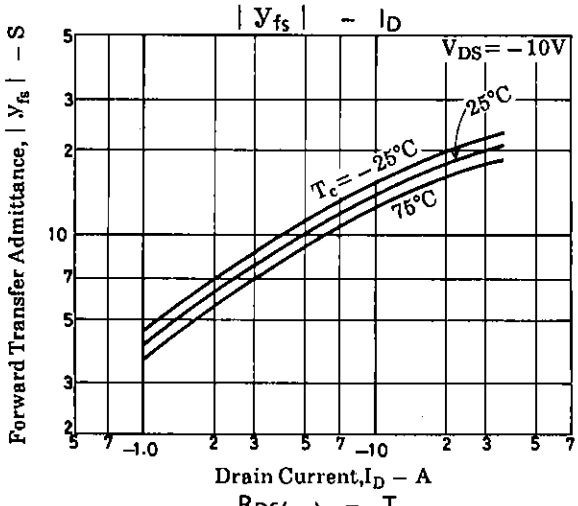
Package Dimensions 2063

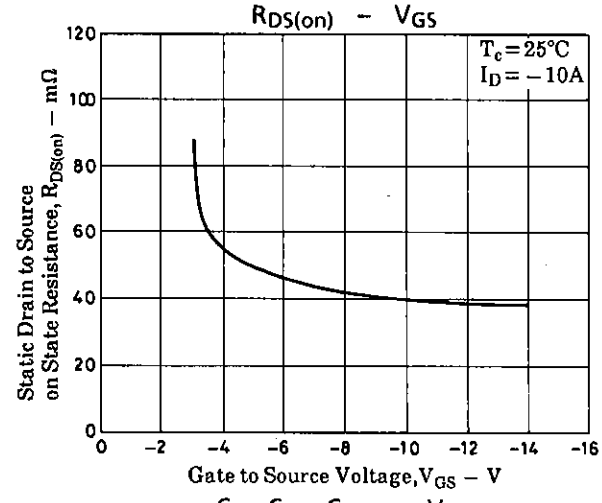
(unit : mm)

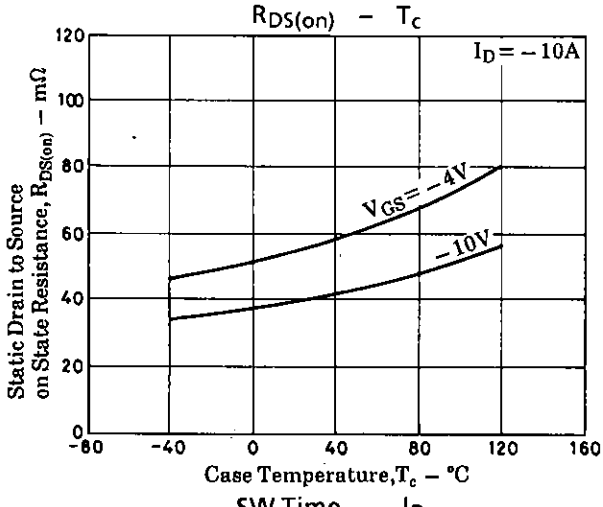


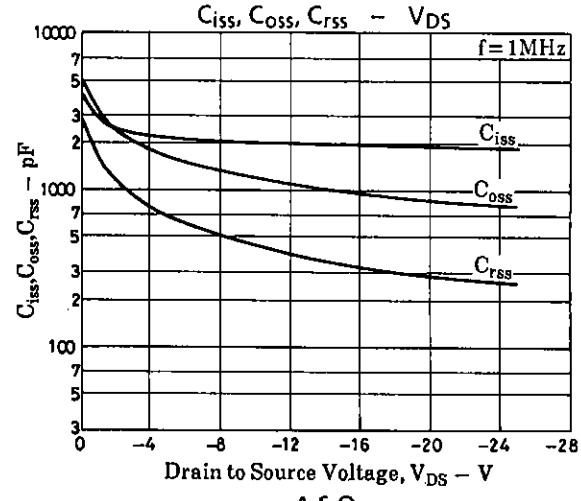

I_D – V_{DS}
Drain Current, I_D – A
Drain to Source Voltage, V_{DS} – V
V_{GS} = –5.0V
–4.5V
–4.0V
–3.5V
–3.0V

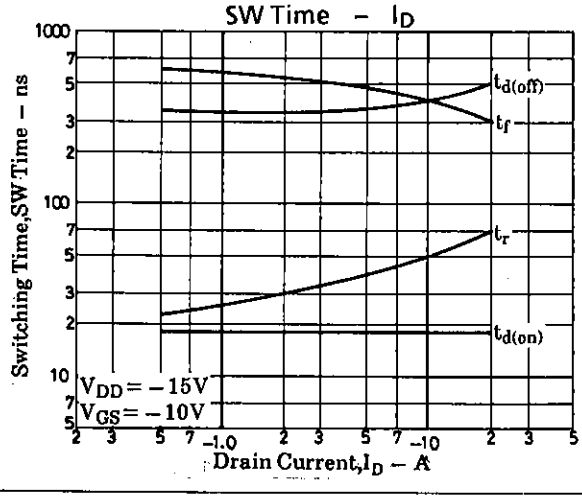

I_D – V_{GS}
V_{DS} = –10V
Drain Current, I_D – A
Gate to Source Voltage, V_{GS} – V
T_c = –25°C
25°C
75°C

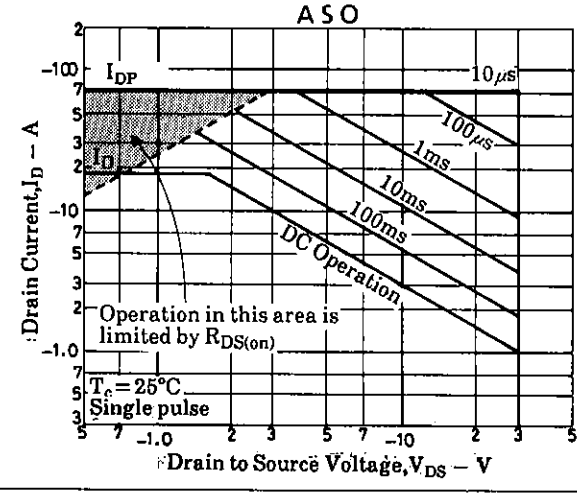

| y_{fs} | – I_D
V_{DS} = –10V
Forward Transfer Admittance, | y_{fs} | – S
Drain Current, I_D – A
T_c = –25°C
25°C
75°C


$R_{DS(on)}$ – V_{GS}
T_c = 25°C
I_D = –10A
Static Drain to Source on State Resistance, $R_{DS(on)}$ – mΩ
Gate to Source Voltage, V_{GS} – V


$R_{DS(on)}$ – T_c
I_D = –10A
V_{GS} = –4V
–10V
Static Drain to Source on State Resistance, $R_{DS(on)}$ – mΩ
Case Temperature, T_c – °C


C_{iss}, C_{oss}, C_{rss} – V_{DS}
f = 1MHz
C_{iss}
C_{oss}
C_{rss}
C_{iss}, C_{oss}, C_{rss} – pF
Drain to Source Voltage, V_{DS} – V


SW Time – I_D
$t_{d(off)}$
t_f
t_r
$t_{d(on)}$
V_{DD} = –15V
V_{GS} = –10V
Switching Time, SW Time – ns
Drain Current, I_D – A


A S O
I_{DP}
I_D
10μs
100μs
1ms
10ms
100ms
DC Operation
Operation in this area is limited by $R_{DS(on)}$
T_c = 25°C
Single pulse
Drain Current, I_D – A
Drain to Source Voltage, V_{DS} – V