NEC

MOS FIELD EFFECT POWER TRANSISTOR
2SJ303

SWITCHING
P-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SJ303 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance.
  $R_{DS(on)} \leqq 0.1\ \Omega$ ($V_{GS} = -10$ V, $I_D = -7$ A)
  $R_{DS(on)} \leqq 0.24\ \Omega$ ($V_{GS} = -4$ V, $I_D = -6$ A)
- Low C_{iss} C_{iss} = 1 200 pF TYP.
- Built-in G-S Gate Protection Diode
- Isolated TO-220 Package

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

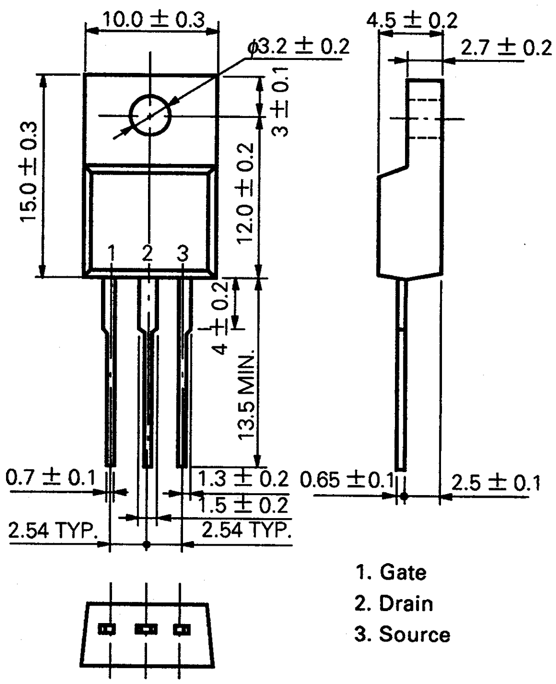
ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Drain to Source Voltage	V_{DSS}	−60	V
Gate to Source Voltage	V_{GSS}	−20, +10	V
Drain Current (DC)	$I_{D(DC)}$	∓14	A
Drain Current (pulse)	$I_{D(pulse)}$*	∓56	A
Total Power Dissipation (T_c = 25 °C)	P_{T1}	35	W
Total Power Dissipation (T_a = 25 °C)	P_{T2}	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

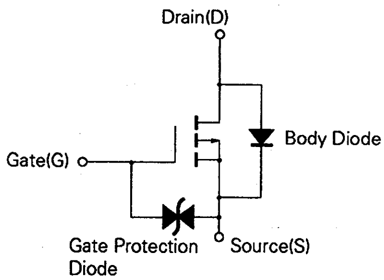
* PW ≦ 10 μs, Duty Cycle ≦ 1 %

PACKAGE DIMENSIONS

in millimeters



1. Gate
2. Drain
3. Source

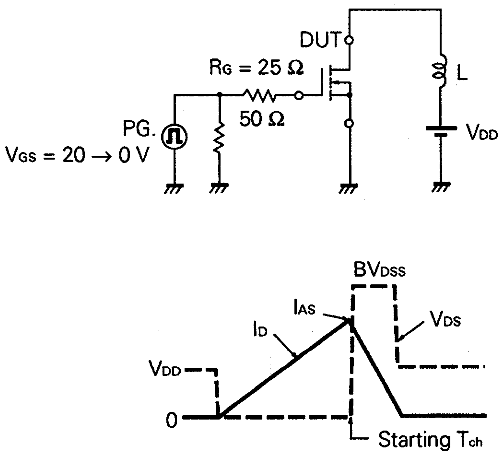


Document No. TC-2456
(O.D. No. TC-7945)
Date Published August 1993 M
Printed in Japan

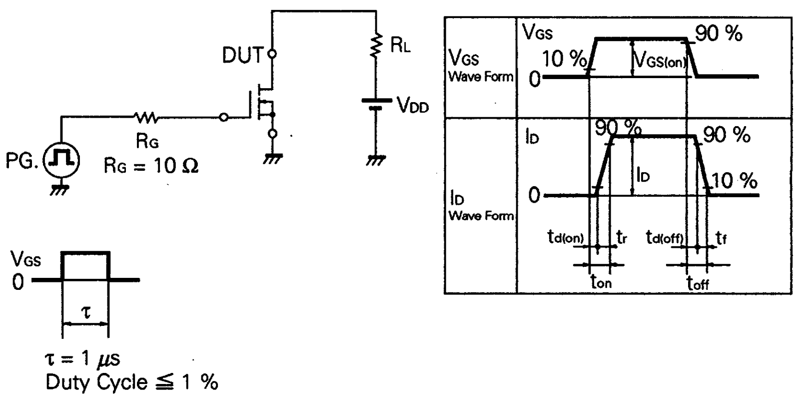
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		75	100	mΩ	V_{GS} = –10 V, I_D = –7 A
Drain to Source On-state Resistance	$R_{DS(on)}$		130	240	mΩ	V_{GS} = –4.0 V, I_D = –6 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	–1.0		–2.0	V	V_{DS} = –10 V, I_D = –1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	5.0			S	V_{DS} = –10 V, I_D = –7 A
Drain Leakage Current	I_{DSS}			–10	μA	V_{DS} = –60 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			∓10	μA	V_{GS} = ∓16 V, V_{DS} = 0
Input Capacitance	C_{iss}		1200		pF	V_{DS} = –10 V V_{GS} = 0 f = 1 MHz
Output Capacitance	C_{oss}		670		pF	
Reverse Transfer Capacitance	C_{rss}		290		pF	
Turn-On Delay Time	$t_{d(on)}$		30		ns	$V_{GS(on)}$ = –10 V V_{DD} = –30 V I_D = –7 A, R_G = 10 Ω R_L = 4.3 Ω
Rise Time	t_r		110		ns	
Turn-Off Delay Time	$t_{d(off)}$		160		ns	
Fall Time	t_f		120		ns	
Total Gate Charge	Q_G		42		nC	V_{GS} = –10 V I_D = –16 A V_{DD} = –48 V
Gate to Source Charge	Q_{GS}		3		nC	
Gate to Drain Charge	Q_{GD}		17		nC	
Diode Forward Voltage	V_{SD}		1.0		V	I_F = –14 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		120		ns	I_F = –14 A, V_{GS} = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q_{rr}		230		nC	

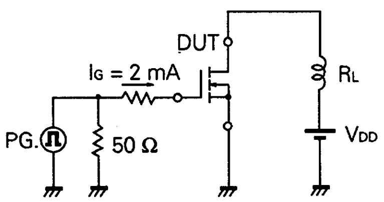
Test Circuit 1 : Avalanche Capability



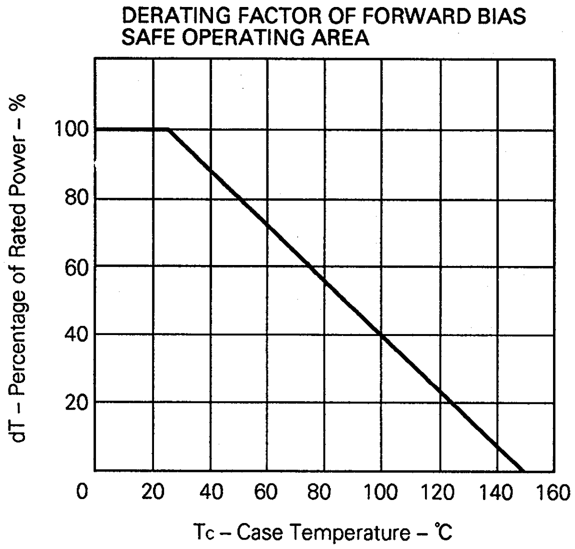
Test Circuit 2 : Switching Time

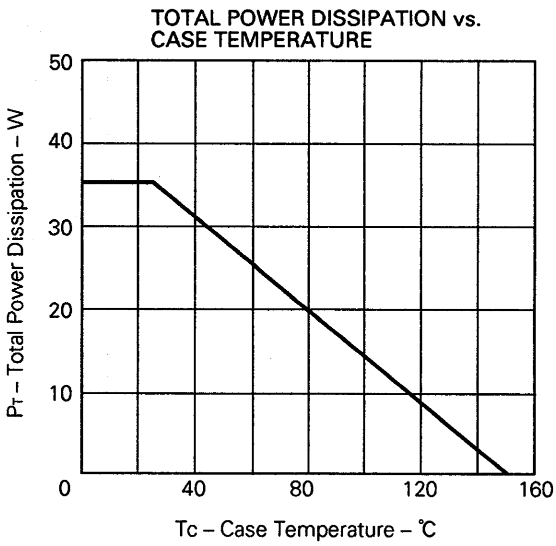


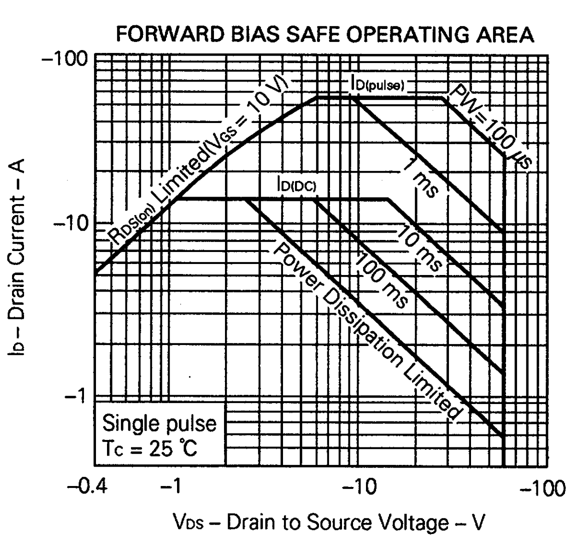
Test Circuit 3 : Gate Charge

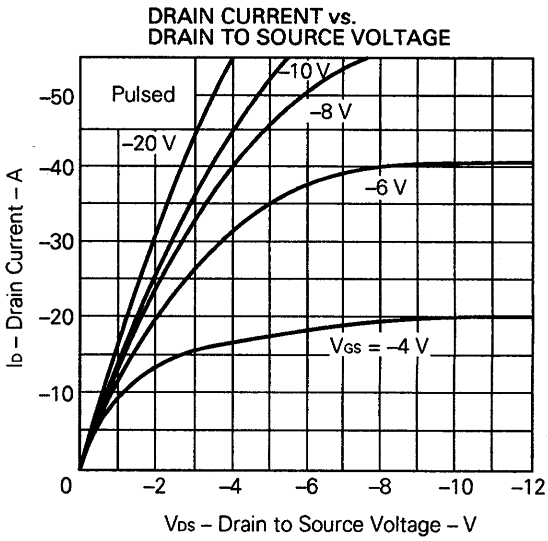


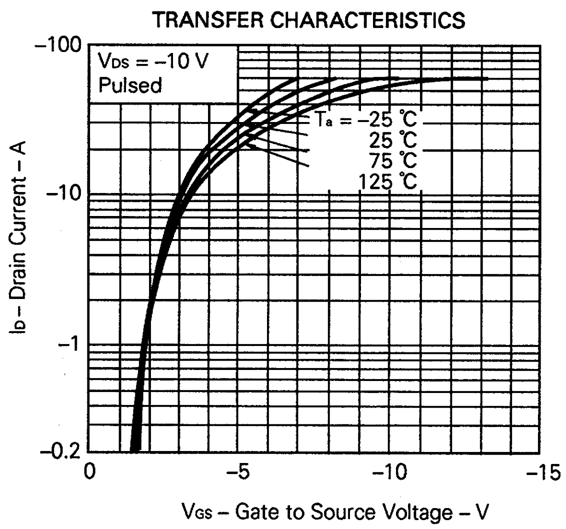
TYPICAL CHARACTERISTICS (T_a = 25 °C)

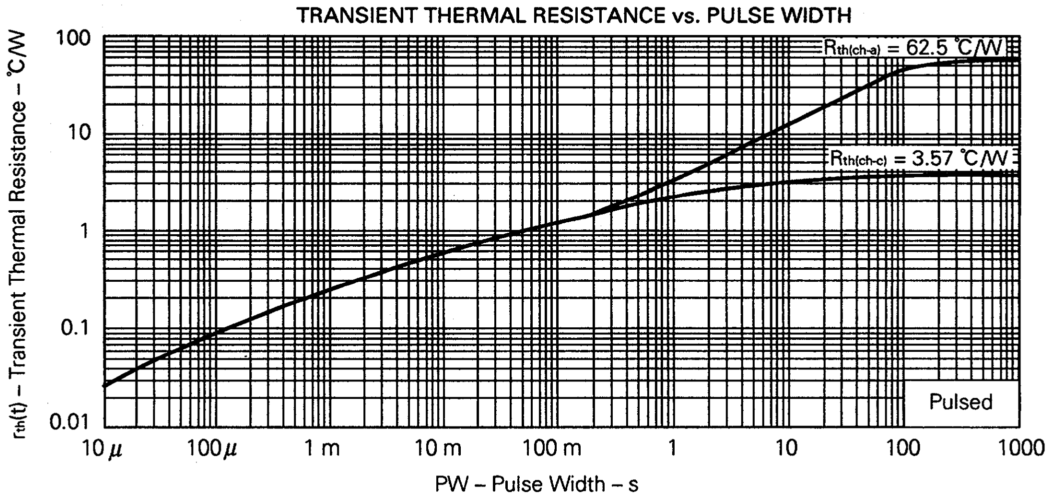


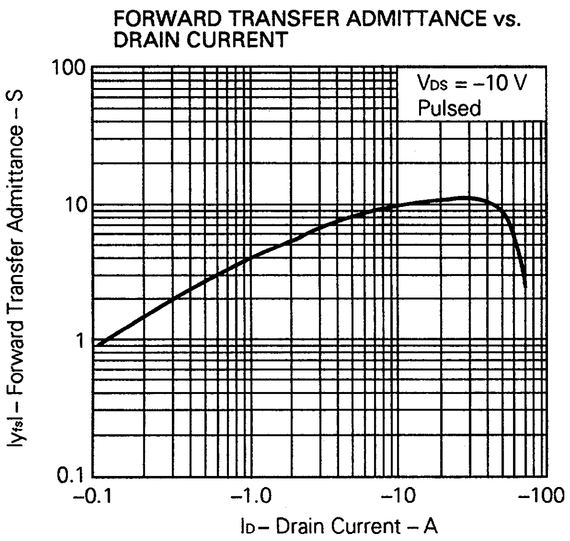


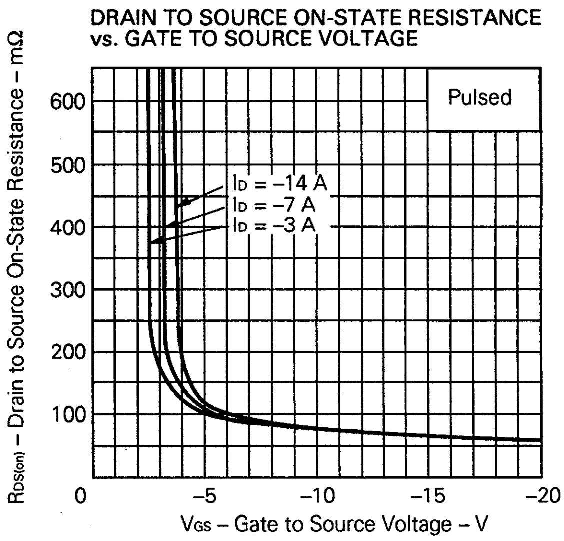


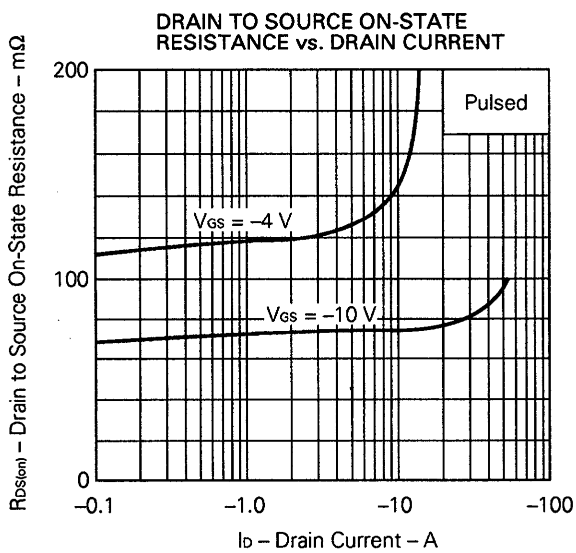


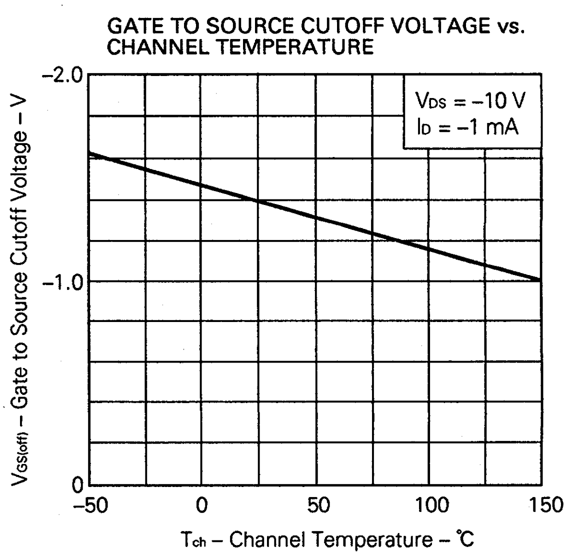



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH
rth(t) – Transient Thermal Resistance – °C/W
100
10
1
0.1
0.01
Rth(ch-a) = 62.5 °C/W
Rth(ch-c) = 3.57 °C/W
Pulsed
10 μ
100 μ
1 m
10 m
100 m
1
10
100
1000
PW – Pulse Width – s

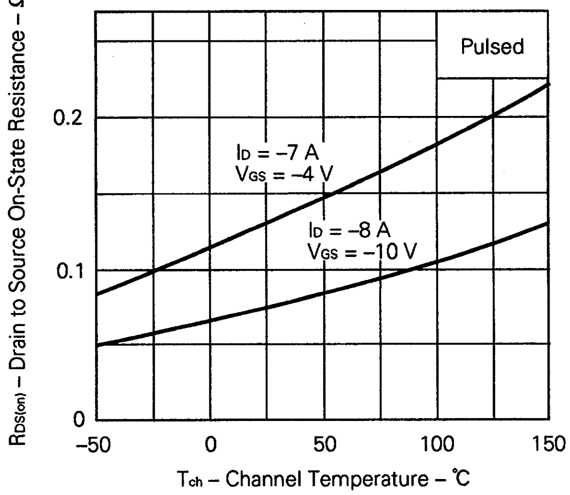

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT
|yfs| – Forward Transfer Admittance – S
100
10
1
0.1
VDS = –10 V
Pulsed
–0.1
–1.0
–10
–100
ID – Drain Current – A


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE
RDS(on) – Drain to Source On-State Resistance – mΩ
600
500
400
300
200
100
0
Pulsed
ID = –14 A
ID = –7 A
ID = –3 A
–5
–10
–15
–20
VGS – Gate to Source Voltage – V

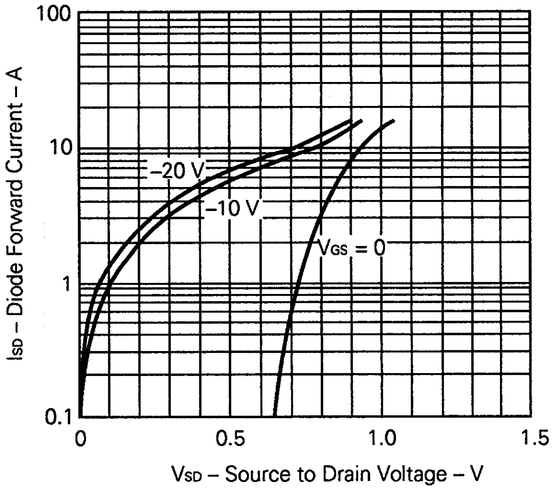

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT
RDS(on) – Drain to Source On-State Resistance – mΩ
200
100
0
Pulsed
VGS = –4 V
VGS = –10 V
–0.1
–1.0
–10
–100
ID – Drain Current – A


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE
VGS(off) – Gate to Source Cutoff Voltage – V
–2.0
–1.0
0
VDS = –10 V
ID = –1 mA
–50
0
50
100
150
Tch – Channel Temperature – °C

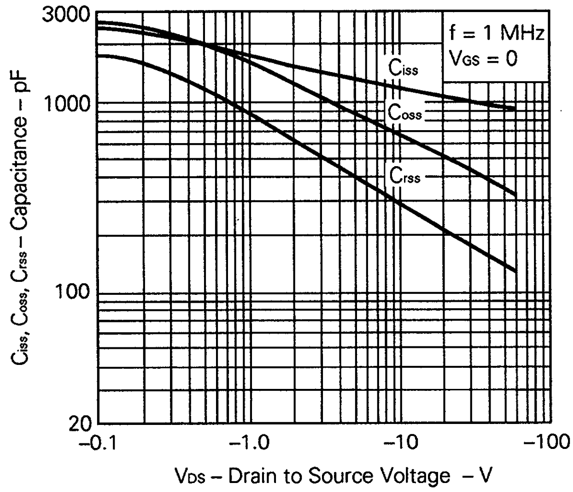
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



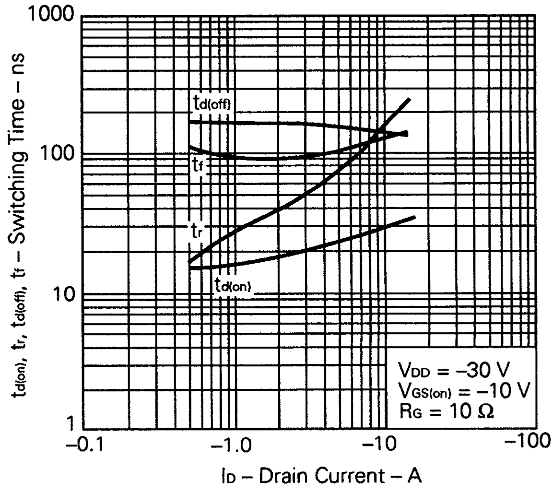
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



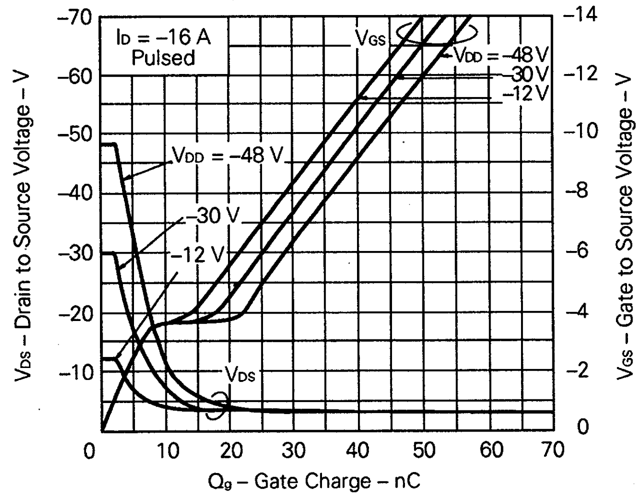
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



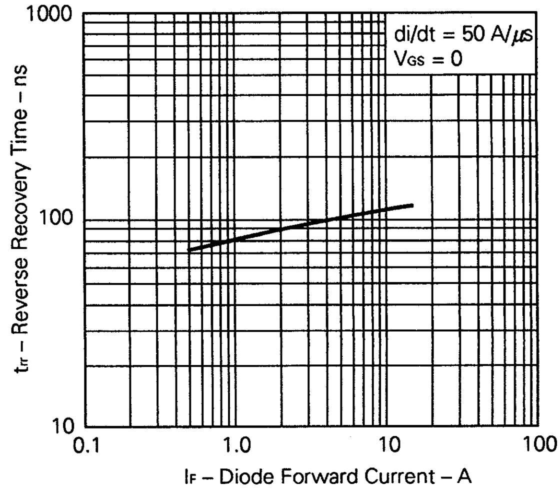
SWITCHING CHARACTERISTICS



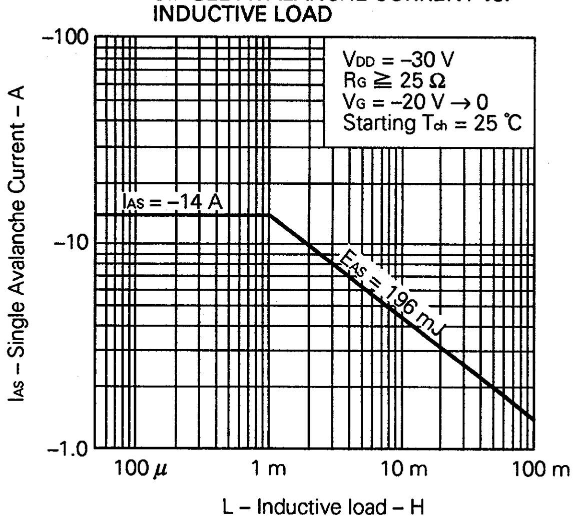
DYNAMIC INPUT CHARACTERISTICS



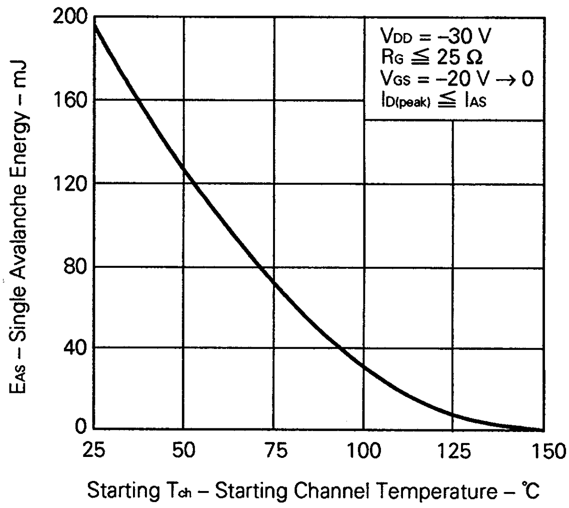
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs. STARTING CHANNEL TEMPERATURE



Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

[MEMO]