

P-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR
2SJ331

SWITCHING
 P-CHANNEL POWER MOS FET
 INDUSTRIAL USE

DESCRIPTION

The 2SJ331 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} \leq 26 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -15 \text{ A)}$
 $R_{DS(on)} \leq 40 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4 \text{ V, } I_D = -12 \text{ A)}$
- Low C_{iss} $C_{iss} = 4 \text{ 300 pF TYP.}$
- Built-in G-S Gate Protection Diodes

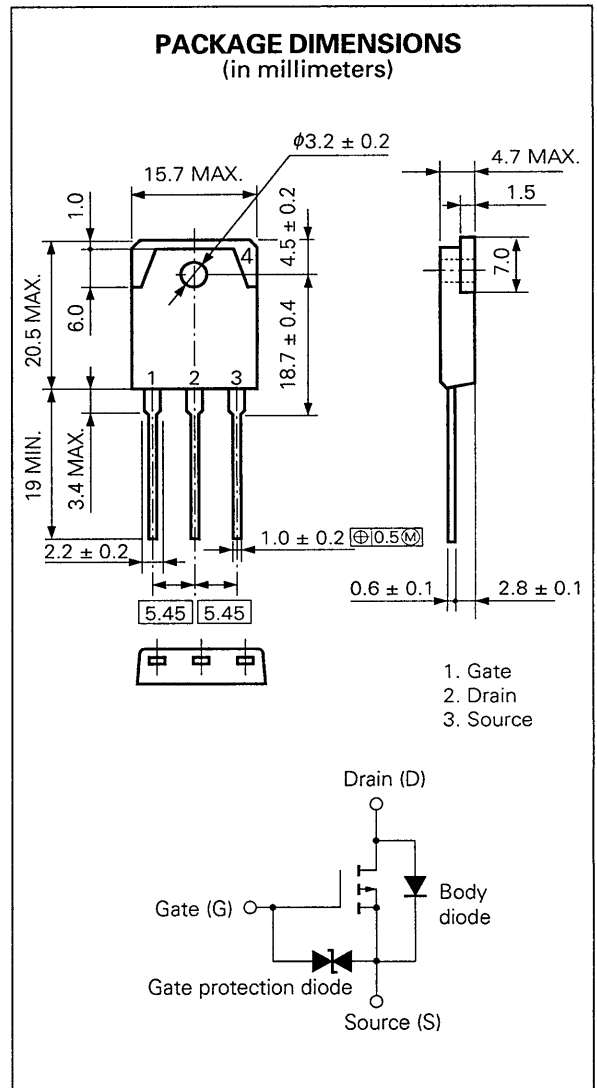
QUALITY GRADE

Standard
 Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25 \text{ }^\circ\text{C}$)

| | | | |
|--|------------------|-------------|------------------|
| Drain to Source Voltage | V_{DSS} | -60 | V |
| Gate to Source Voltage | $V_{GSS(AC)}$ | ∓ 20 | V |
| Gate to Source Voltage | $V_{GSS(DC)}$ | -20, +10 | V |
| Drain Current (DC) | $I_{D(DC)}$ | ∓ 30 | A |
| Drain Current (pulse) | $I_{D(pulse)^*}$ | ∓ 120 | A |
| Total Power Dissipation ($T_c = 25 \text{ }^\circ\text{C}$) P_{T1} | | 150 | W |
| Total Power Dissipation ($T_a = 25 \text{ }^\circ\text{C}$) P_{T2} | | 3.0 | W |
| Channel Temperature | T_{ch} | 150 | $^\circ\text{C}$ |
| Storage Temperature | T_{stg} | -55 to +150 | $^\circ\text{C}$ |

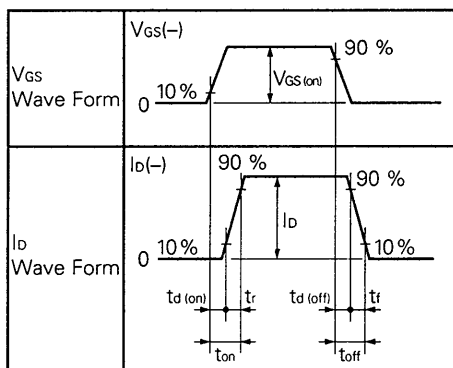
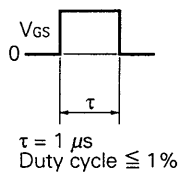
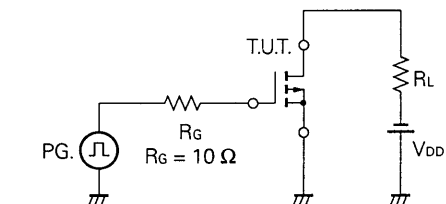
* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1 \%$



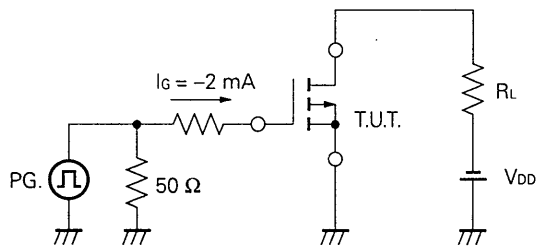
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|-------------------------------------|----------------------|------|-------|------|------|---|
| Drain to Source On-state Resistance | R _{DS(on)} | | 26 | 30 | mΩ | V _{GS} = -10 V, I _D = -15 A |
| Drain to Source On-state Resistance | R _{DS(on)} | | 40 | 55 | mΩ | V _{GS} = -4 V, I _D = -12 A |
| Gate to Source Cutoff Voltage | V _{GS(off)} | -1.0 | -1.5 | -2.0 | V | V _{DS} = -10 V, I _D = -1 mA |
| Forward Transfer Admittance | y _{fs} | 15 | 23 | | S | V _{DS} = -10 V, I _D = -15 A |
| Drain Leakage Current | I _{DSS} | | | -10 | μA | V _{DS} = -60 V, V _{GS} = 0 |
| Gate to Source Leakage Current | I _{GSS} | | | ±10 | μA | V _{GS} = ±16 V, V _{DS} = 0 |
| Input Capacitance | C _{iss} | | 4 300 | | pF | V _{DS} = -10 V V _{GS} = 0 f = 1 MHz |
| Output Capacitance | C _{oss} | | 2 300 | | pF | |
| Reverse Transfer Capacitance | C _{rss} | | 1 100 | | pF | |
| Turn-On Delay Time | t _{d(on)} | | 60 | | ns | V _{GS(on)} = -10 V V _{DD} = -30 V I _D = -15 A, R _G = 10 Ω R _L = 2.0 Ω |
| Rise Time | t _r | | 320 | | ns | |
| Turn-Off Delay Time | t _{d(off)} | | 490 | | ns | |
| Fall Time | t _f | | 470 | | ns | |
| Total Gate Charge | Q _G | | 160 | | nC | V _{GS} = -10 V I _D = -30 A V _{DD} = -48 V |
| Gate to Source Charge | Q _{GS} | | 12 | | nC | |
| Gate to Drain Charge | Q _{GD} | | 66 | | nC | |
| Diode Forward Voltage | V _{SD} | | 1.1 | | V | I _F = 30 A, V _{GS} = 0 |
| Reverse Recovery Time | t _{rr} | | 150 | | ns | I _F = 30 A, V _{GS} = 0 |
| Reverse Recovery Charge | Q _{rr} | | 300 | | nC | di/dt = 50 A/μs |

Test Circuit 1: Switching Time

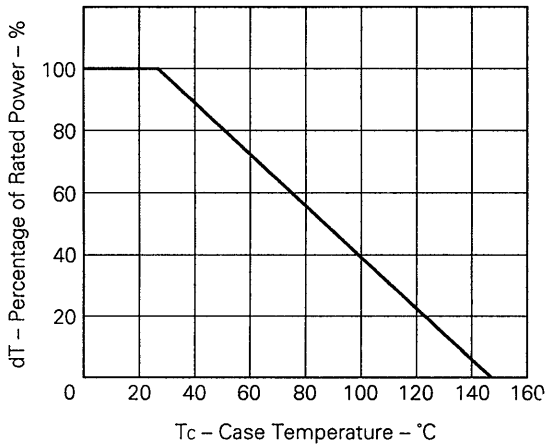


Test Circuit 2: Gate Charge

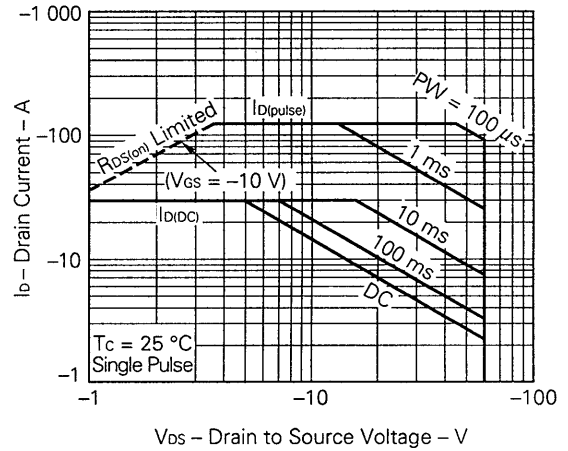


ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

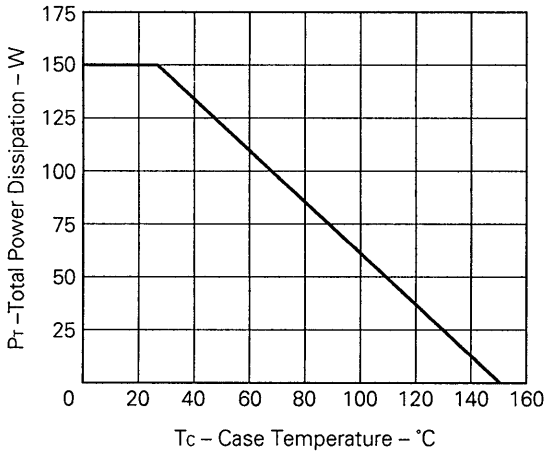
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



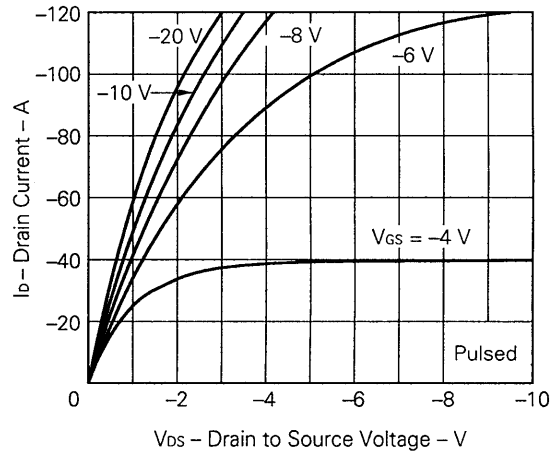
FORWARD BIAS SAFE OPERATING AREA



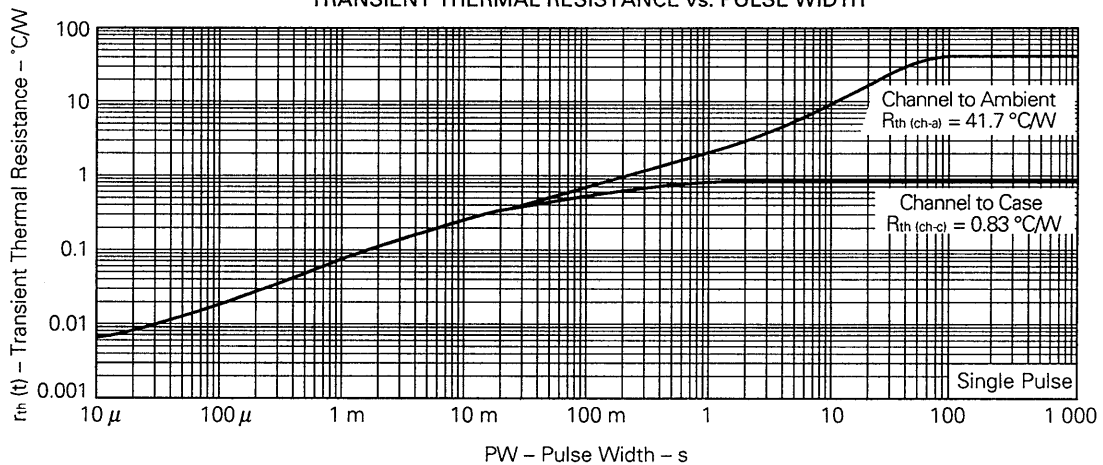
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

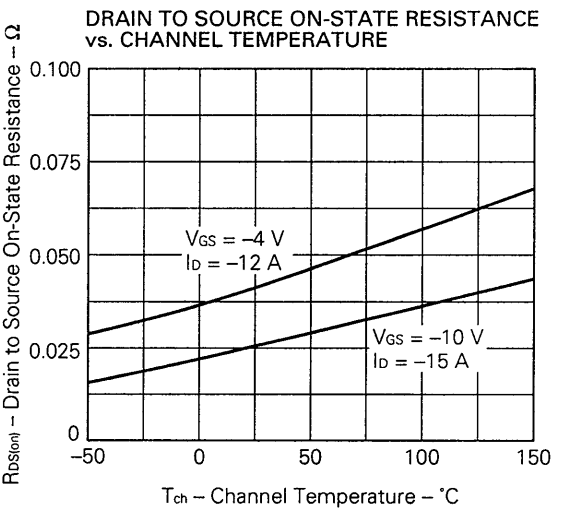
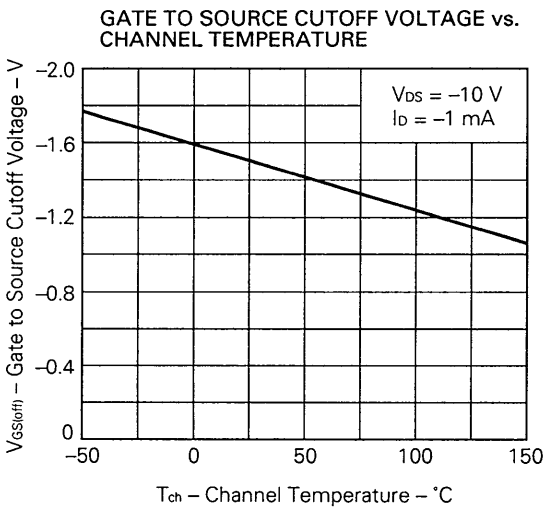
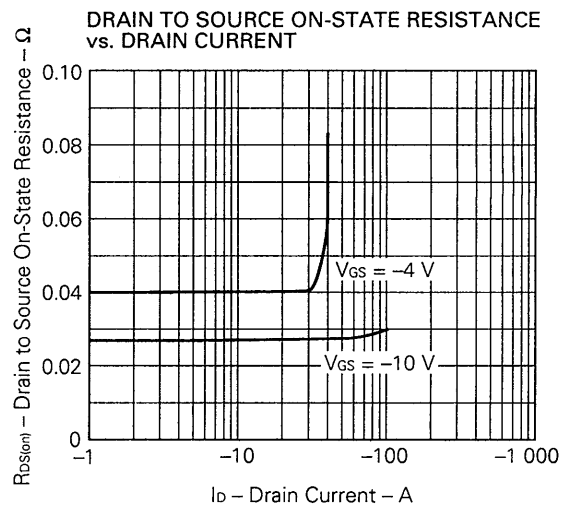
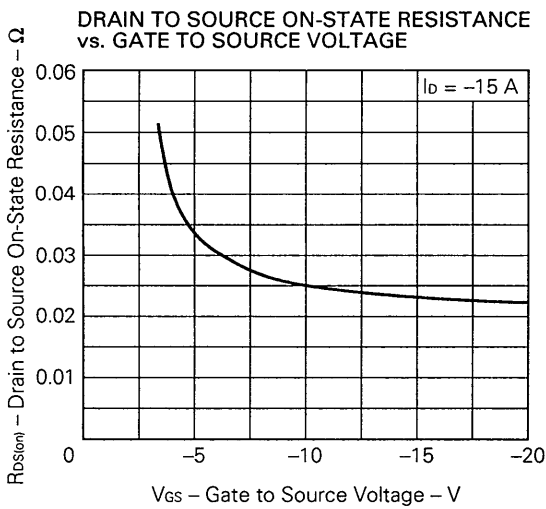
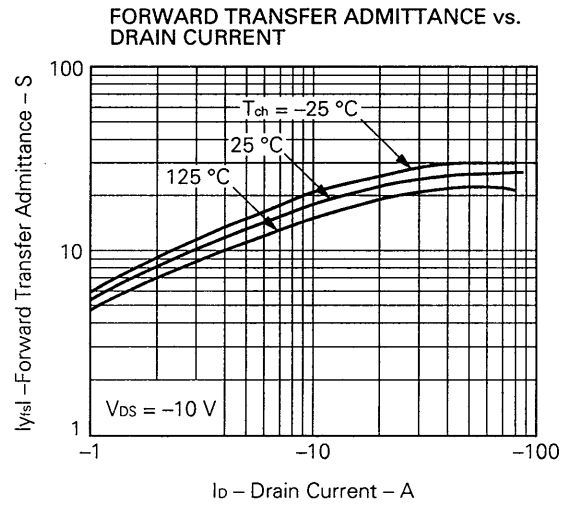
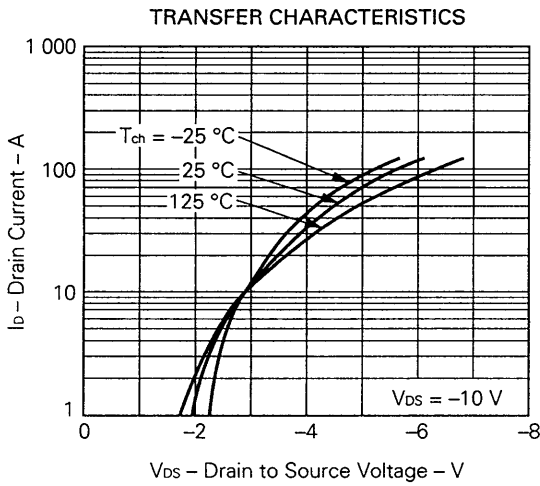


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

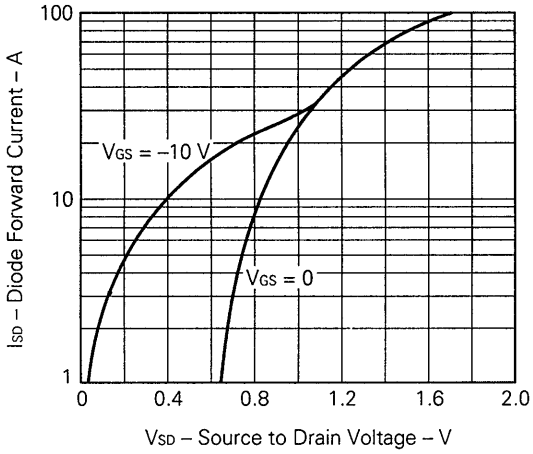


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

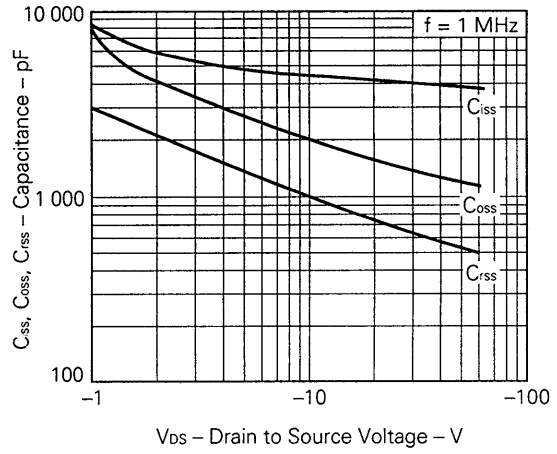




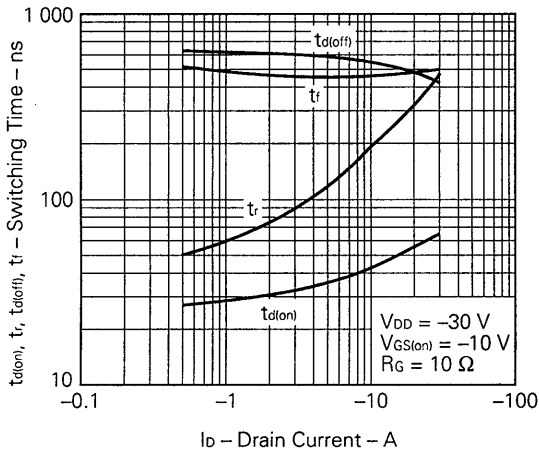
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



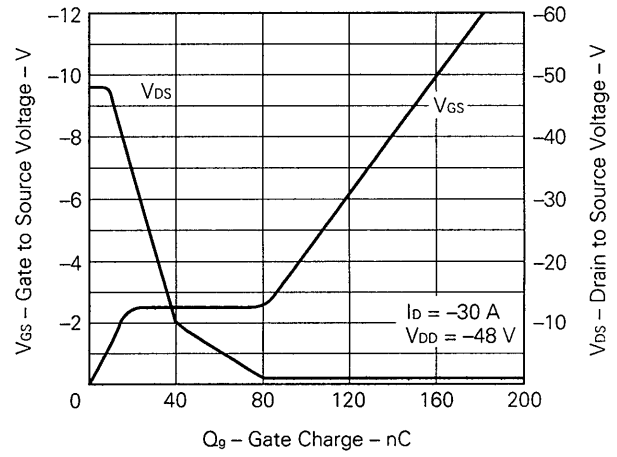
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



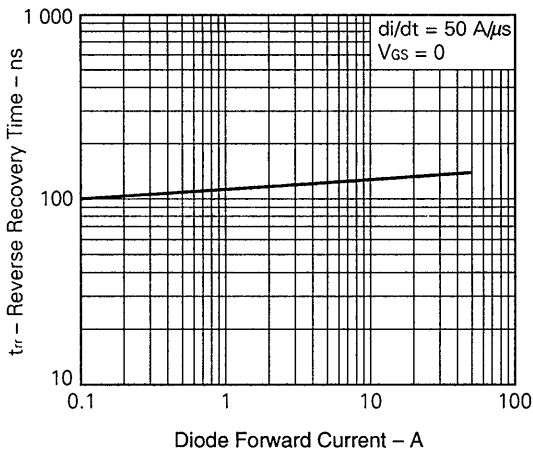
SWITCHING CHARACTERISTICS



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REVERSE RECOVERY TIME vs. REVERSE DRAIN CURRENT



Reference

| Application note name | No. |
|--|----------|
| Safe operating area of Power MOS FET. | TEA-1034 |
| Application circuit using Power MOS FET. | TEA-1035 |
| Quality control of NEC semiconductors devices. | TEI-1202 |
| Quality control guide of semiconductors devices. | MEI-1202 |
| Assembly manual of semiconductors devices. | IEI-1207 |

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