

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7WH123FU, TC7WH123FK

MONOSTABLE MULTIVIBRATOR

The TC74WH123 is high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C²MOS technology.

There are two trigger inputs, $\overline{A}$ input (Negative edge), and B input (Positive edge). These inputs are valid for a slow rise/fall time signal ($t_r = t_f = 1\text{sec.}$) as they are schmitt trigger inputs. This device may also be triggered by using CLR input (Positive edge).

After triggering, the output stays in a MONOSTABLE state for a time period determined by the external resistor and capacitor (R_x, C_x). A low level at the $\overline{\text{CLR}}$ input breaks this state.

Limits for C_x and R_x are :

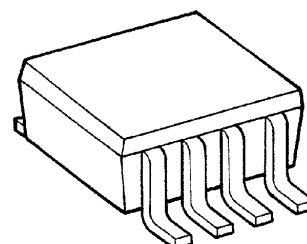
External capacitor, C_x No limit

External resistor, R_x $V_{CC} = 2.0\text{V}$ more than $5\text{k}\Omega$
 $V_{CC} \geq 3.0\text{V}$ more than $1\text{k}\Omega$

An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up.

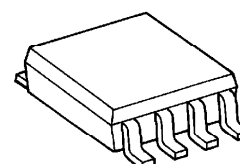
This circuit prevents device destruction due to mismatched supply and input voltages.

TC7WH123FU



SSOP8-P-0.65

TC7WH123FK



SSOP8-P-0.50A

Weight

SSOP8-P-0.65 : 0.02g (Typ.)

SSOP8-P-0.50A : 0.01g (Typ.)

FEATURES

- High Speed $t_{pd} = 8.1\text{ns}$ (Typ.) at $V_{CC} = 5\text{V}$
- Low Power Dissipation
 - Standby State $I_{CC} = 2\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
 - Active State $I_{CC} = 600\mu\text{A}$ (Max.) at $V_{CC} = 5\text{V}$
- High Noise Immunity $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays $t_{pLH} = t_{pHL}$
- Wide Operation Voltage Range ... $V_{CC}(\text{opr}) = 2 \sim 5.5\text{V}$

980508EBA2

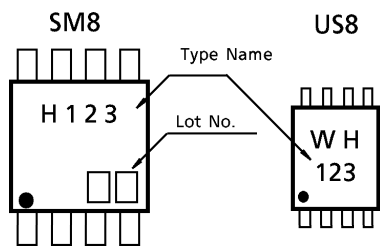
● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

● The products described in this document are subject to foreign exchange and foreign trade laws.

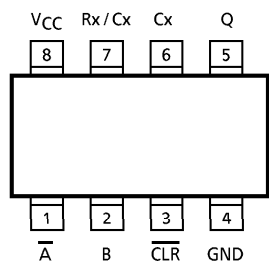
● The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.

● The information contained herein is subject to change without notice.

MARKING



PIN ASSIGNMENT (TOP VIEW)

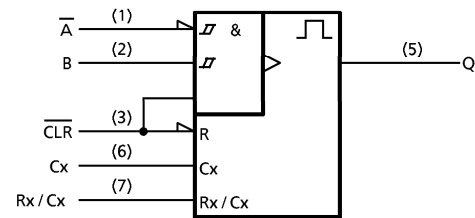


TRUTH TABLE

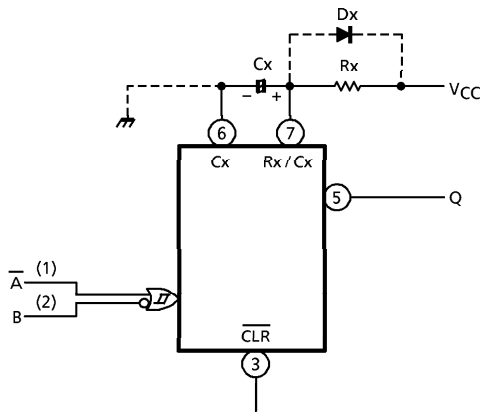
INPUTS			OUTPUTS	NOTE
$\overline{A}$	B	$\overline{CLR}$	Q	
	H	H		OUTPUT ENABLE
x	L	H	L	INHIBIT
H	x	H	L	INHIBIT
L		H		OUTPUT ENABLE
L	H			OUTPUT ENABLE
x	x	L	L	RESET

x : Don't Care

LOGIC DIAGRAM



BLOCK DIAGRAM



(Note 1) Cx, Rx, Dx are external

Capacitor, Resistor, and Diode, respectively.

(Note 2) External clamping diode, Dx ;

The external capacitor is charged to V_{CC} level in the wait state, i.e. when no trigger is applied.

If the supply voltage is turned off, Cx is discharges mainly through the internal (parasitic) diode. If Cx is sufficiently large and V_{CC} drops rapidly, there will be some possibility of damaging the IC through in rush current or latch-up. If the capacitance of the supply voltage filter is large enough and V_{CC} drops slowly, the in rush current is automatically limited and damage to the IC is avoided.

The maximum value of forward current through the parasitic diode is $\pm 20\text{mA}$.

In the case of a large Cx, the limit of fall time of the supply voltage is determined as follows:

$$t_r \geq (V_{CC} - 0.7) \cdot C_x / 20\text{mA}$$

(t_r is the time between the supply voltage turn off
and the supply voltage reaching 0.4 V_{CC} .)

In the even a system does not satisfy the above condition, an external clamping diode (Dx) is needed to protect the IC from rush current.

FUNCTIONAL DESCRIPTION

(1) Stand-by State

The external capacitor (C_x) is fully charged to V_{CC} in the stand-by state. That means, before triggering, the Q_p and Q_N transistors which are connected to the R_x/C_x node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies turn off. The total supply current is only leakage current.

(2) Trigger operation

Trigger operation is effective in any of the following three cases. First, the condition where the $\overline{A}$ input is low, and the B input has a rising signal; second, where the B input is high, and the $\overline{A}$ input has a falling signal; and third, where the $\overline{A}$ input is low and the B input is high, and the $\overline{CLR}$ input has a rising signal.

After a trigger becomes effective, comparators C1 and C2 start operating, and Q_N is turned on. The external capacitor discharges through Q_N . The voltage level at the R_x/C_x node drops. If the R_x/C_x voltage level falls to the internal reference voltage V_{refL} , the output of C1 becomes low. The flip-flop is then reset and Q_N turns off. At that moment C1 stops but C2 continues operating.

After Q_N turns off, the voltage at the R_x/C_x node starts rising at a rate determined by the time constant of external capacitor C_x and resistor R_x .

Upon triggering, output Q becomes high, following some delay time of the internal F/F and gates. It stays high even if the voltage of R_x/C_x changes from falling to rising. When R_x/C_x reaches the internal reference voltage V_{refH} , the output of C2 becomes low, the output Q goes low and C2 stops its operation. That means, after triggering, when the voltage level of the R_x/C_x node reaches V_{refH} , the IC returns to its MONOSTABLE state.

With large values of C_x and R_x , and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse, t_w (OUT), is as follows :

$$t_w(\text{OUT}) = 1.0 C_x R_x$$

(3) Retrigger operation

When a new trigger is applied to either input $\overline{A}$ or B while in the MONOSTABLE state, it is effective only if the IC is charging C_x . The voltage level of the R_x/C_x node then falls to V_{refL} level again. Therefore the Q output stays high if the next trigger comes in before the time period set by C_x and R_x .

If the new trigger is very close to previous trigger, such as an occurrence during the discharge cycle, it will have no effect.

The minimum time for a trigger to be effective 2nd trigger, $t_{rr}(\text{Min.})$, depends on V_{CC} and C_x .

(4) Reset operation

In normal operation, the $\overline{CLR}$ input is held high. If $\overline{CLR}$ is low, a trigger has no effect because the Q output is held low and the trigger control F/F is reset. Also, Q_p turns on and C_x is charged rapidly to V_{CC} .

This means if $\overline{CLR}$ is set low, the IC goes into a wait state.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V _{CC}	-0.5~7	V
DC Input Voltage	V _{IN}	-0.5~7	V
DC Output Voltage	V _{OUT}	-0.5~V _{CC} +0.5	V
Input Diode Current	I _{IK}	-20	mA
Output Diode Current	I _{OK}	±20	mA
DC Output Current	I _{OUT}	±25	mA
DC V _{CC} /Ground Current	I _{CC}	±50	mA
Power Dissipation	P _D	300 (SM8)	mW
		200 (US8)	
Storage Temperature	T _{stg}	-65~150	°C
Lead Temperature (10 s)	T _L	260	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC}	2~5.5	V
Input Voltage	V _{IN}	0~5.5	V
Output Voltage	V _{OUT}	0~V _{CC}	V
Operating Temperature	T _{opr}	-40~85	°C
Input Rise and Fall Time	dt/dv	0~100 (V _{CC} = 3.3 ± 0.3V)	ns/V
		0~20 (V _{CC} = 5 ± 0.5V)	
External Capacitor	C _x	No Limitation*	F
External Resistor	R _x	≥5k (V _{CC} = 2.0V)*	Ω
		≥1k (V _{CC} ≥ 3.0V)*	

- * The maximum allowable values of C_x and R_x are a function of leakage of capacitor C_x, the leakage of TC74VHC123A/221A, and leakage due to board layout and surface resistance.
Susceptibility to externally induced noise signals may occur for R_x > 1MΩ.

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		SYM- BOL	TEST CONDITION		V _{CC} (V)	Ta = 25°C			Ta = - 40~85°C		UNIT	
						MIN.	TYP.	MAX.	MIN.	MAX.		
Input Voltage	“H” Level	V _{IH}			2.0	1.5	—	—	1.5	—	V	
					3.0~ 5.5	V _{CC} × 0.7	—	—	V _{CC} × 0.7	—		
	“L” Level	V _{IL}			2.0	—	—	0.5	—	0.5		
					3.0~ 5.5	—	—	V _{CC} × 0.3	—	V _{CC} × 0.3		
Output Voltage	“H” Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = - 50μA	2.0	1.9	2.0	—	1.9	—	V	
					3.0	2.9	3.0	—	2.9	—		
					4.5	4.4	4.5	—	4.4	—		
					I _{OH} = - 4mA	3.0	2.58	—	—	2.48		—
					I _{OH} = - 8mA	4.5	3.94	—	—	3.80		—
	“L” Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	2.0	—	0	0.1	—	0.1		
					3.0	—	0	0.1	—	0.1		
					4.5	—	0	0.1	—	0.1		
					I _{OL} = 4mA	3.0	—	—	0.36	—		0.44
					I _{OL} = 8mA	4.5	—	—	0.36	—		0.44
Control Input Current		I _{IN}	V _{IN} = 5.5V or GND	0~ 5.5	—	—	± 0.1	—	± 1.0	μA		
Rx / Cx Terminal Off-State Current		I _{IN}	V _{IN} = V _{CC} or GND	5.5	—	—	± 0.25	—	± 0.25	μA		
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	2.0	—	20.0	μA		
		I _{CC}	V _{IN} = V _{CC} or GND Rx / Cx = 0.5V _{CC}	3.0	—	160	250	—	280			
				4.5	—	380	500	—	650			
				5.5	—	560	750	—	975			

TIMING REQUIREMENTS (Input t_r = t_f = 3ns)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C		Ta = - 40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width	t _w (L)		3.3 ± 0.3	—	5.0	5.0	ns
	t _w (H)		5.0 ± 0.5	—	5.0	5.0	
Minimum Clear Width (CLR)	t _w (L)		3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum Retrigger Time	t _{rr}	Rx = 1kΩ	3.3 ± 0.3	60	—	—	ns
		Cx = 100pF	5.0 ± 0.5	39	—	—	
		Rx = 1kΩ	3.3 ± 0.3	1.5	—	—	
		Cx = 0.01μF	5.0 ± 0.5	1.2	—	—	μs

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYM-BOL	TEST CONDITION			Ta = 25°C			Ta = − 40~85°C		UNIT
			V _{CC} (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A , B-Q)	t _{pLH} t _{pHL}		3.3 ± 0.3	15	—	13.4	20.6	1.0	24.0	ns
				50	—	15.9	24.1	1.0	27.5	
			5.0 ± 0.5	15	—	8.1	12.0	1.0	14.0	
				50	—	9.6	14.0	1.0	16.0	
Propagation Delay Time (CLR trigger-Q)	t _{pLH} t _{pHL}		3.3 ± 0.3	15	—	14.5	22.4	1.0	26.0	
				50	—	17.0	25.9	1.0	29.5	
			5.0 ± 0.5	15	—	8.7	12.9	1.0	15.0	
				50	—	10.2	14.9	1.0	17.0	
Propagation Delay Time (CLR-Q)	t _{pLH} t _{pHL}		3.3 ± 0.3	15	—	10.3	15.8	1.0	18.5	
				50	—	12.8	19.3	1.0	22.0	
			5.0 ± 0.5	15	—	6.3	9.4	1.0	11.0	
				50	—	7.8	11.4	1.0	13.0	
Output Pulse Width	t _{wOUT}	Cx = 28pF Rx = 2kΩ	3.3 ± 0.3	50	—	160	240	—	300	μs
			5.0 ± 0.5		—	133	200	—	240	
		Cx = 0.01μF Rx = 10kΩ	3.3 ± 0.3	50	90	100	110	90	110	
			5.0 ± 0.5		90	100	110	90	110	
		Cx = 0.1μF Rx = 10kΩ	3.3 ± 0.3	50	0.9	1.0	1.1	0.9	1.1	ms
			5.0 ± 0.5		0.9	1.0	1.1	0.9	1.1	
Input Capacitance	C _{IN}					4	10	—	10	pF
Power Dissipation Capacitance	C _{PD}	(Note 1)			—	73	—	—	—	

(Note 1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

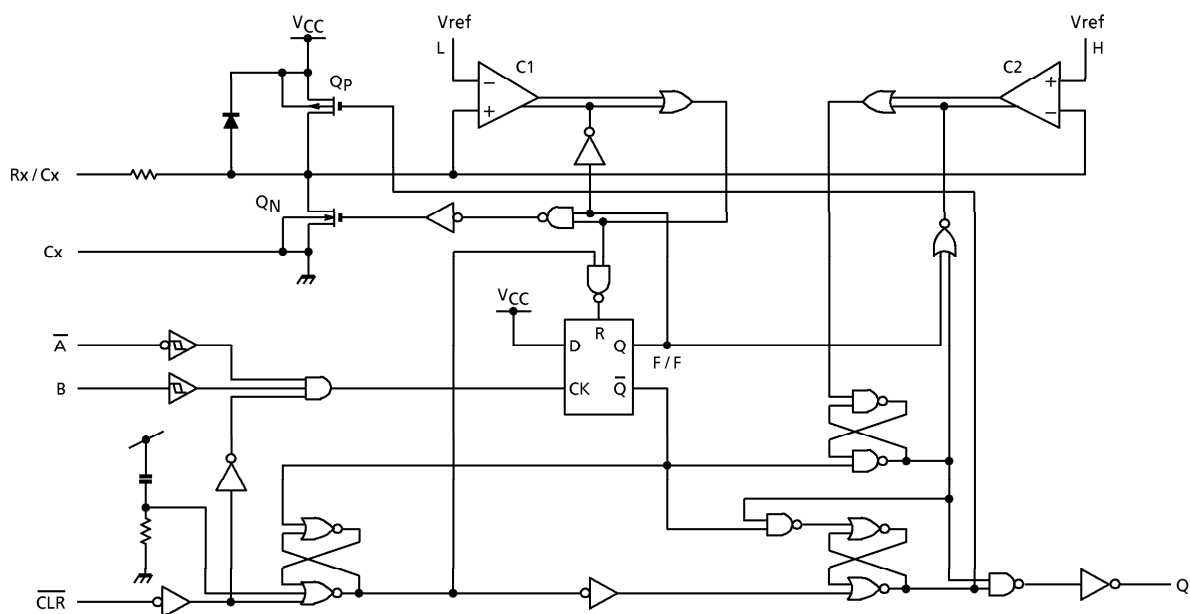
Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot \text{Duty} / 100 + I_{CC} / 2 \text{ (per circuit)}$$

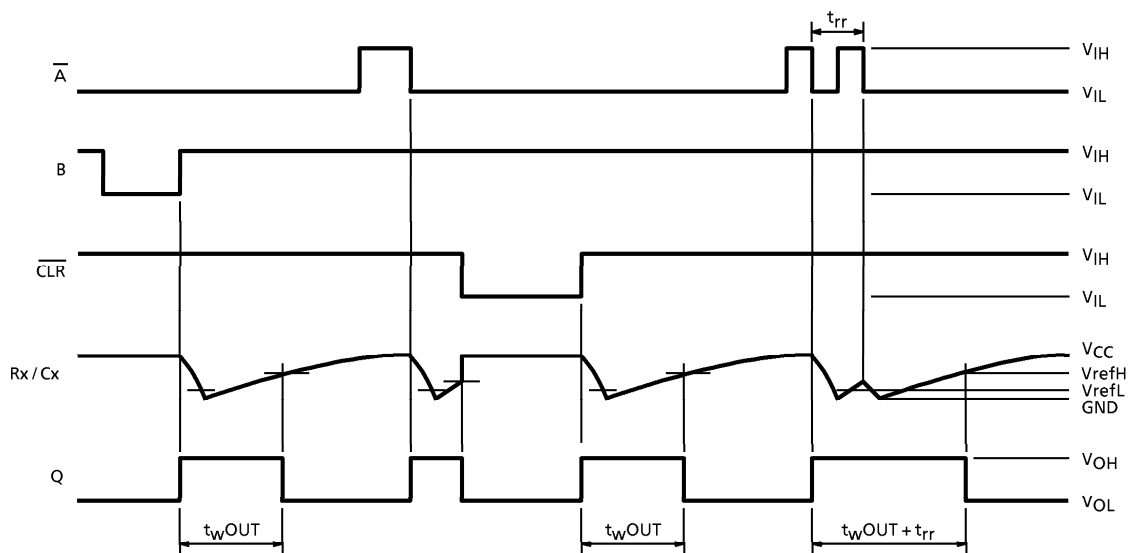
(I_{CC}' : Active Supply Current)

(Duty : %)

IEC LOGIC SYMBOL

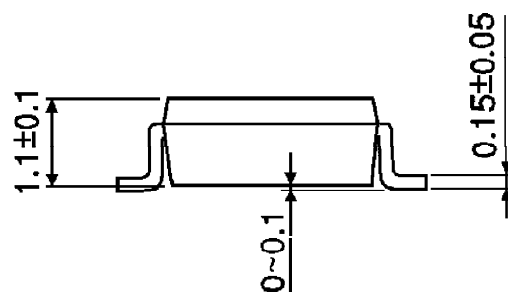
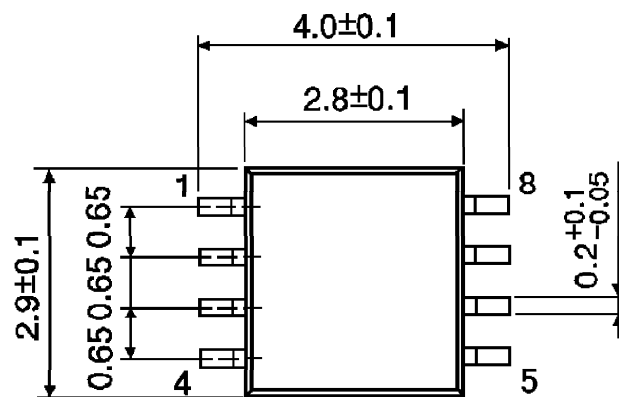


Timing Chart



OUTLINE DRAWING
SSOP8-P-0.65

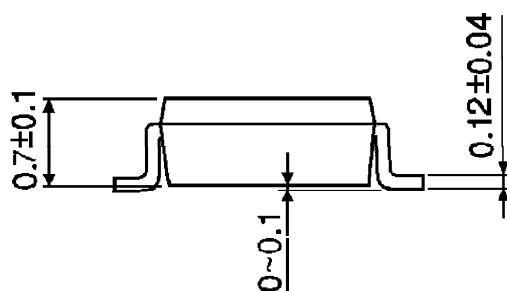
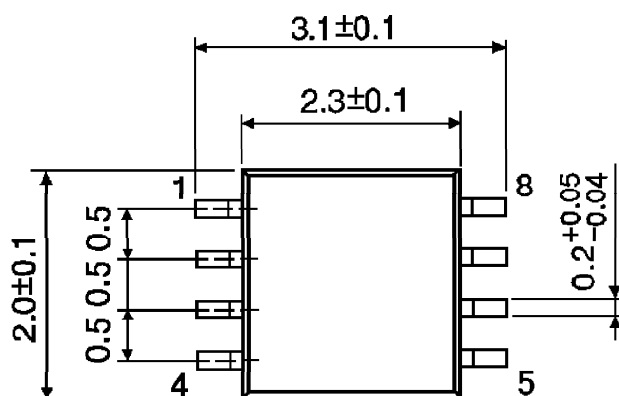
Unit : mm



Weight : 0.02g (Typ.)

OUTLINE DRAWING
SSOP8-P-0.50A

Unit : mm



Weight : 0.01g (Typ.)