PIC16C72A → PIC16F72 Migration

DEVICE MIGRATIONS

This document is intended to describe the differences that are present when migrating from one device to the next. Table 1 and Table 2 list the data memory organization differences and the additional Special Function Registers, Table 3 lists the differences in functionality, and Table 4 through Table 7 list the differences in the electrical and timing specifications.

Note:	This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

Note:	The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the oscillator mode may be required.

TABLE 1: PIC16C72A → PIC16F72 DATA MEMORY DIFFERENCES

No.	SFR	Differences from PIC16C72A	Comment
1	BANK 2	BANK 2 is implemented	
2	BANK 3	BANK 3 is implemented	
3	PMADRH:PMADRL	Implemented	Address register pair
4	PMDATH:PMDATL	Implemented	Data register pair
5	PMCON1	Implemented	Control register for memory access
6	STATUS	Bit 6 (RP1) and Bit 7 (IRP) are implemented	RP1 to access BANK 2 & 3, IRP used for indirect addressing
7	INTCON	Bit 2 (TMR0IF) and Bit 5 (TMR0IE)	T0IF and T0IE in PIC16C72A

TABLE 2: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS(3)
Bank 2											
100h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
101h	TMR0	Timer0 Module's Register								xxxx xxxx	uuuu uuuu
102h(1	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
103h(1)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
104h(1)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	uuuu uuuu
105h	—	Unimplemented								—	—
106h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
107h	—	Unimplemented								—	—
108h	—	Unimplemented								—	—
109h	—	Unimplemented								—	—
10Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
10Bh(1)	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u
10Ch	PMDATL	Data Register Low Byte								xxxx xxxx	uuuu uuuu
10Dh	PMADRL	Address Register Low Byte								xxxx xxxx	uuuu uuuu
10Eh	PMDATH	—	—	Data Register High Byte						xxxx xxxx	uuuu uuuu
10Fh	PMADRH	—	—	—	Address Register High Byte					xxxx xxxx	uuuu uuuu
Bank 3											
180h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
181h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
182h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
183h(1)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
184h(1)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	uuuu uuuu
185h	—	Unimplemented								—	—
186h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
187h	—	Unimplemented								—	—
188h	—	Unimplemented								—	—
189h	—	Unimplemented								—	—
18Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
18Bh(1)	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u
18Ch	PMCON1	— (4)	—	—	—	—	—	—	RD	1--- ---0	1--- ---0
18Dh	—	Unimplemented								—	—
18Eh	—	Reserved maintain clear								0000 0000	0000 0000
18Fh	—	Reserved maintain clear								0000 0000	0000 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

3: Other (non power-up) RESETs include external RESET through $\overline{MCLR}$ and Watchdog Timer Reset.

4: This bit always reads as a '1'.

FIGURE 1: PIC16F72 BANK 2 & 3 REGISTER FILE MAP

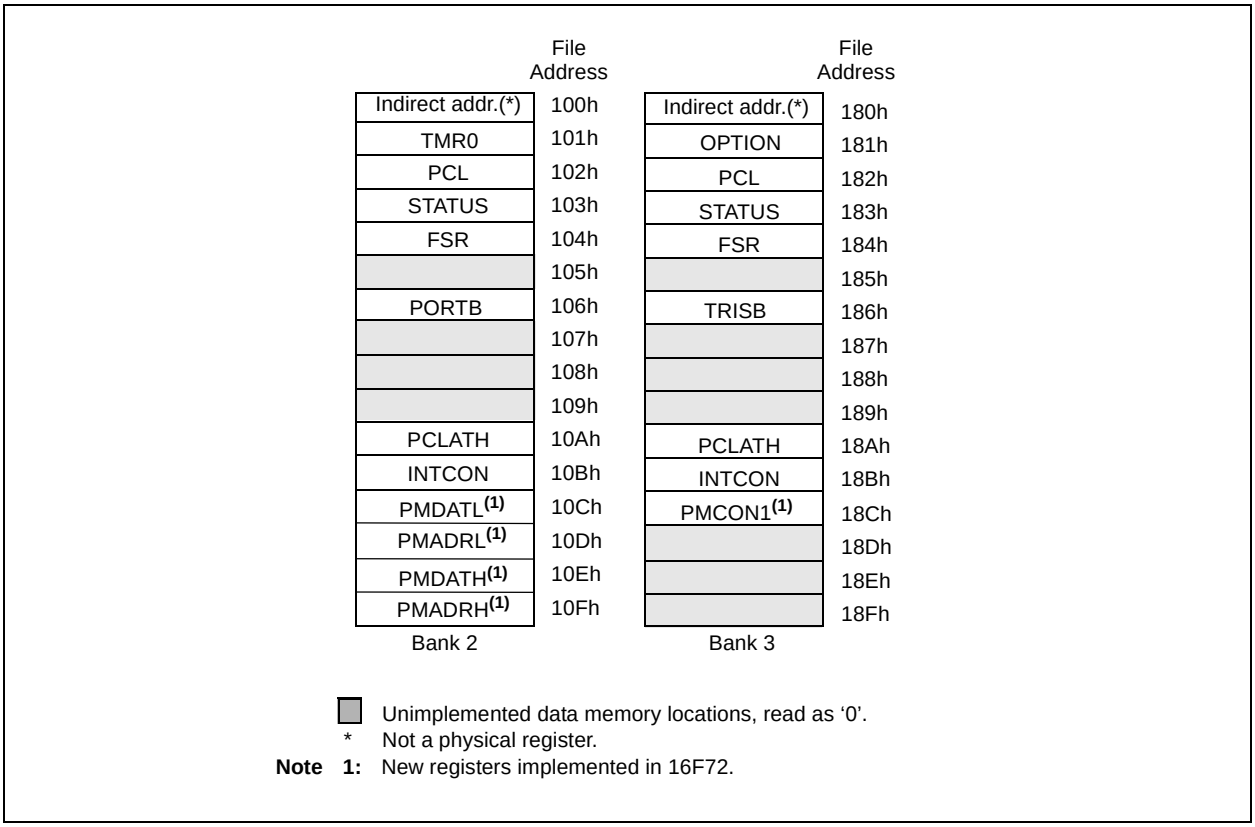

TABLE 3: PIC16C72A → PIC16F72 FUNCTIONAL DIFFERENCES

No.	Module	Differences from PIC16C72A	H/W	S/W	Prog
1	Program Memory Read	The FLASH Program Memory is readable during normal operation	—	Yes	—

Legend: H/W - Issues may exist with regard to the application circuit.
S/W - Issues may exist with regard to the user program.
Prog. - Issues may exist with regard to programming.

READING PROGRAM MEMORY

The FLASH Program Memory is readable during normal operation over the entire VDD range. It is indirectly addressed through Special Function Registers (SFR). Up to 14-bit numbers can be stored in memory for use as calibration parameters, serial numbers, packed 7-bit ASCII, etc. Executing a program memory location containing data that forms an invalid instruction results in a NOP.

There are five SFRs used to read the program and memory:

- PMCON1
- PMDATL
- PMDATH
- PMADRL
- PMADRH

The program memory allows word reads. Program memory access allows for checksum calculation and reading calibration tables.

When interfacing to the program memory block, the PMDATH:PMDATL registers form a two-byte word that holds 14-bit data for reads. The PMADRH:PMADRL registers form a two-byte word that holds the 13-bit address of the FLASH location being accessed. This device can have up to 2K words of program FLASH, with an address range from 0h to 07FFh. The unused upper bits in both the PMDATH and PMADRH registers are not implemented and read as zeroes.

PMADR

The address registers can address up to a maximum of 8K words of program FLASH.

When selecting a program address value, the MSByte of the address is written to the PMADRH register and the LSByte is written to the PMADRL register. The upper MSbits of PMADRH must always be clear.

PMCON1 Register

PMCON1 is the control register for memory access.

The control bit, RD, initiates read operations. This bit cannot be cleared, only set, in software. It is cleared in hardware at the completion of the read operation.

REGISTER 1: PMCON1: PROGRAM MEMORY CONTROL REGISTER (ADDRESS: 18Ch)

R-1	U-0	U-0	U-0	U-x	U-0	U-0	R/S-0
reserved	—	—	—	—	—	—	RD
bit 7							bit 0

bit 7 **Reserved:** Read as ‘1’

bit 6-1 **Unimplemented:** Read as ‘0’

bit 0 **RD:** Read Control bit

1 = Initiates a FLASH read, RD is cleared in hardware. The RD bit can only be set (not cleared) in software.

0 = Does not initiate a FLASH read

Legend:		
S = Settable bit	U = Unimplemented bit, read as ‘0’	
W = Writable bit	R = Readable bit	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

REGISTER 2: CONFIGURATION WORD (ADDRESS: 2007h)(1)

U-1	U-1	U-1	U-1	U-1	U-1	U-1	u-1	U-1	u-1	u-1	u-1	u-1	u-1
—	—	—	—	—	—	—	BOREN	—	CP	$\overline{\text{PWRTEN}}$	WDTEN	F0SC1	F0SC0
bit13													bit0

bit 13-7 **Unimplemented:** Read as '1'

bit 6 **BOREN:** Brown-out Reset Enable bit(2)
1 = BOR enabled
0 = BOR disabled

bit 5 **Unimplemented:** Read as '1'

bit 4 **CP:** FLASH Program Memory Code Protection bit
1 = Code protection off
0 = All memory locations code protected

bit 3 **$\overline{\text{PWRTEN}}$:** Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 2 **WDTEN:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0 **FOSC1:FOSC0:** Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: The erased (unprogrammed) value of the configuration word is 3FFFh.

2: Enabling Brown-out RESET automatically enables Power-up Timer (PWRT), regardless of the value of bit $\overline{\text{PWRTEN}}$. Ensure the Power-up Timer is enabled any time Brown-out Reset is enabled.

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
- n = Value when device is unprogrammed		u = Unchanged from programmed state

REGISTER 3: STATUS REGISTER (ADDRESS: 03h, 83h, 103h, 183h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)
1 = Bank 2, 3 (100h - 1FFh)
0 = Bank 0, 1 (00h - FFh)

bit 6-5 **RP1:RP0:** Register Bank Select bits (used for direct addressing)
Each bank is 128 bytes
11 = Bank 3 (180h - 1FFh)
10 = Bank 2 (100h - 17Fh)
01 = Bank 1 (80h - FFh)
00 = Bank 0 (00h - 7Fh)

bit 4 **$\overline{TO}$:** Time-out bit
1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit carry/$\overline{borrow}$ bit
(ADDWF, ADDLW, SUBLW, SUBWF instructions)**(1)**
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0 **C:** Carry/$\overline{borrow}$ bit
(ADDWF, ADDLW, SUBLW, SUBWF instructions)**(1,2)**
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand.

2: For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

TABLE 4: PIC16C72A → PIC16F72 ELECTRICAL CHARACTERISTICS DIFFERENCES

Characteristic	PIC16C72A Data Sheet	PIC16F72 Data Sheet	Units
Voltage on VDD with respect to Vss	-0.3 to 7.5	-0.3 to 6.5	V
Voltage on $\overline{\text{MCLR}}$ with respect to Vss (Note 1)	0 to 13.25	0 to 13.5	V
Voltage on RA4 with respect to Vss	0 to 8.5	0 to 12	V

Note 1: It is recommended to not tie the $\overline{\text{MCLR}}$ pin directly to VDD (see Figure 11-5 in the PIC16F72 Data Sheet for the recommended $\overline{\text{MCLR}}$ circuit).

TABLE 5: PIC16C72A → PIC16F72 ELECTRICAL SPECIFICATION DIFFERENCES

Parm. No.	Sym.	Characteristic	PIC16C72A Data Sheet			PIC16F72 Data Sheet			Units	Conditions
			Min	Typ†	Max	Min	Typ†	Max		
D010	IDD	**Supply Current (Notes 1, 2)**	—	2.7	5.0	—	0.9	4.0	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 5.5V **(Note 4)**
D013			—	10.0	20.0	—	5.2	15.0	mA	HS osc configuration FOSC = 10 MHz, VDD = 5.5V
D020	IPD	**Power-down Current (Notes 2,3)**	—	10.5	42.0	—	5.0	42.0	µA	VDD = 4.0V, WDT enabled, -40°C to +85°C
D021			—	1.5	19.0	—	0.1	19.0	µA	VDD = 4.0V, WDT enabled, -40°C to +85°C
D023*	ΔIBOR	**Brown-out Reset Current (Note 5)**	—	TBD	200	—	25	200	µA	BOR Enabled, VDD = 5.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption. The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

2: Timer1 oscillator (when enabled) adds approximately 20 mA to the specification. This value is from characterization and is for design guidance only. This is not tested.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

TABLE 6: PIC16C72A → PIC16F72 DC CHARACTERISTICS DIFFERENCES

Parm. No.	Sym.	Characteristic	PIC16C72A Data Sheet			PIC16F72 Data Sheet			Units	Conditions
			Min	Typ†	Max	Min	Typ†	Max		
D042A	VIH	**Input High Voltage**	0.7 VDD 0.7 VDD	— —	VDD VDD	1.6 0.7 VDD	— —	VDD VDD	V V	OSC1 (in XT and LP mode) OSC1 (in HS mode) **(Note 1)**
D150*	VOD	**Open Drain High Voltage**	—	—	8.5	—	—	12	V	RA4 pin
D130	EP	**Program FLASH Memory Endurance**	—	—	—	100	1000	—	E/W	25°C at 5V
D131	VPR	**VDD for Program FLASH Memory Read**	—	—	—	2.0	—	5.5	V	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: For RC osc configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC16F72 be driven with external clock in RC mode.

TABLE 7: PIC16C72A → PIC16F72 ADC MODULE DIFFERENCES

Parm. No.	Sym.	Characteristic	PIC16C72A Data Sheet			PIC16F72 Data Sheet			Units	Conditions
			Min	Typ†	Max	Min	Typ†	Max		
A020	VREF	**Reference Voltage**	2.5 2.5	— —	VDD+0.3 VDD+0.3	2.5 2.2	— —	VDD+0.3 VDD+0.3	V V	-40°C to +85°C 0°C to +85°C
131	TCNV	**Conversion Time (not including S/H time) (Note 1)**	11	—	11	9	—	9	TAD	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

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