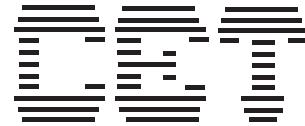


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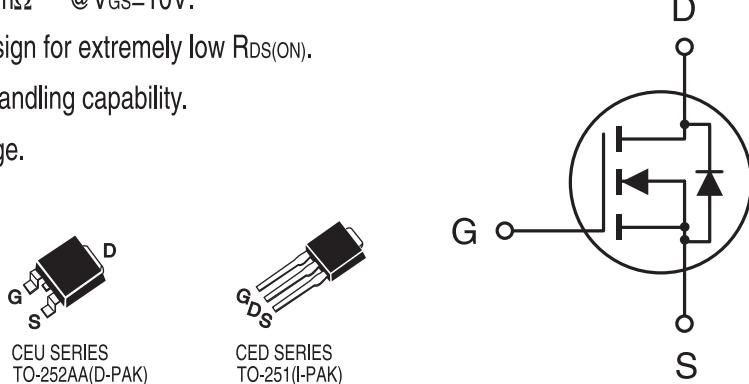
PRELIMINARY

N-Channel Enhancement Mode Field Effect Transistor

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FEATURES

- 200V , 18A , $R_{DS(ON)}=180\text{m}\Omega$ @ $V_{GS}=10\text{V}$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- TO-251 & TO-252 package.



ABSOLUTE MAXIMUM RATINGS (T_c=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	200	V
Gate-Source Voltage	V _{GS}	± 20	V
Drain Current-Continuous -Pulsed	I _D	18	A
	I _{DM}	72	A
Drain-Source Diode Forward Current	I _S	18	A
Maximum Power Dissipation @ T _c =25°C Derate above 25°C	P _D	50	W
		0.3	W/°C
Operating and Storage Temperature Range	T _J , T _{TSG}	-55 to 175	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	R _{θJC}	3	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	°C/W

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ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}} = 0\text{V}, I_{\text{D}} = 250\mu\text{A}$	200			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 200\text{V}, V_{\text{GS}} = 0\text{V}$		25		μA
Gate-Body Leakage	I_{GSS}	$V_{\text{GS}} = \pm 20\text{V}, V_{\text{DS}} = 0\text{V}$			± 100	nA
ON CHARACTERISTICS^a						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_{\text{D}} = 250\mu\text{A}$	2		4	V
Drain-Source On-State Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}} = 10\text{V}, I_{\text{D}} = 11\text{A}$			180	$\text{m}\Omega$
On-State Drain Current	$I_{\text{D}(\text{ON})}$	$V_{\text{GS}} = 10\text{V}, V_{\text{DS}} = 10\text{V}$	18			A
Forward Transconductance	g_{FS}	$V_{\text{DS}} = 50\text{V}, I_{\text{D}} = 11\text{A}$	6.7			S
DYNAMIC CHARACTERISTICS^b						
Input Capacitance	C_{iss}	$V_{\text{DS}} = 25\text{V}, V_{\text{GS}} = 0\text{V}$ $f = 1.0\text{MHz}$		1250	1700	pF
Output Capacitance	C_{oss}			188	250	pF
Reverse Transfer Capacitance	C_{rss}			60	80	pF
SWITCHING CHARACTERISTICS^b						
Turn-On Delay Time	$t_{\text{D}(\text{ON})}$	$V_{\text{DD}} = 100\text{V},$ $I_{\text{D}} = 11\text{A},$ $V_{\text{GS}} = 10\text{V},$ $R_{\text{GEN}} = 9.1\Omega$		16	30	ns
Rise Time	t_r			70	105	ns
Turn-Off Delay Time	$t_{\text{D}(\text{OFF})}$			50	85	ns
Fall time	t_f			55	70	ns
Total Gate Charge	Q_g	$V_{\text{DS}} = 160\text{V}, I_{\text{D}} = 18\text{A},$ $V_{\text{GS}} = 10\text{V}$		64	80	nC
Gate-Source Charge	Q_{gs}			12		nC
Gate-Drain Charge	Q_{gd}			37		nC

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CEDF640/CEUF640

ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS ^a						
Diode Forward Voltage	V_{SD}	$V_{GS} = 0\text{V}$, $I_S = 18\text{A}$			1.5	V

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Notes

- a. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

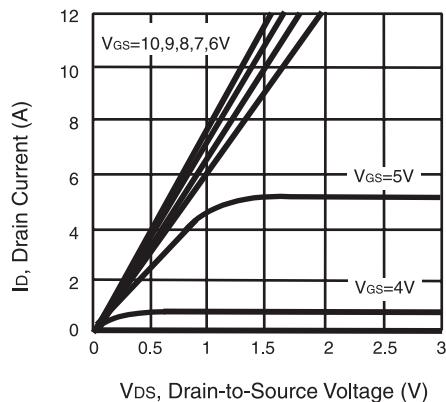


Figure 1. Output Characteristics

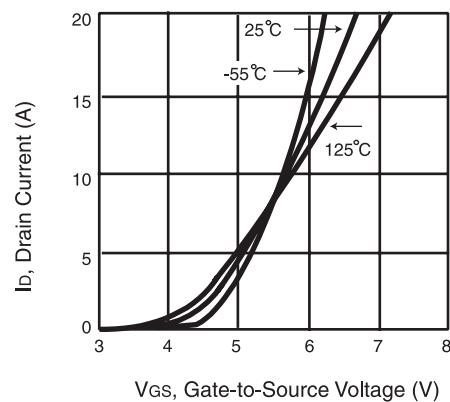


Figure 2. Transfer Characteristics

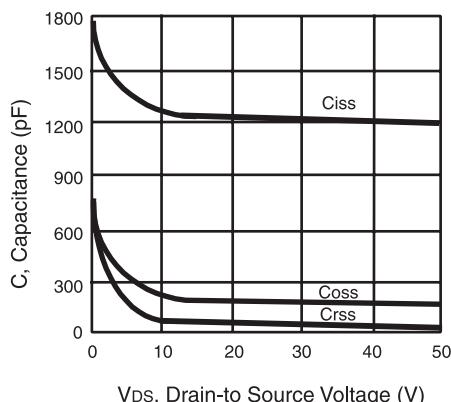


Figure 3. Capacitance

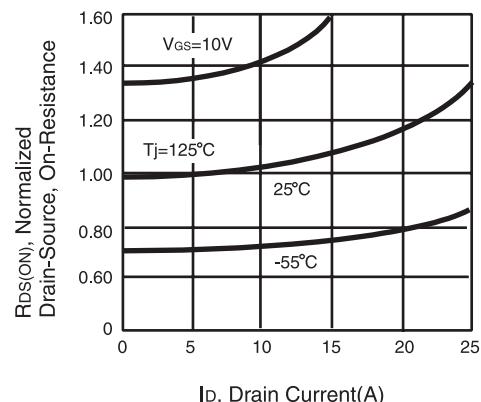


Figure 4. On-Resistance Variation with Drain Current and Temperature

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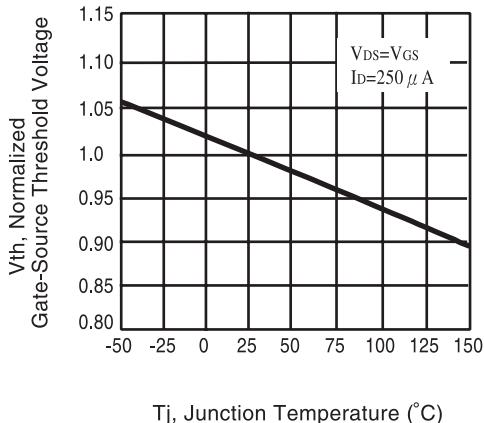
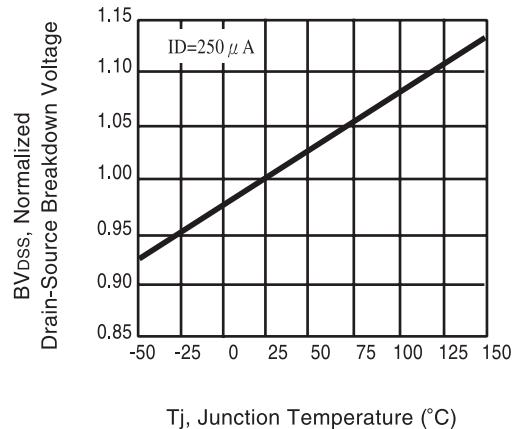


Figure 5. Gate Threshold Variation with Temperature



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Figure 6. Breakdown Voltage Variation with Temperature

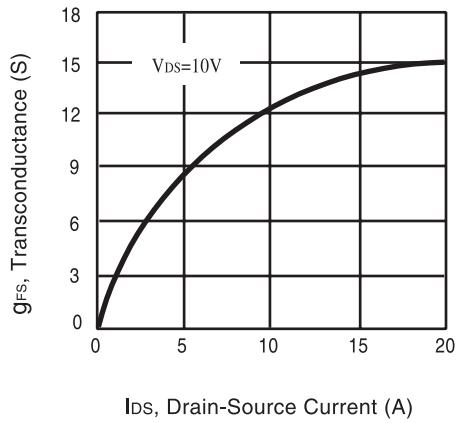


Figure 7. Transconductance Variation with Drain Current

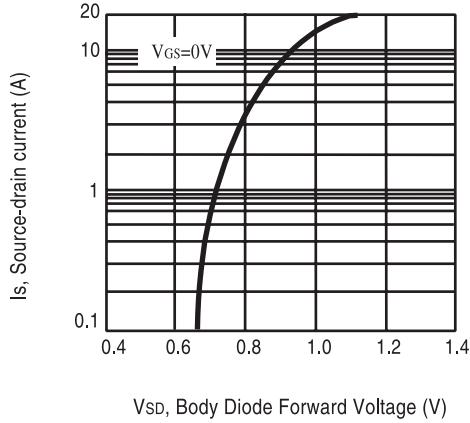


Figure 8. Body Diode Forward Voltage Variation with Source Current

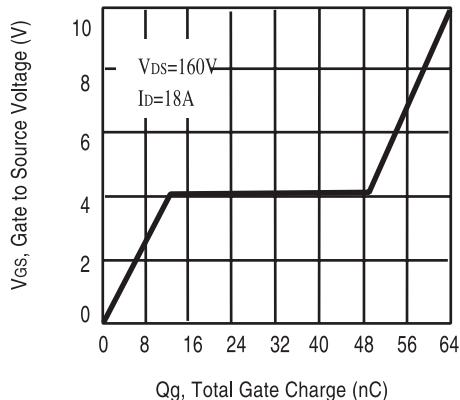


Figure 9. Gate Charge

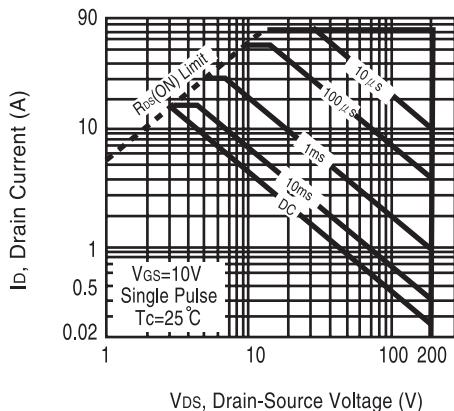


Figure 10. Maximum Safe Operating Area

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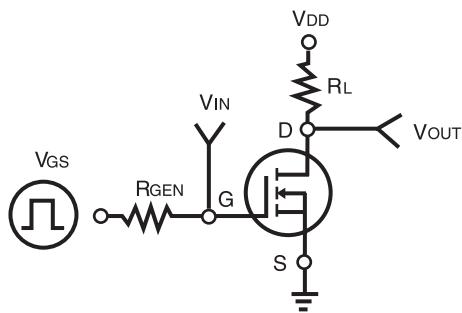


Figure 11. Switching Test Circuit

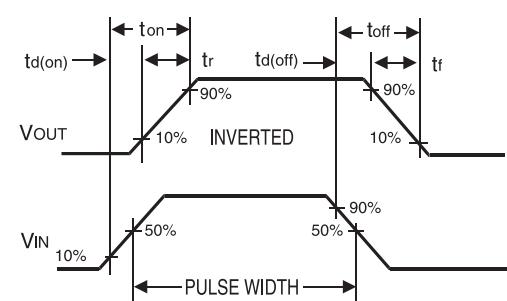


Figure 12. Switching Waveforms

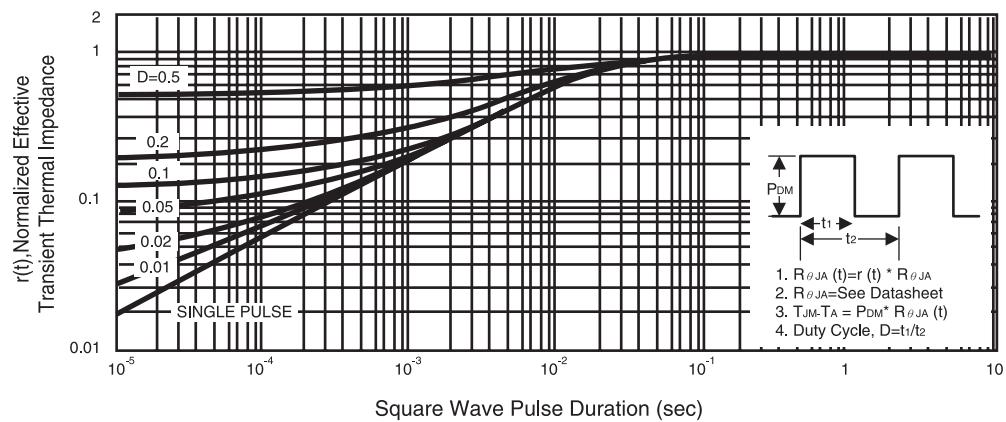


Figure 13. Normalized Thermal Transient Impedance Curve