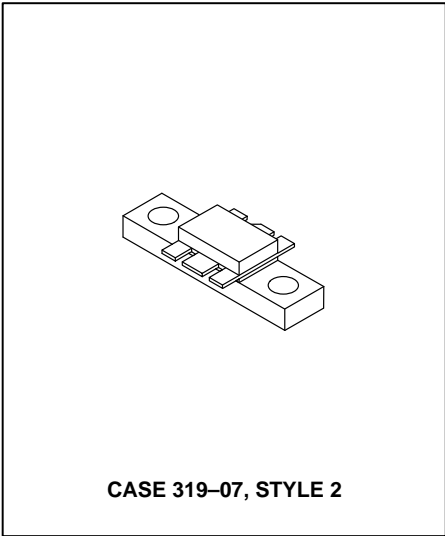


# The RF Line

## NPN Silicon

### RF Power Transistor



The TP3032 is designed for 26 volts, common emitter, 960 MHz base station amplifiers, for use in analog and digital systems.

- Specified 26 Volts, 960 MHz Characteristics  
Output Power — 21 Watts  
Gain — 7.5 dB min
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Class AB Operation
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CER}$	40	Vdc
Collector–Base Voltage	$V_{CBO}$	48	Vdc
Emitter–Base Voltage	$V_{EBO}$	3.5	Vdc
Collector–Current — Continuous	$I_C$	4	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	52.5 0.3	Watts W/ $^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	– 65 to +150	$^\circ\text{C}$
Operating Junction Temperature	$T_J$	200	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (1)	$R_{\theta JC}$	3.3	$^\circ\text{C}/\text{W}$

#### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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#### OFF CHARACTERISTICS

Collector–Emitter Breakdown Voltage ( $I_C = 30\text{ mA}$ , $R_{BE} = 75\ \Omega$ )	$V_{(BR)CER}$	40	—	—	Vdc
Emitter–Base Breakdown Voltage ( $I_E = 5\text{ mAdc}$ )	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector–Base Breakdown Voltage ( $I_C = 30\text{ mAdc}$ )	$V_{(BR)CBO}$	48	—	—	Vdc
Collector–Emitter Leakage ( $V_{CE} = 26\text{ V}$ , $R_{BE} = 75\ \Omega$ )	$I_{CER}$	—	—	8	mA

#### ON CHARACTERISTICS

DC Current Gain ( $I_C = 1\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ )	$h_{FE}$	15	—	80	—
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NOTE:

- Thermal resistance is determined under specified RF operating condition.

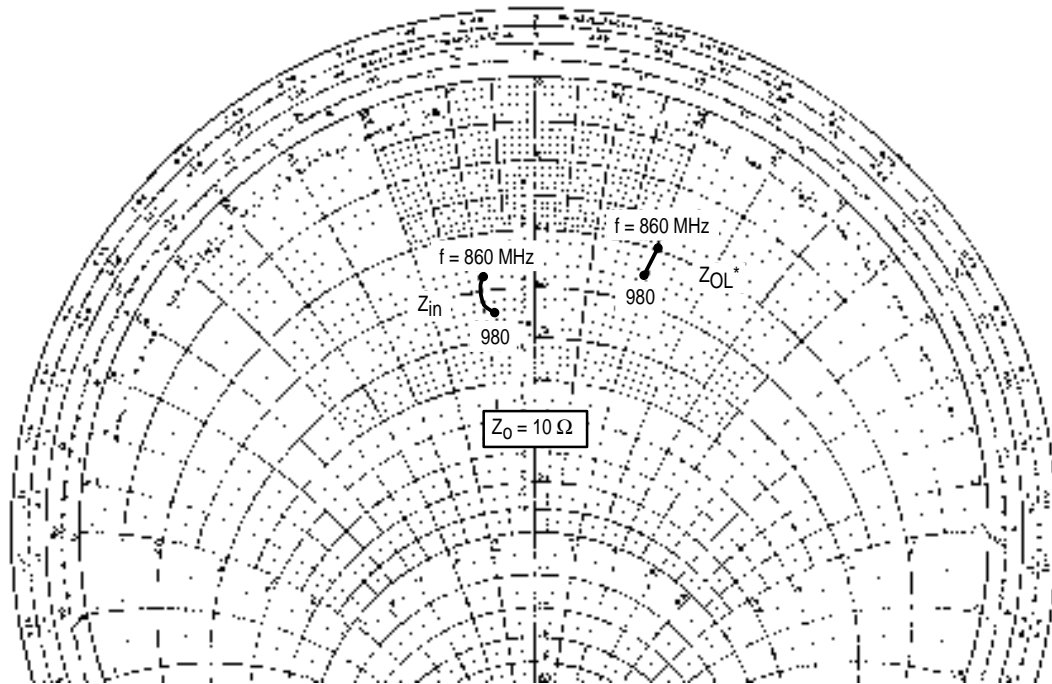
(continued)

**ELECTRICAL CHARACTERISTICS — continued** ( $T_C = 25^\circ\text{C}$  unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>DYNAMIC CHARACTERISTICS</b>					
Output Capacitance ( $V_{CB} = 26\text{ V}$ , $I_E = 0$ , $f = 1\text{ MHz}$ )	$C_{ob}$	—	30	—	pF

**FUNCTIONAL TESTS**

Common-Emitter Amplifier Gain ( $V_{CC} = 26\text{ V}$ , $P_{out} = 21\text{ W}$ , $I_{CQ} = 100\text{ mA}$ , $f = 960\text{ MHz}$ )	$G_p$	7.5	8.5	—	dB
Load Mismatch ( $V_{CC} = 26\text{ V}$ , $P_{out} = 21\text{ W}$ , $I_{CQ} = 100\text{ mA}$ , Load VSWR = 5:1, at All Phase Angles at Frequency of Test)	$\psi$	No Degradation in Output Power			
Collector Efficiency ( $V_{CC} = 26\text{ V}$ , $P_{out} = 21\text{ W}$ , $f = 960\text{ MHz}$ )	$\eta$	50	55	—	%
Over Drive ( $V_{CC} = 26\text{ V}$ , $P_{in} = 6\text{ W}$ , $f = 960\text{ MHz}$ )	OD	No Degradation in Output Power			

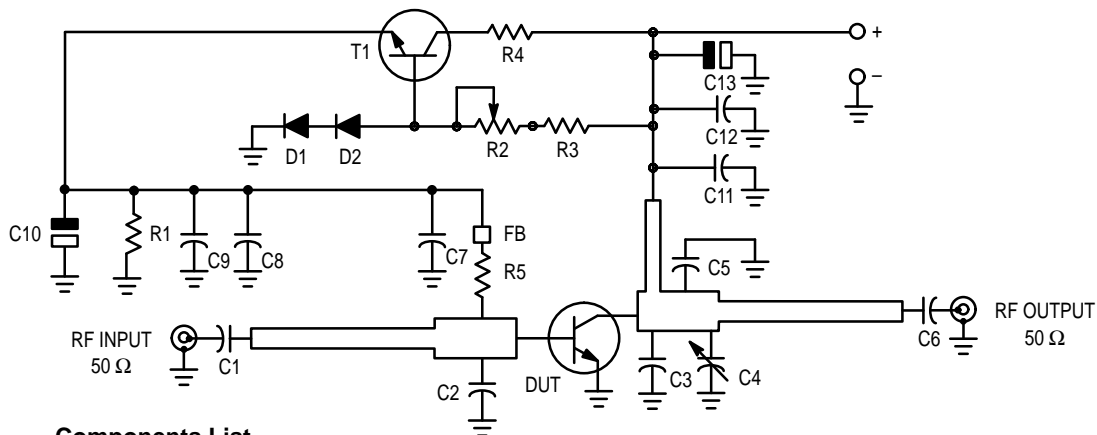


$V_{CE} = 26\text{ V}$        $P_{out} = 21\text{ W}$

f (MHz)	$Z_{in}$ ( $\Omega$ )	$Z_{OL}^*$ ( $\Omega$ )
860	$2.9 - j0.4$	$2 + j2.2$
880	$2.9 - j0.9$	$2.1 + j2.2$
900	$2.9 - j1.45$	$2.25 + j2.5$
935	$3.2 - j0.95$	$2.4 + j2.3$
960	$3.25 - j1.5$	$2.5 + j2$
980	$3.55 - j1.1$	$2.6 + j2.15$

$Z_{OL}^*$  = Conjugate of optimum load impedance into which the device operates at a given output power, voltage, current and frequency.

**Figure 1. Series Equivalent Input and Output Impedances**

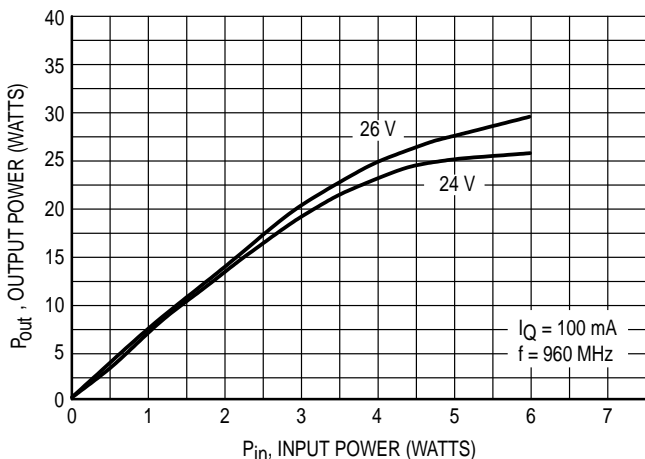


**Components List**

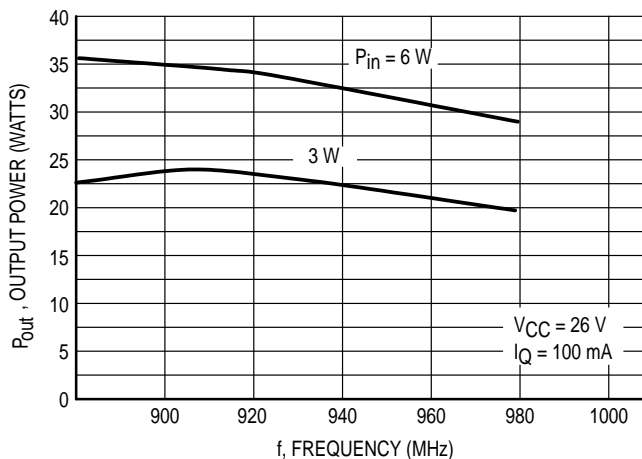
C1	300 pF, ATC Chip Capacitor 100B	D1,D2	Diode, 1N4148
C2	12 pF, ATC Chip Capacitor 100A	FB	Ferrite Bead
C3	10 pF, ATC Chip Capacitor 100A	R1	75 $\Omega$ , Chip Resistor 1206
C4	1–4.5 pF, Johanson Capacitor 9410–0	R2	10 k $\Omega$ , Trimmer Resistor
C5	6.8 pF, ATC Chip Capacitor 100A	R3	1 k $\Omega$ , 1/2 W, Resistor
C6	82 pF, ATC Chip Capacitor 100B	R4	82 $\Omega$ , 3 W, Resistor
C7,C8,C11	330 pF, Chip Capacitor	R5	1 $\Omega$ , 1/4 W, Resistor
C9,C12	15 nF, Chip Capacitor	T1	Transistor, BD135
C10,C13	6.8 $\mu$ F, 35 V, Tantalum Capacitor		

**Figure 2. 960 MHz Test Circuit Schematic**

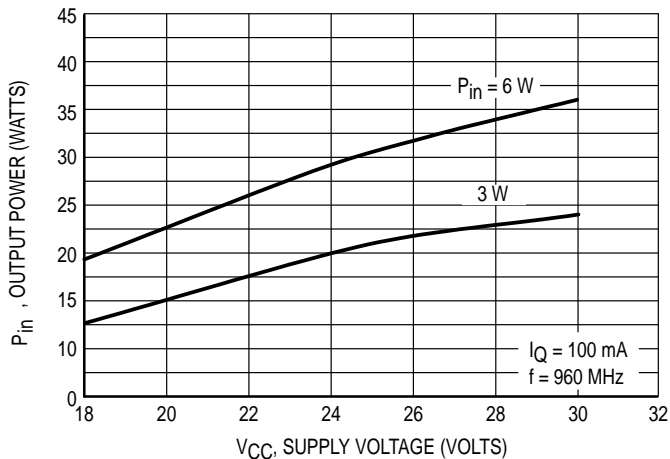
**TYPICAL CHARACTERISTICS**



**Figure 3. Output Power versus Input Power**



**Figure 4. Output Power versus Frequency**



**Figure 5. Output Power versus Supply Voltage**

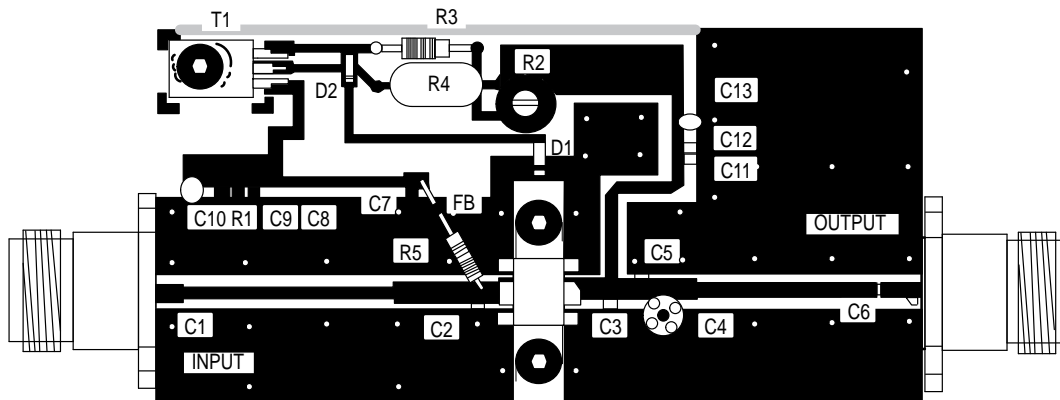
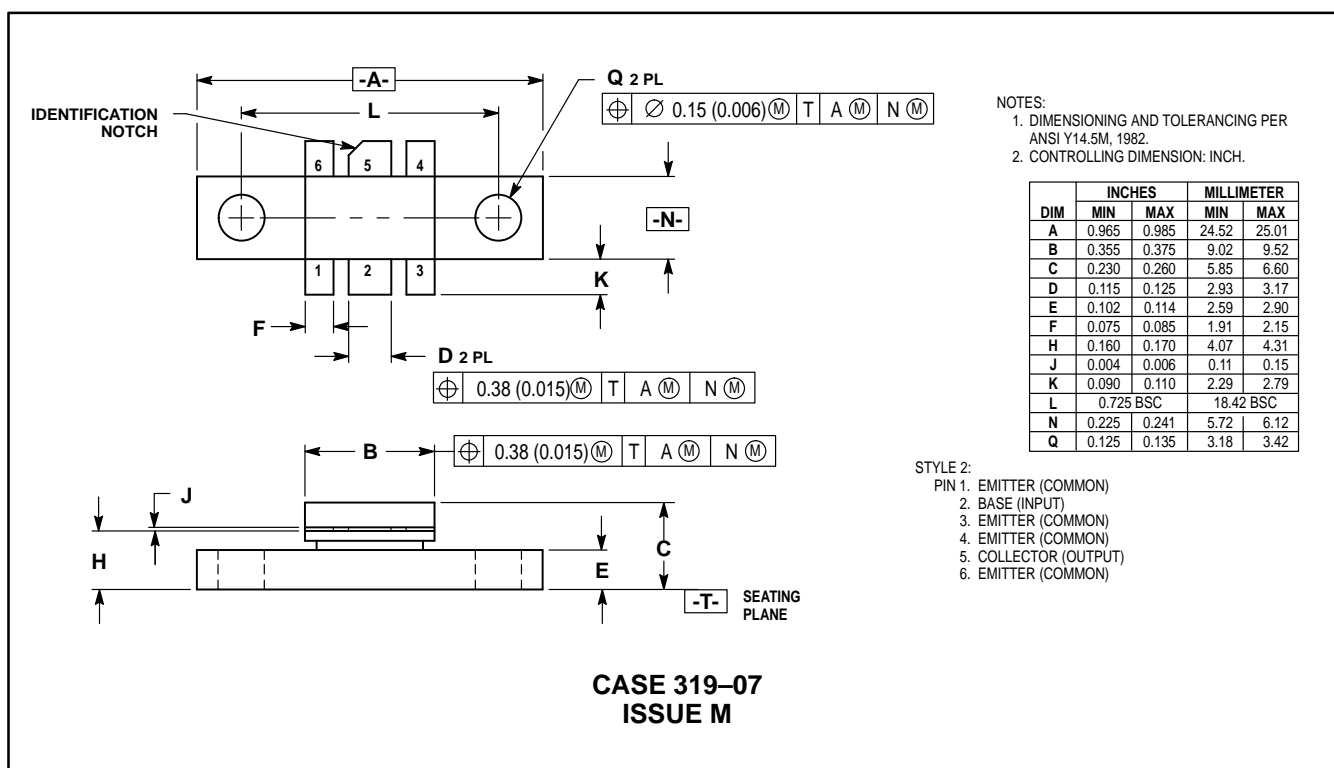


Figure 6. Test Circuit Components View

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