

Si4416DY

N-channel enhancement mode field-effect transistor

Rev. 01 — 05 June 2001

Product data

1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™¹ technology.

Product availability:

Si4416DY in SOT96-1 (SO8).

2. Features

- Low on-state resistance
- Fast switching
- TrenchMOS™ technology.

3. Applications

- DC to DC convertors
- DC motor control
- Lithium-ion battery applications
- Notebook PC
- Portable equipment applications.

4. Pinning information

Table 1: Pinning - SOT96-1, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)		
4	gate (g)		
5,6,7,8	drain (d)		

1. TrenchMOS is a trademark of Royal Philips Electronics.



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5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 150 °C	–	30	V
I_D	drain current	$T_{amb} = 25$ °C; pulsed; $t_p \leq 10$ s	–	9	A
P_{tot}	total power dissipation	$T_{amb} = 25$ °C; pulsed; $t_p \leq 10$ s	–	2.5	W
T_j	junction temperature		–	150	°C
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 9$ A	14	18	mΩ
		$V_{GS} = 4.5$ V; $I_D = 7.3$ A	21	28	mΩ

6. Limiting values

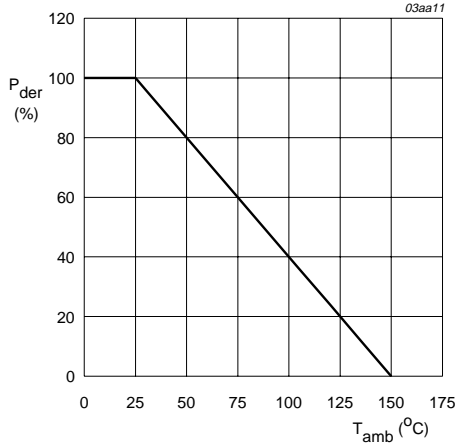
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 150 °C	–	30	V
V_{GS}	gate-source voltage (DC)		–	± 20	V
I_D	drain current	$T_{amb} = 25$ °C; pulsed; $t_p \leq 10$ s; Figure 2 and 3	–	9	A
		$T_{amb} = 70$ °C; pulsed; $t_p \leq 10$ s; Figure 2	–	7.2	A
I_{DM}	peak drain current	$T_{amb} = 25$ °C; pulsed; $t_p \leq 10$ μs; Figure 3	–	50	A
P_{tot}	total power dissipation	$T_{amb} = 25$ °C; pulsed; $t_p \leq 10$ s;	–	2.5	W
		$T_{amb} = 70$ °C; pulsed; $t_p \leq 10$ s; Figure 1	–	1.6	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C

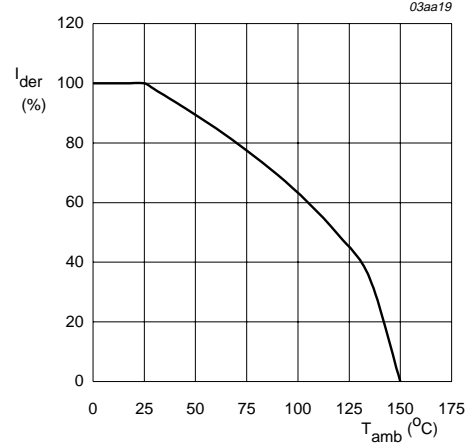
Source-drain diode

I_S	source (diode forward) current (DC)	$T_{amb} = 25$ °C; pulsed; $t_p \leq 10$ s	–	2.1	A
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$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

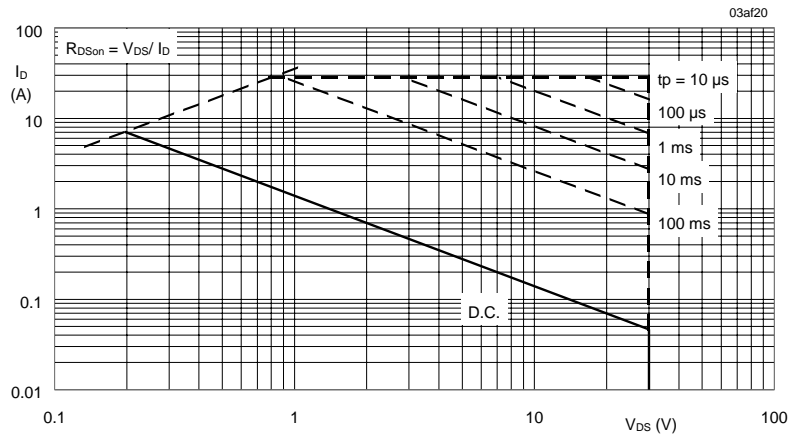
Fig 1. Normalized total power dissipation as a function of ambient temperature.



$$V_{GS} \geq 10 \text{ V}$$

$$I_D = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of ambient temperature.



T_{amb} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; minimum footprint; $t \leq 10$ sec. Figure 4	50	K/W

7.1 Transient thermal impedance

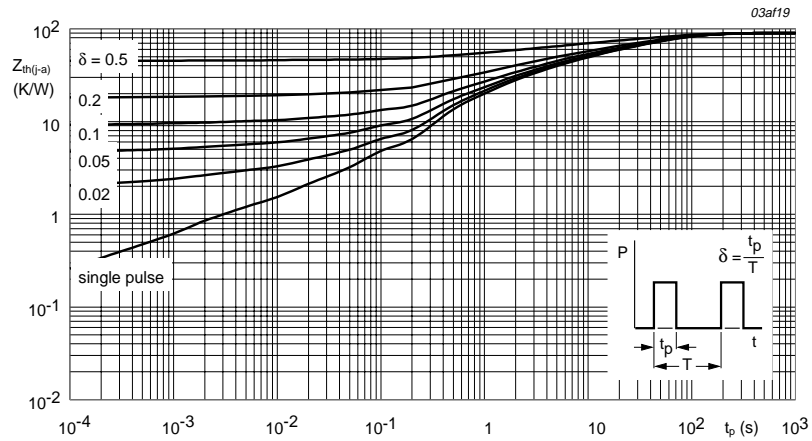


Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration.

8. Characteristics

Table 5: Characteristics

$T_j = 25\text{ °C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 250\ \mu\text{A}$; $V_{DS} = V_{GS}$; Figure 9	1	–	–	V
I_{DSS}	drain-source leakage current	$V_{DS} = 24\ \text{V}$; $V_{GS} = 0\ \text{V}$	–	–	1	μA
		$T_j = 25\text{ °C}$	–	–	25	μA
		$T_j = 55\text{ °C}$	–	–	100	nA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\ \text{V}$; $V_{DS} = 0\ \text{V}$	–	–	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$; $I_D = 9\ \text{A}$; Figure 7 and 8	–	14	18	m Ω
		$V_{GS} = 4.5\ \text{V}$; $I_D = 7.3\ \text{A}$; Figure 7 and 8	–	21	28	m Ω
Dynamic characteristics						
g_{fs}	forward transconductance	$V_{DS} = 15\ \text{V}$; $I_D = 9\ \text{A}$; Figure 11	–	22	–	S
$Q_{g(tot)}$	total gate charge	$I_D = 9\ \text{A}$; $V_{DD} = 15\ \text{V}$; $V_{GS} = 5\ \text{V}$; Figure 14	–	18	25	nC
$Q_{g(tot)}$	total gate charge	$I_D = 9\ \text{A}$; $V_{DD} = 15\ \text{V}$; $V_{GS} = 10\ \text{V}$; Figure 14	–	30	40	nC
Q_{gs}	gate-source charge		–	6	–	nC
Q_{gd}	gate-drain (Miller) charge		–	6	–	nC
$t_{d(on)}$	turn-on delay time	$V_{DD} = 15\ \text{V}$; $R_D = 15\ \Omega$; $V_{GS} = 10\ \text{V}$; $R_G = 6\ \Omega$	–	8	20	ns
t_r	turn-on rise time		–	10	20	ns
$t_{d(off)}$	turn-off delay time		–	40	60	ns
t_f	turn-off fall time			30	45	ns
Source-drain (reverse) diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 2.3\ \text{A}$; $V_{GS} = 0\ \text{V}$; Figure 13	–	0.75	1.2	V
t_{rr}	reverse recovery time	$I_S = 2.3\ \text{A}$; $di_S/dt = -100\ \text{A}/\mu\text{s}$; $V_{GS} = 0\ \text{V}$	–	50	80	ns

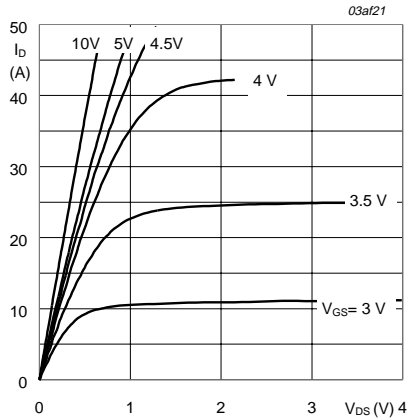


Fig 5. Output characteristic; drain current as function of drain-source voltage; typical values.

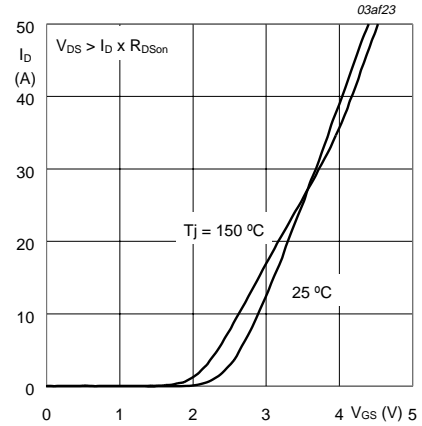
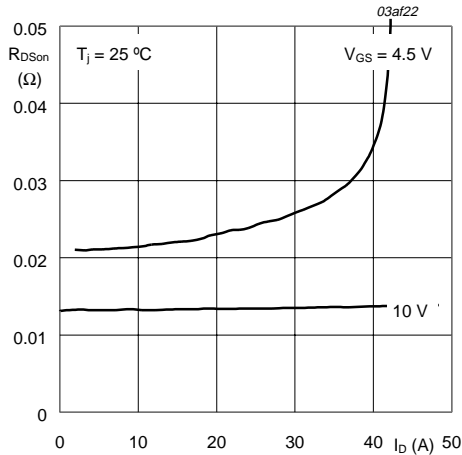
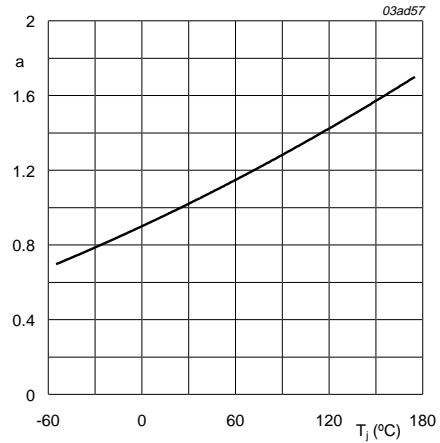


Fig 6. Transfer characteristic: drain current as function of gate-source voltage; typical values
 $T_j = 25\text{ °C}$ and 150 °C ; $V_{DS} > I_D \times R_{DSon}$



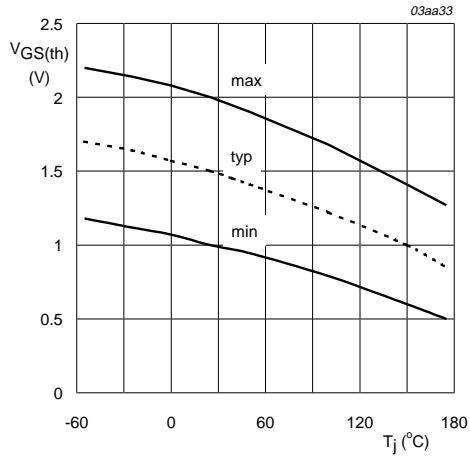
$T_j = 25\text{ °C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



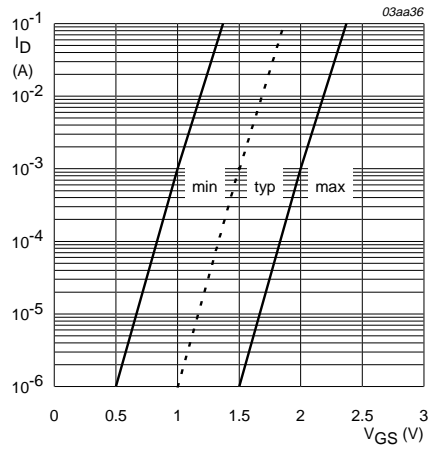
$$a = \frac{R_{DSon}}{R_{DSon(25\text{°C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



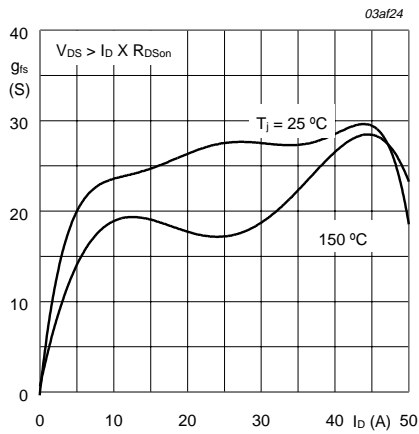
$I_D = 250 \mu A$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



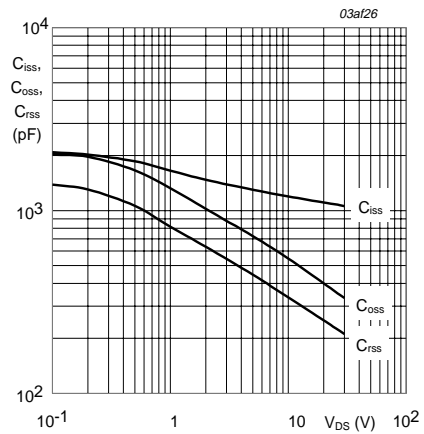
$T_j = 25 \text{ }^\circ\text{C}$; $V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



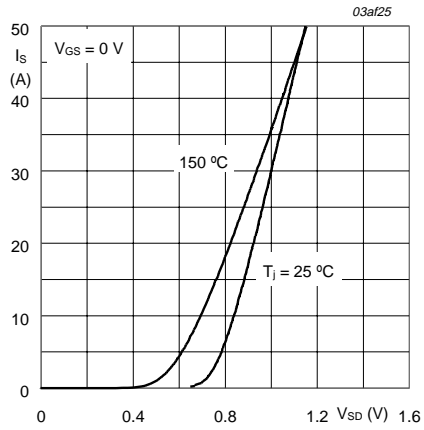
$T_j = 25 \text{ }^\circ\text{C}$ and $150 \text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{Dson}$

Fig 11. Forward transconductance as a function of drain current; typical values.



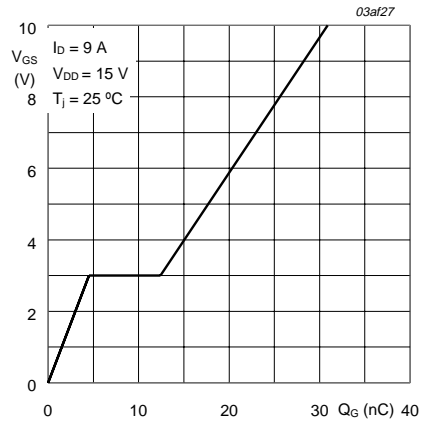
$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{GS} = 0\text{ V}$

Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 9\text{ A}$; $V_{DD} = 15\text{ V}$

Fig 14. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

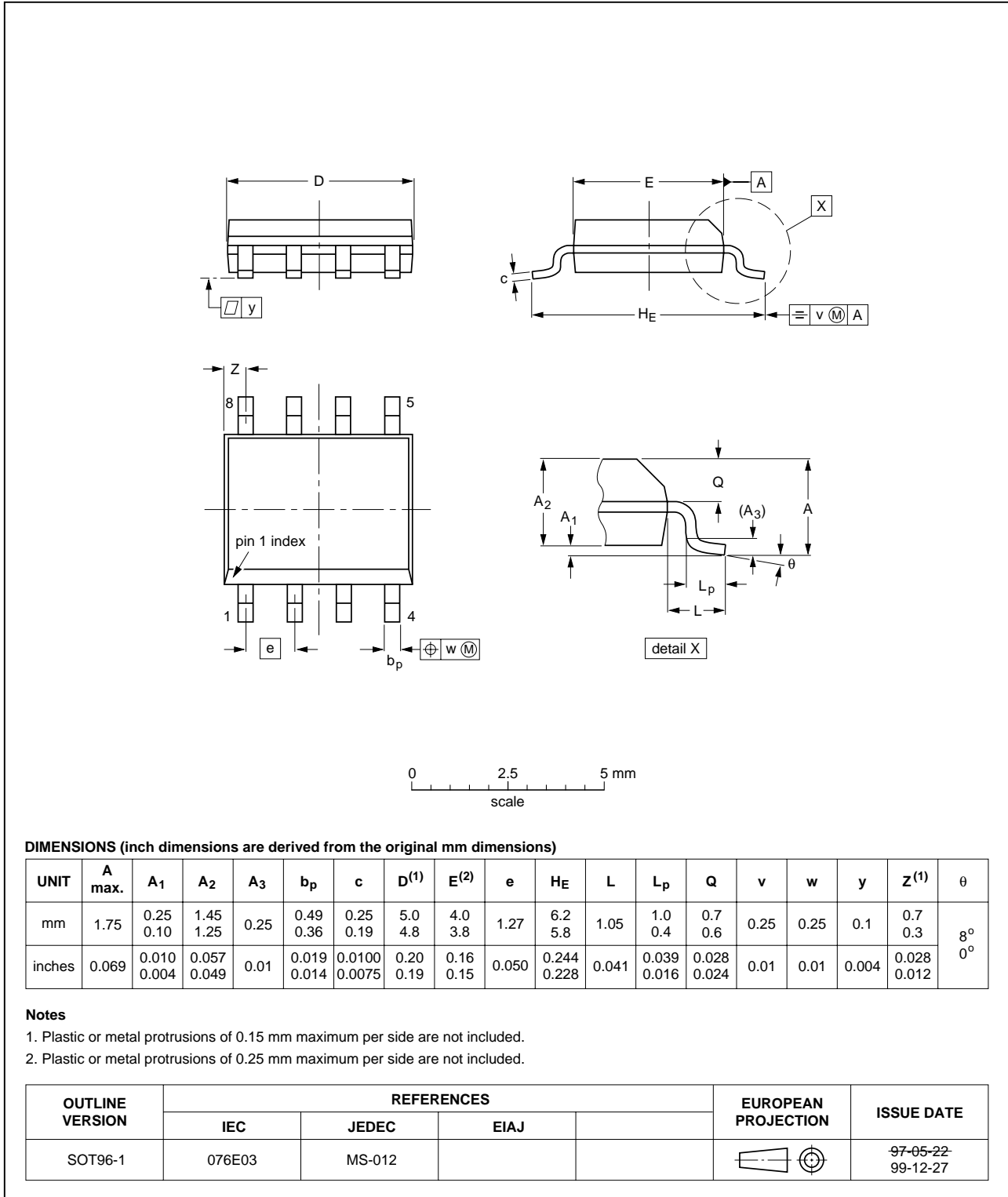


Fig 15. SOT96-1 (SO8).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20010605	-	Product specification; initial version

11. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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