

# LH5PV16256

## CMOS 4M (256K × 16) Pseudo-Static RAM

### FEATURES

- 262,144 words × 16 bit organization
- Power supply: +3.0 ± 0.15 V
- Access time: 120 ns (MAX.)
- Cycle time: 190 ns (MIN.)
- Power consumption (MAX.):
  - 126 mW (Operating)
  - 94.5 μW (Standby = CMOS input level)
  - 220.5 μW (Self-refresh = CMOS input level)
- LVTTL compatible I/O
- Available for address refresh, auto-refresh, and self-refresh modes
- 2,048 refresh cycles/32 ms
- Address non-multiple
- Available for byte write mode using  $\overline{UWE}$  and  $\overline{LWE}$  pins
- Package:
  - 44-pin, TSOP (Type II)
- Process: Silicon-gate CMOS
- Operating temperature: 0 - 70°C
- Not designed or rated as radiation hardened

### DESCRIPTION

The LH5PV16256 is a 4M bit Pseudo-Static RAM with a 262,144 words × 16 bit organization.

### PIN CONNECTIONS

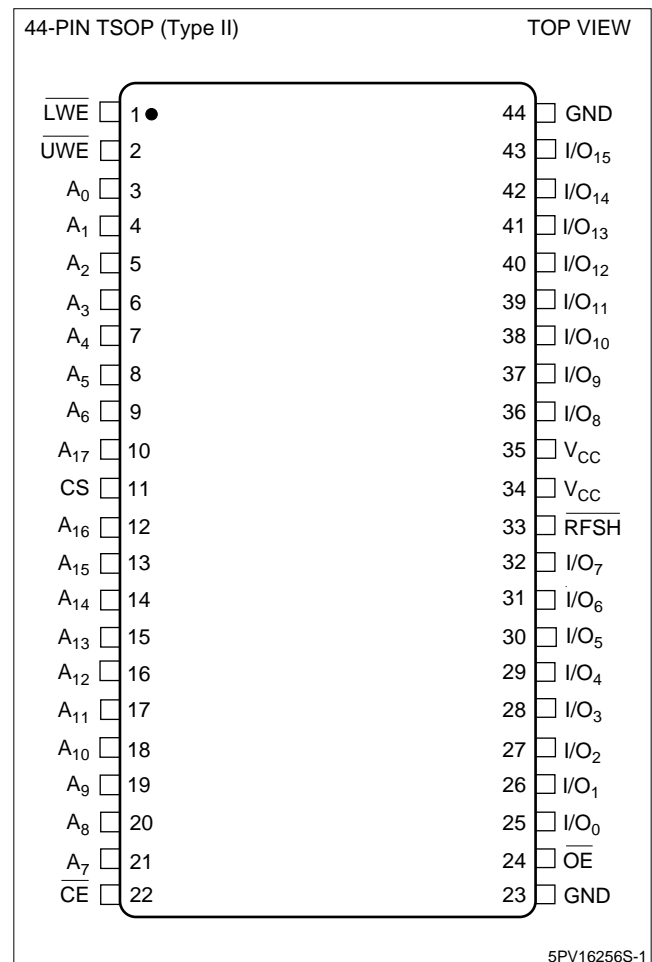
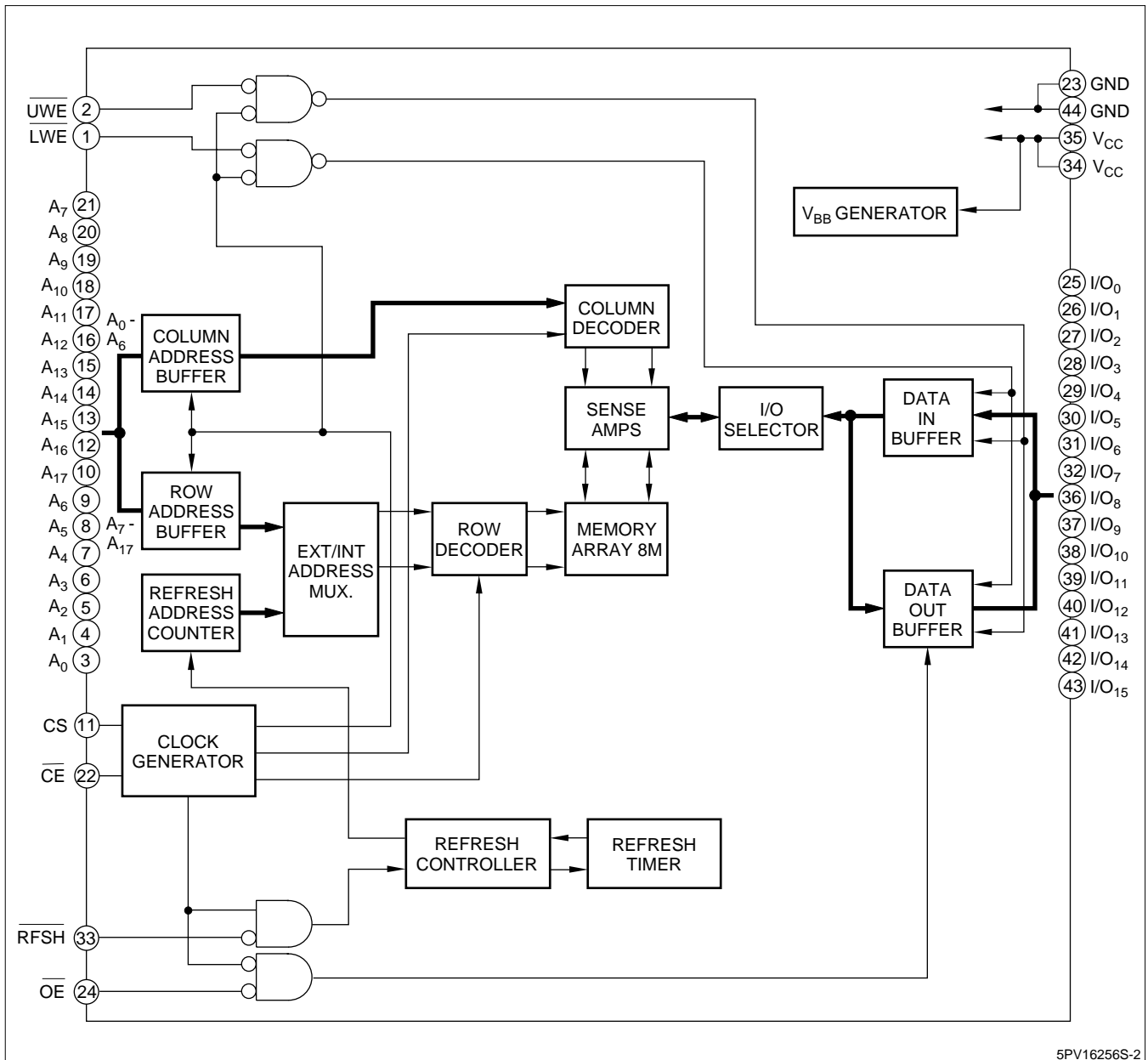


Figure 1. Pin Connections



5PV16256S-2

Figure 2. LH5PV16256 Block Diagram

**PIN DESCRIPTION**

PIN NAME	FUNCTION
A <sub>7</sub> - A <sub>17</sub>	Row address input
A <sub>0</sub> - A <sub>6</sub>	Column address input
UWE, LWE	Upper/lower write enable input
OE	Output enable input
RFSH	Refresh input
CE	Chip enable input

PIN NAME	FUNCTION
CS	Chip select input
I/O <sub>8</sub> - I/O <sub>15</sub>	Upper byte data input/output
I/O <sub>0</sub> - I/O <sub>7</sub>	Lower byte data input/output
V <sub>CC</sub>	Power supply
GND	Ground

## TRUTH TABLE

$\overline{CE}$	CS	$\overline{RFSH}$	$\overline{OE}$	$\overline{UWE}$	$\overline{LWE}$	MODE	I/O <sub>0 - 7</sub>	I/O <sub>8 - 15</sub>	
L	H	H	L	H	H	Word Read	Output data	Output data	
L	H	H	X	H	L	Write	Lower byte write	Input data	Don't care
				L	H		Upper byte write	Don't care	Input data
				L	L		Word write	Input data	Input data
				H	H		Invalid	High-Z	High-Z
H	X	L	X	X	X	Auto refresh	High-Z	High-Z	
L	L	H	X	X	X	CS standby	High-Z	High-Z	
H	X	H	X	X	X	Standby	High-Z	High-Z	

### NOTES:

H = High

L = Low

X = Don't care

## REQUIREMENTS

### $\overline{2WE}$ control

Please do not separate the  $\overline{UWE}$  and  $\overline{LWE}$  operation timing intentionally in the same write cycles. Each of the  $\overline{UWE}/\overline{LWE}$  should satisfy the timing specifications individually.

### Refresh after self-refresh or data retention mode

- If address refresh is used during normal read/write cycles, the first address refresh must be executed within 15  $\mu$ s after self-refresh or data retention mode ends and the address refresh must be executed continuously for 2,048 refresh cycles.
- If distributed auto-refresh is used during normal read/write cycles, the first auto-refresh must be executed within 15  $\mu$ s after self-refresh or data retention mode ends.
- If burst auto-refresh is used during normal read/write cycles, the first auto-refresh must be executed within 15  $\mu$ s after self-refresh or data retention mode ends, and the auto-refresh must be executed continuously for 2,048 refresh cycles.

### Bypass capacitor for power supply noise reduction

Because a PSRAM operates dynamically like a DRAM, it is recommended to put bypass capacitors between  $V_{CC}$  and GND to absorb power supply noise due to the peak current.

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	$V_T$	-0.5 to +4.6	V	1
Output short circuit current	$I_O$	50	mA	—
Power dissipation	$P_D$	600	mW	—
Operating temperature	$T_{OPR}$	0 to +70	°C	—
Storage temperature	$T_{STG}$	-65 to +150	°C	—

### NOTE:

1. The maximum applicable voltage on any pin with respect to GND.

## RECOMMENDED OPERATING CONDITIONS ( $T_A = 0$ to $+70^\circ\text{C}$ )

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	$V_{CC}$	2.85	3.0	3.15	V	1
	GND	0	0	0	V	1
Input voltage	$V_{IH}$	2.0	—	$V_{CC} + 0.3$	V	—
	$V_{IL}$	-0.3	—	0.8	V	—

### NOTE:

1. The supply voltage with all  $V_{CC}$  pins must be on the same level. The supply voltage with all GND pins must be on the same level.

## PIN CAPACITANCE ( $T_A = 0$ to $+70^\circ\text{C}$ , $f = 1$ MHz, $V_{CC} = 3.0$ V $\pm$ 0.15 V)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Input capacitance	$A_0 - A_{17}$	$C_{IN1}$	—	8	pF
	UWE, LWE OE, RFSH	$C_{IN2}$	—	8	pF
	CE, CS	$C_{IN3}$	—	8	pF
Input/output capacitance	$I/O_0 - I/O_{15}$	$C_{OUT1}$	—	10	pF

## DC ELECTRICAL CHARACTERISTICS ( $T_A = 0$ to $+70^\circ\text{C}$ , $V_{CC} = 3.0$ V $\pm$ 0.15 V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Operating current in normal operation	$I_{CC1}$	$t_{RC} = t_{RC}(\text{MIN.})$	—	40	mA	1, 2
Standby current	$I_{CC2}$	CE, RFSH = $V_{IH}(\text{MIN.})$	—	1	mA	1
		CE, RFSH = $V_{CC} - 0.2$ V	—	30	mA	1
Self-refresh average current	$I_{CC3}$	CE = $V_{IH}(\text{MIN.})$ RFSH = $V_{IL}(\text{MAX.})$	—	1	mA	1
		CE = $V_{CC} - 0.2$ V, RFSH = 0.2 V	—	70	mA	1
Input leakage current	$I_{LI}$	$0 \text{ V} \leq V_{IN} \leq 6.5 \text{ V}$ 0 V on all other pins	-10	10	$\mu\text{A}$	—
Output leakage current	$I_{LO}$	$0 \text{ V} \leq V_{OUT} \leq V_{CC} + 0.3 \text{ V}$ Input/output pins in High-Z state	-10	10	$\mu\text{A}$	—
Output HIGH voltage	$V_{OH}$	$I_{OUT} = -1 \text{ mA}$	2.4	—	V	—
		$I_{OUT} = -100 \mu\text{A}$	$V_{CC} - 0.2$	—	V	—
Output LOW voltage	$V_{OL}$	$I_{OUT} = 1 \text{ mA}$	—	0.4	V	—
		$I_{OUT} = 100 \mu\text{A}$	—	0.2	V	—
Data retention voltage	$V_R$	—	2.2	3.15	V	—

### NOTES:

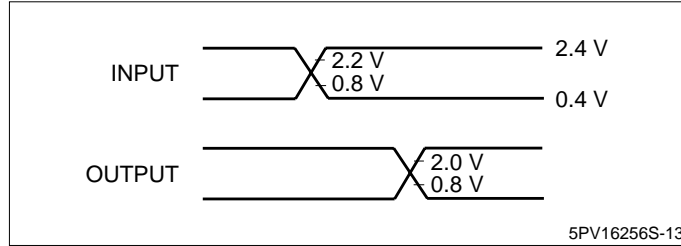
1. The input/output pins are in high impedance state.
2.  $I_{CC1}$  depends on the cycle time.

AC ELECTRICAL CHARACTERISTICS <sup>1,2,7</sup> ( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.0\text{ V} \pm 0.15\text{ V}$ )

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTES
Random read, write cycle time	$t_{RC}$	190	—	ns	—
Random modify write cycle time	$t_{RMW}$	250	—	ns	—
CE pulse width	$t_{CE}$	120	10,000	ns	—
CE precharge time	$t_P$	60	—	ns	—
Address setup time	$t_{AS}$	0	—	ns	3
Row address hold time from CE	$t_{RAH}$	30	—	ns	3
Column address hold time from CE	$t_{CAH}$	120	—	ns	—
CS setup time from $\overline{CE}$	$t_{CSS}$	0	—	ns	—
CS hold time from $\overline{CE}$	$t_{CSH}$	30	—	ns	—
Read command setup time	$t_{RCS}$	0	—	ns	11
Read command hold time	$t_{RCH}$	0	—	ns	9
CE access time	$t_{CEA}$	—	120	ns	4
OE access time	$t_{OEA}$	—	60	ns	4
CE to output in Low-Z	$t_{CLZ}$	20	—	ns	—
OE to output in Low-Z	$t_{OLZ}$	0	—	ns	—
Write disable to output in Low-Z	$t_{WLZ}$	0	—	ns	11
Chip disable to output in High-Z	$t_{CHZ}$	0	30	ns	—
Output disable to output in High-Z	$t_{OHZ}$	0	30	ns	—
WE to output in High-Z	$t_{WHZ}$	0	30	ns	9, 13
Write command pulse width	$t_{WCP}$	35	—	ns	13
Write command setup time	$t_{WCS}$	35	10,000	ns	10, 13
Write command hold time	$t_{WCH}$	120	10,000	ns	12, 13
Data setup time from write disable	$t_{DSW}$	30	—	ns	5, 12, 13
Data setup time from chip disable	$t_{DSC}$	30	—	ns	5
Data hold time from write disable	$t_{DHW}$	0	—	ns	5, 11, 13
Data hold time from chip disable	$t_{DHC}$	30	—	ns	5
Data hold time from column address	$t_{OH}$	0	—	ns	—
Column address hold time from chip disable	$t_{AHC}$	20	—	ns	5
Column address hold time from write disable	$t_{AHW}$	0	—	ns	5, 13
Transition time (rise and fall)	$t_T$	3	50	ns	—
Output disable setup time	$t_{ODS}$	0	—	ns	—
Output disable hold time	$t_{ODH}$	15	—	ns	—
Refresh time interval (2048 cycle)	$t_{REF}$	—	32	ms	6
Auto refresh cycle time	$t_{FC}$	190	—	ns	6
Refresh delay time from CE	$t_{RFD}$	90	—	ns	—
Refresh pulse width (Auto refresh)	$t_{FAP}$	80	1,000	ns	8
Refresh precharge time (Auto refresh)	$t_{FP}$	40	—	ns	—
CE delay time from refresh enable (Auto refresh)	$t_{FCE}$	190	—	ns	—
Refresh pulse width (Self refresh)	$t_{FAS}$	8,000	—	ns	8
CE delay time from refresh precharge (Self refresh)	$t_{FRS}$	600	—	ns	—
$V_{CC}$ recovery time from data retention	$t_R$	5	—	ms	—
Refresh setup hold time	$t_{FS}$	0	—	ns	—
Refresh disable hold time	$t_{RDH}$	15	—	ns	—
Chip disable delay time from RFSH	$t_{RDD}$	15	—	ns	—

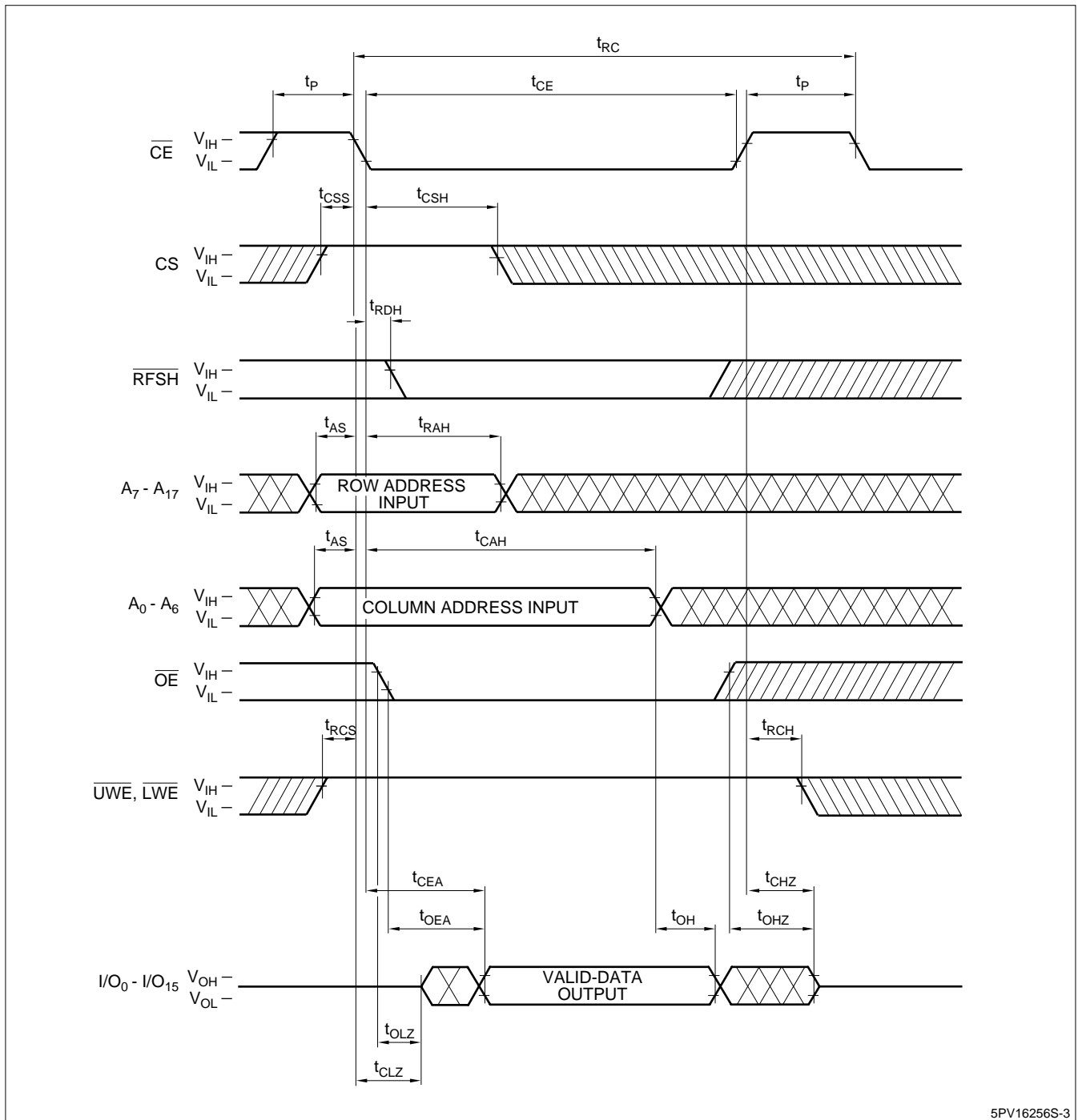
**NOTES:**

1. AC characteristics are measured at  $t_T = 5$  ns.
2. AC characteristics are measured at the following condition:
3. Row address signals are latched in the memory at the falling edge of  $\overline{CE}$ .



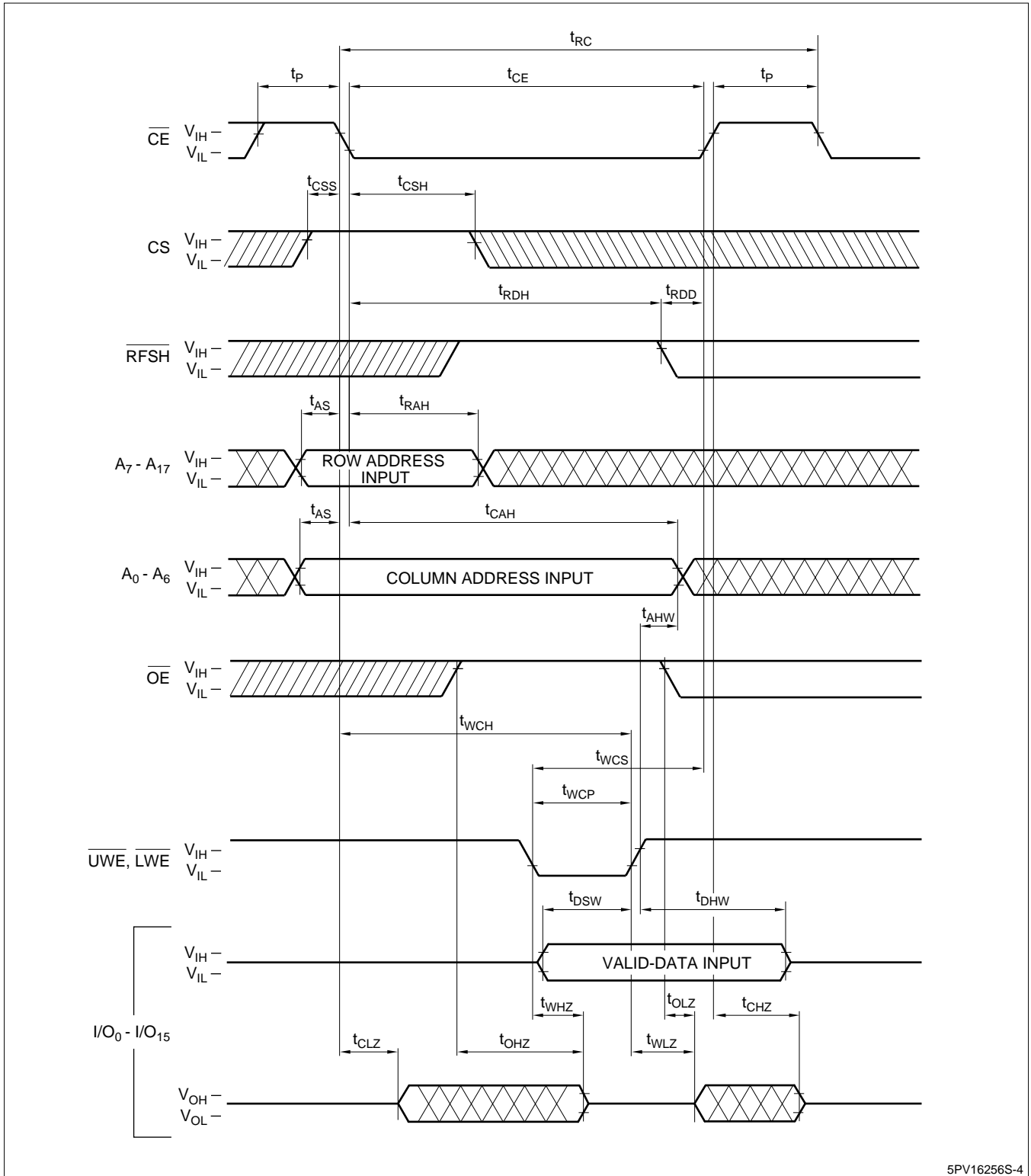
**Figure 3. AC Characteristics**

4. Measured with a load equivalent to 50 pF.
5. Input data is latched in the memory at the earlier rising edge of  $\overline{CE}$  and  $\overline{UWE/LWE}$ . One of ( $t_{AHW}$ ,  $t_{DSW}$ ,  $t_{DHW}$ ) and ( $t_{AHC}$ ,  $t_{DSC}$ ,  $t_{DHC}$ ) needs to be satisfied. The other is "Don't care."
6. Address refresh or auto refresh is needed to be executed 2,048 times within 32 ms.
7. In order to initialize the internal circuits, an initial pause of 500  $\mu$ s with  $\overline{CE} = \overline{RFSH} = V_{IH}$  is required after power-up, and followed by at least 8 dummy cycles. When supply voltage falls down below the recommended supply voltage by temporarily power-down, a waiting time is required at  $V_{CC} = 0$  V for more than 400 ms before power-up, and a pause of 500  $\mu$ s with  $\overline{CE} = \overline{RFSH} = V_{IH}$  and 8 dummy cycles are also necessary after power-up.
8. Auto refresh and self refresh are defined by  $\overline{RFSH}$  pulse width during  $\overline{CE} = V_{IH}$ . If  $\overline{RFSH}$  pulse width is shorter than  $t_{FAP}$  (MAX.), the cycle is an auto refresh cycle and memory cells are refreshed by an internal counter. If  $\overline{RFSH}$  pulse width is longer than  $t_{FAS}$  (MIN.), the cycle is a self refresh cycle and memory cells are refreshed by an internal clock generator automatically.
9.  $t_{RCH}$  and  $t_{WHZ}$  are determined by the earlier falling edge of  $\overline{UWE}$  and  $\overline{LWE}$ .
10.  $t_{WCS}$  is determined by the later falling edge of  $\overline{UWE}$  and  $\overline{LWE}$ .
11.  $t_{RCS}$ ,  $t_{WLZ}$ , and  $t_{DHW}$  are determined by the later rising edge of  $\overline{UWE}$  and  $\overline{LWE}$ .
12.  $t_{WCH}$  and  $t_{DSW}$  are determined by the earlier rising edge of  $\overline{UWE}$  and  $\overline{LWE}$ .
13.  $t_{WHZ}$ ,  $t_{WCP}$ ,  $t_{WCS}$ ,  $t_{WCH}$ ,  $t_{DSW}$ ,  $t_{DHW}$ ,  $t_{WLZ}$ , and  $t_{AHW}$  should be satisfied by both  $\overline{UWE}$  and  $\overline{LWE}$ .
14. The transition time of the supply voltage in data retention mode is less than 0.05 V/ms.
15. The width of data retention period is more than  $t_{FAS}$  (MIN.) like self-refresh cycle.
16. All input pins are required to be higher than -0.3 V.
17.  $\overline{RFSH}$  must be lower than 0.2 V during the data retention period.
18.  $\overline{CE}$  and  $\overline{CS}$  must be higher than  $V_{CC} - 0.2$  V during the data retention period.



5PV16256S-3

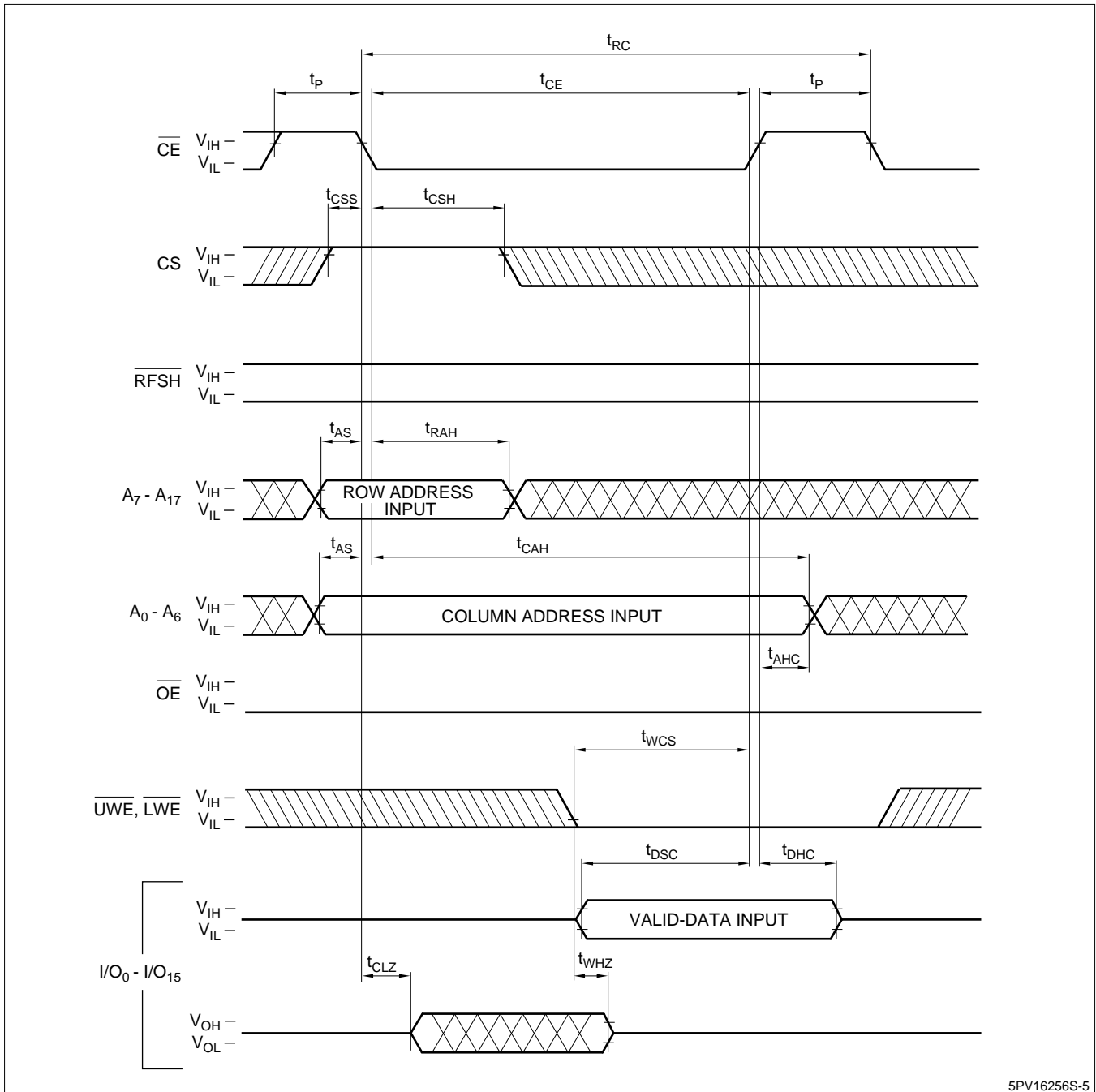
Figure 4. Read Cycle



5PV16256S-4

Figure 5. Write Cycle (1)  
(OE Clock)





**Figure 6. Write Cycle (2)**  
**(OE = Low , CE Control)**



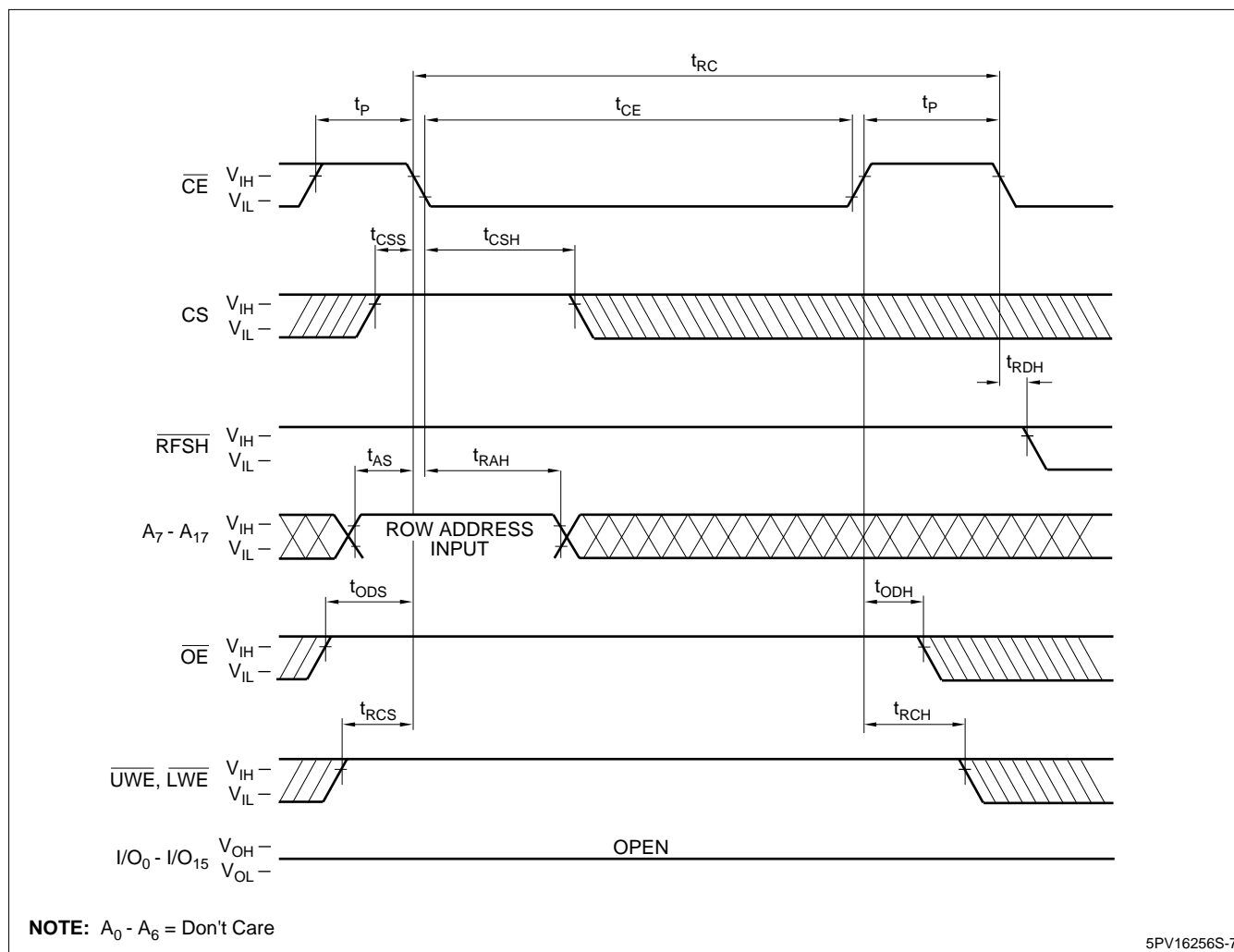


Figure 8. Address Refresh Cycle

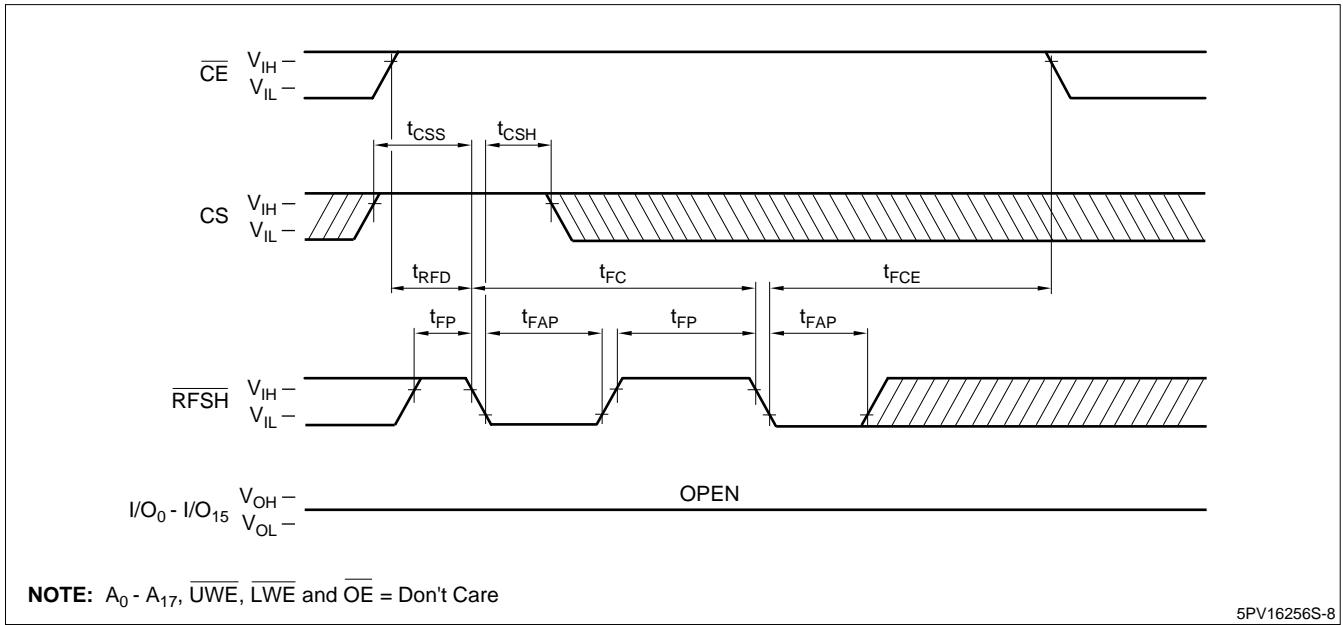


Figure 9. Auto Refresh Cycle

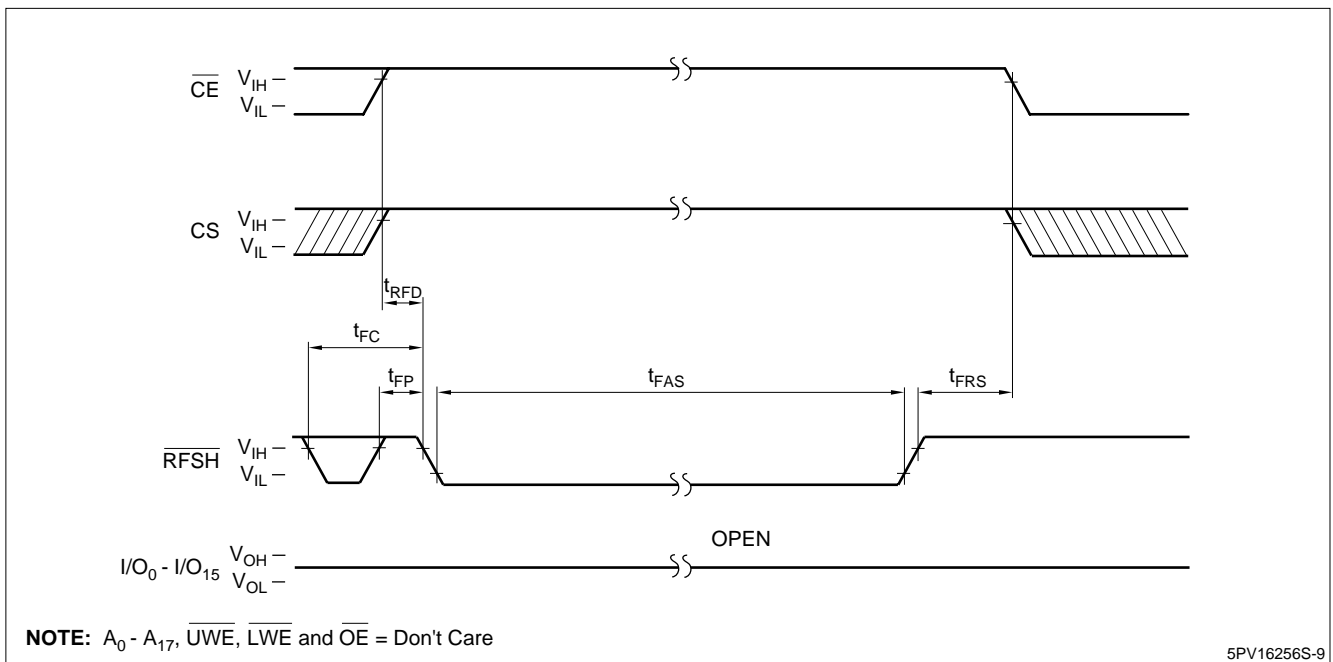


Figure 10. Self Refresh Cycle

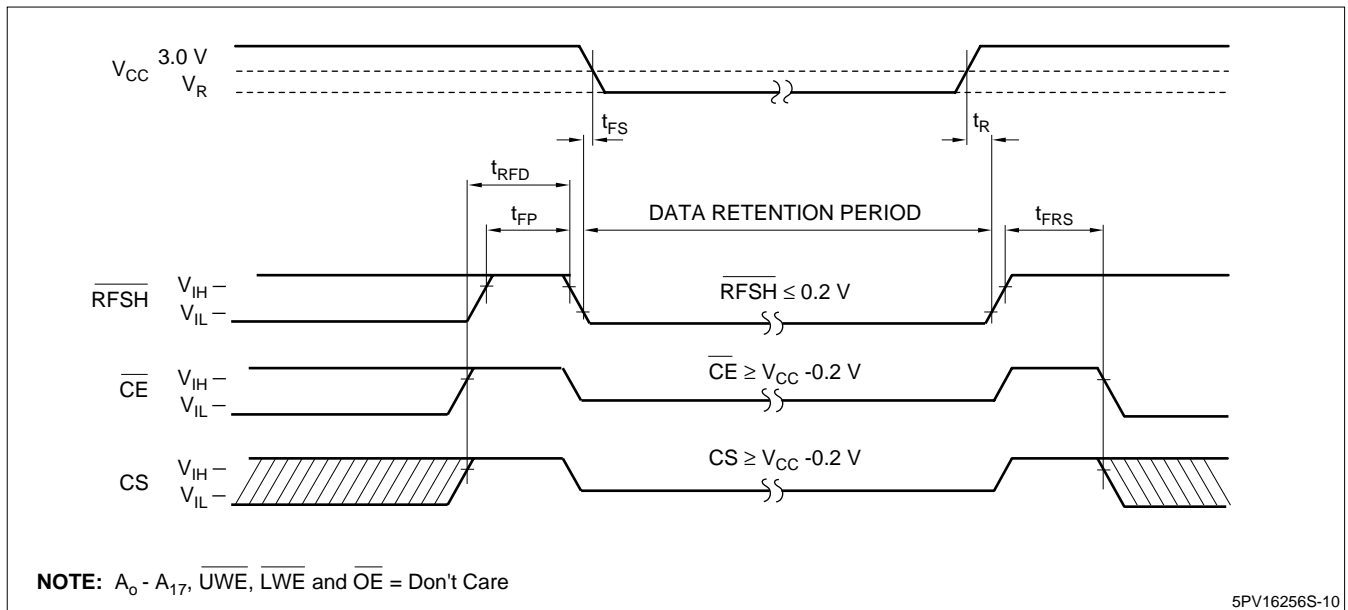


Figure 11. Data Retention Mode

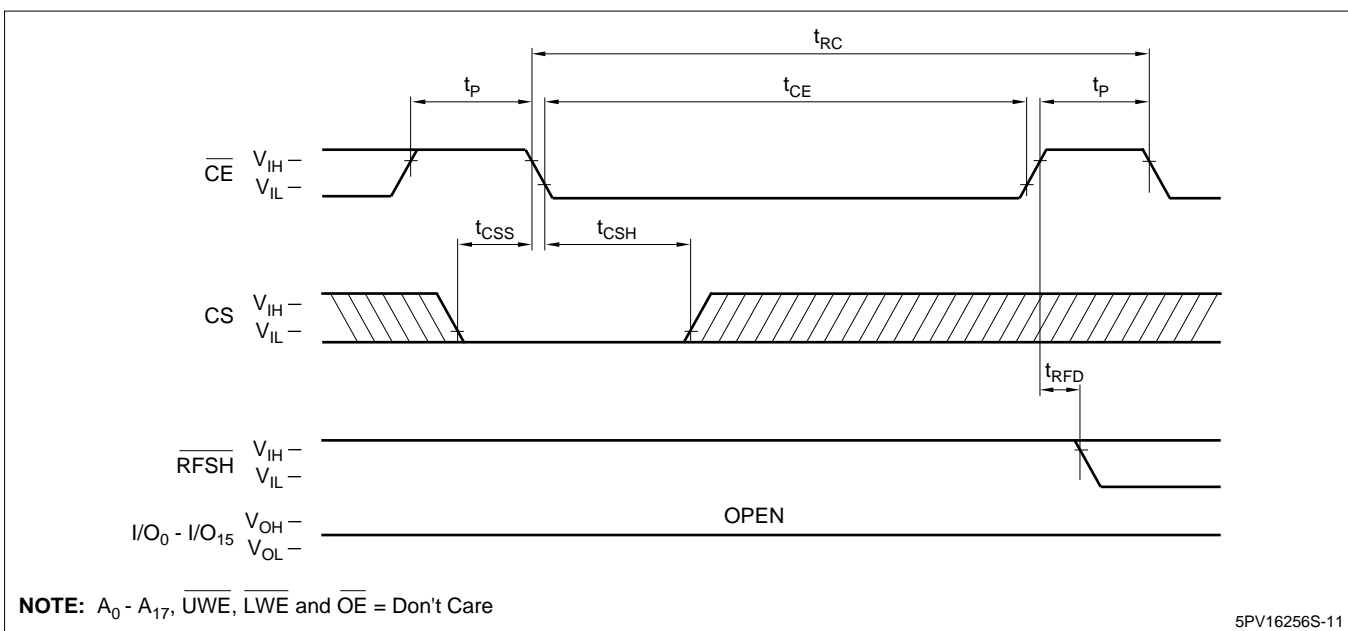
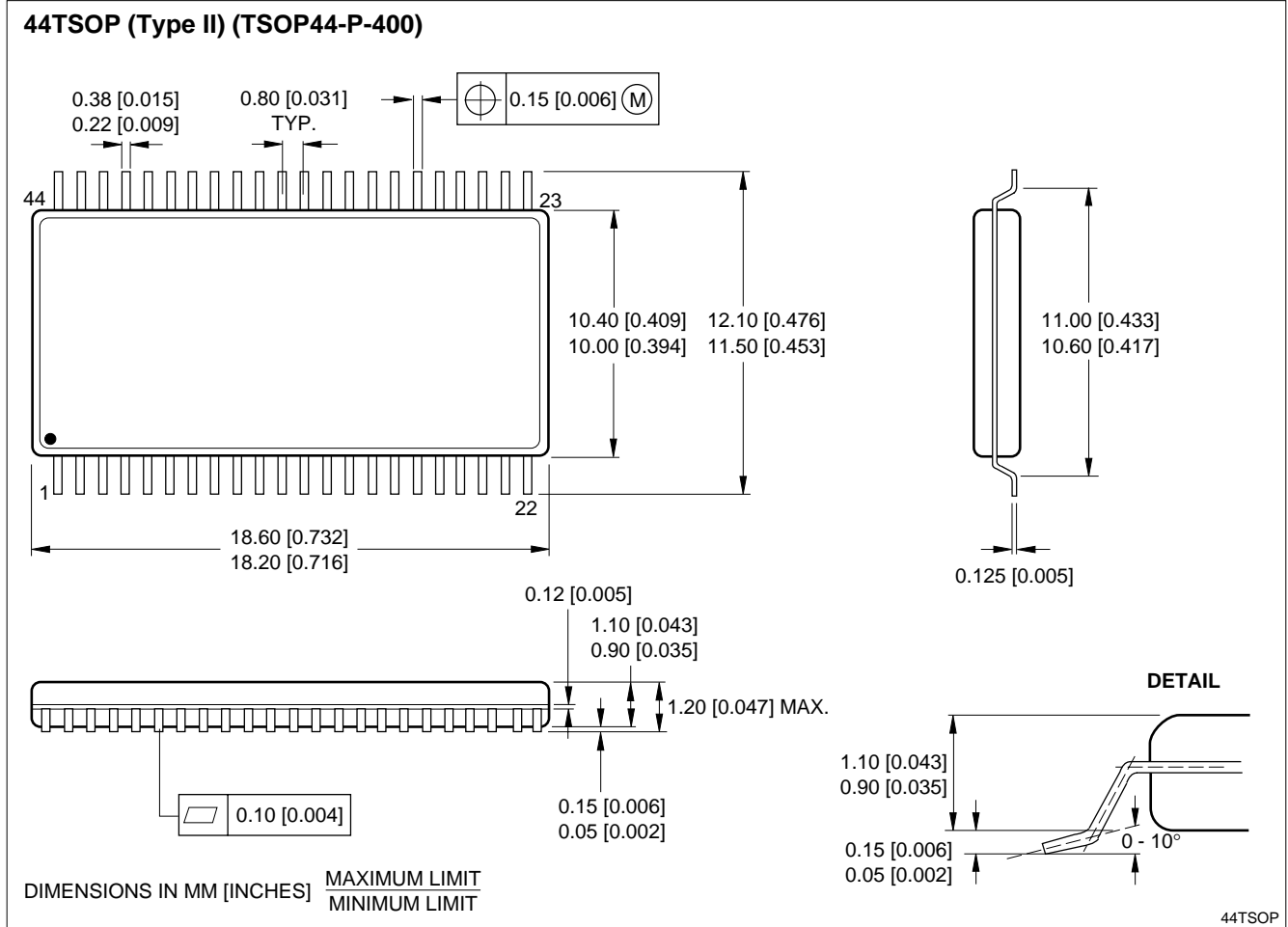


Figure 12. CS Standby Mode

**PACKAGE DIAGRAM**



**ORDERING INFORMATION**

