SONY

CXD2309Q

10-bit 85MSPS 3-Channel D/A Converter

Description

The CXD2309Q is a 10-bit high-speed D/A converter for video band, featuring RGB 3-channel input/output. This is ideal for use in high-definition TVs and high-resolution displays.

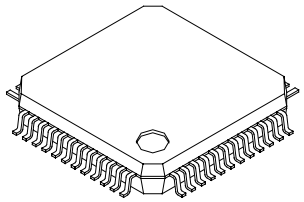
Features

- Resolution 10-bit
- Maximum conversion speed 85MSPS
- RGB 3-channel input/output
- Differential linearity error ±0.5 LSB
- Low power consumption 275 mW
  (200 Ω load for 2 Vp-p output)
- Single +5 V power supply
- Low glitch
- 48-pin QFP package

Structure

Silicon gate CMOS IC

48 pin QFP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

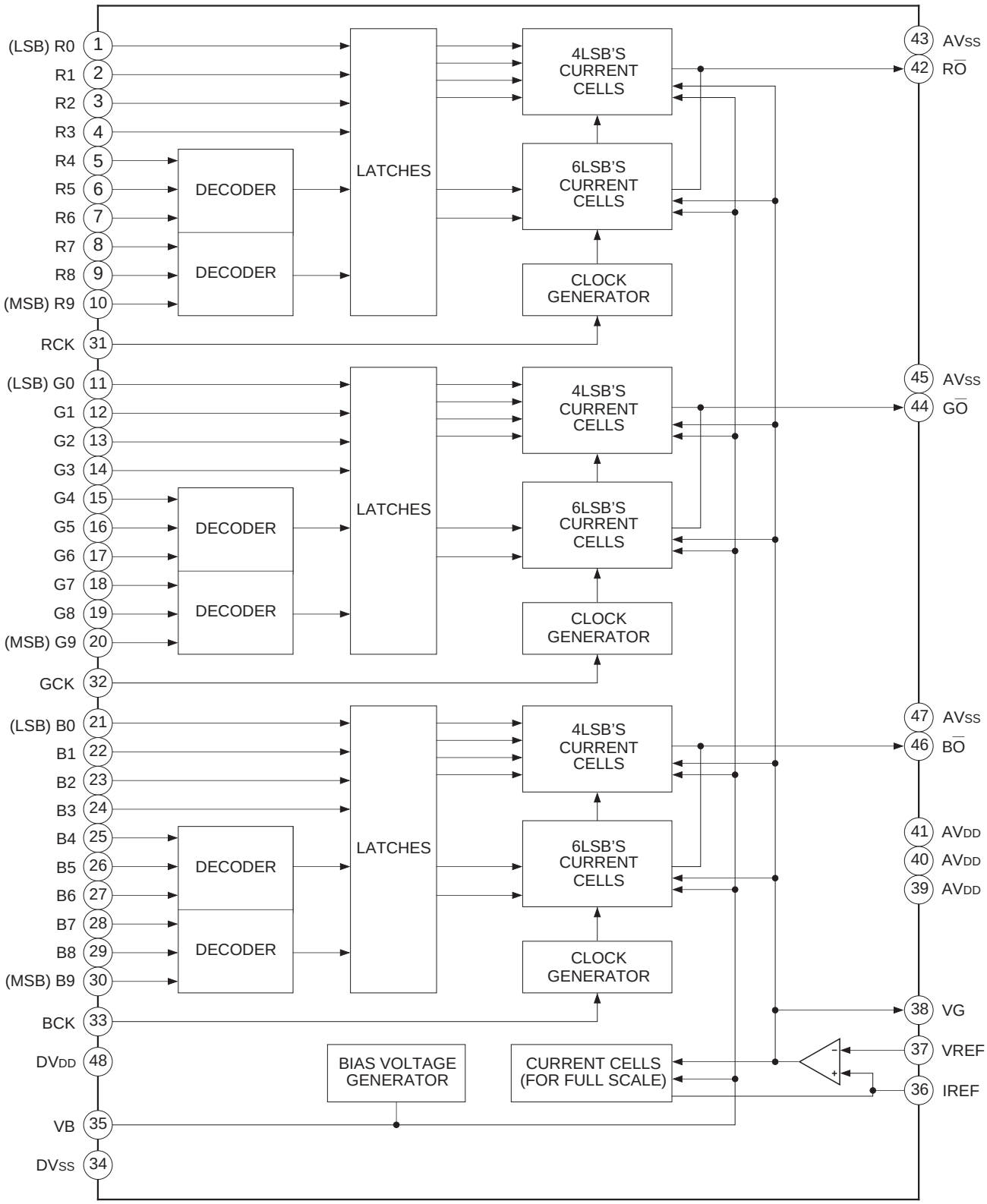
• Supply voltage	AV_{DD}, DV_{DD}	7	V
• Input voltage (All pins)	V_{IN}	V_{DD}+0.5 to V_{SS}–0.5	V
• Output current	I_{OUT}	0 to 15	mA
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

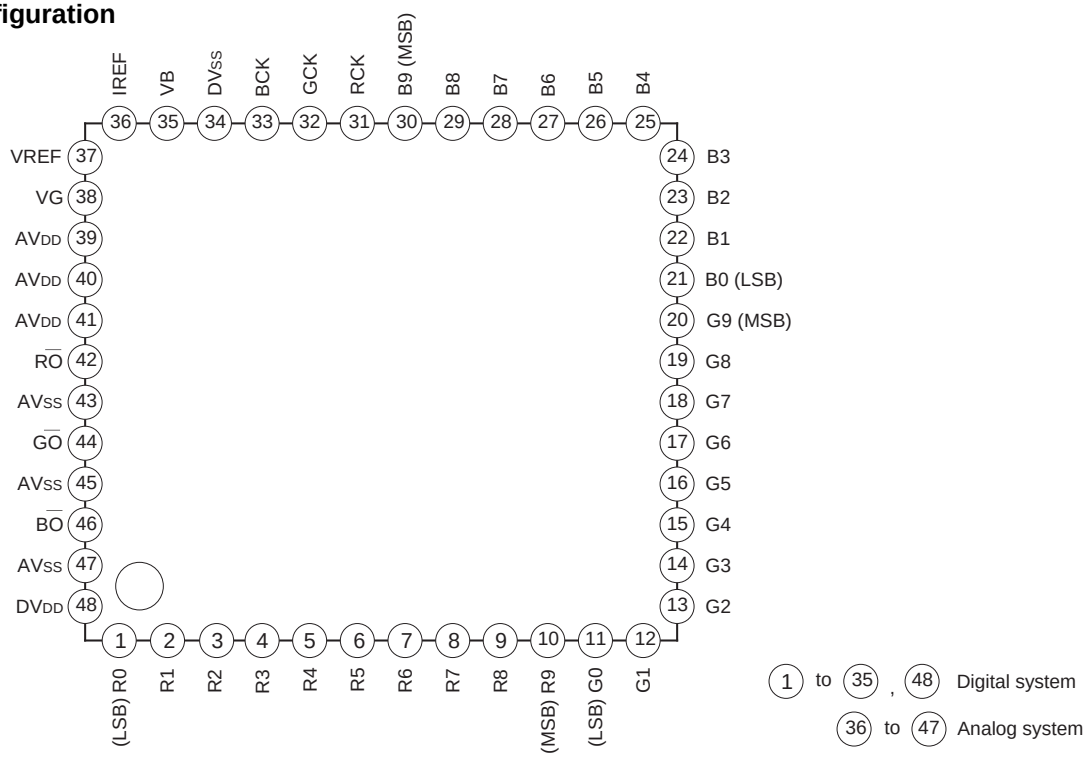
• Supply voltage	AV_{DD}, AV_{SS}	4.75 to 5.25	V
	DV_{DD}, DV_{SS}	4.75 to 5.25	V
• Reference input voltage	V_{REF}	0.5 to 2.0	V
• Clock pulse width	$T_{PW}1$, $T_{PW}0$	9 (min.)	ns
• Operating temperature	Topr	–20 to +85	°C

E94341B01

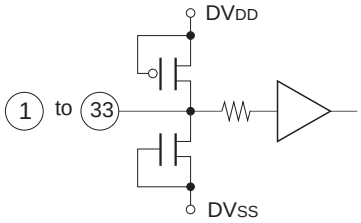
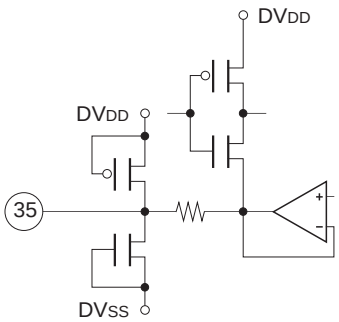
Block Diagram

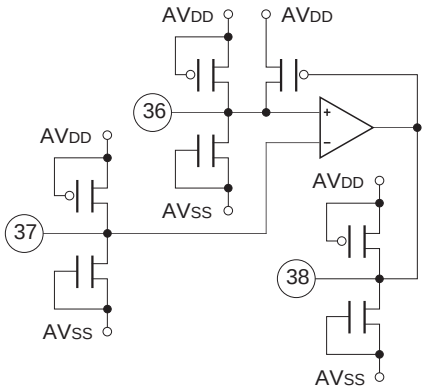
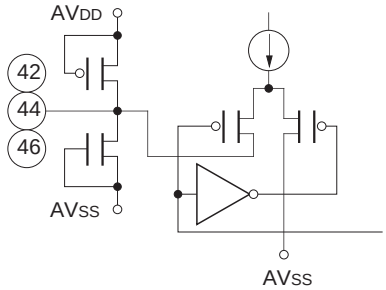


Pin Configuration



Pin Description and Equivalent Circuit

Pin No.	Symbol	I/$\overline{O}$	Equivalent circuit	Description
1 to 10	R0 to R9	I		Digital input. 1 pin R0 (LSB) to 10 pin R9 (MSB) 11 pin G0 (LSB) to 20 pin G9 (MSB) 21 pin B0 (LSB) to 30 pin B9 (MSB)
11 to 20	G0 to G9			
21 to 30	B0 to B9			
31	RCLK			Clock input.
32	GCLK			
33	BCLK			
34	DVSS	—		Digital ground.
35	VB	$\overline{O}$		Connect an approximately 0.1µF capacitor.

Pin No.	Symbol	I/$\overline{O}$	Equivalent circuit	Description
36	IREF	$\overline{O}$		Reference current output. Connect an "RIR" resistor which are 16 times the output resistance "ROUT".
37	VREF	I		Reference voltage input. Sets an output full-scale value.
38	VG	$\overline{O}$		Connect an approximately 0.1µF capacitor.
39 to 41	AVDD	—		Analog power supply.
42	R$\overline{O}$	$\overline{O}$		Current output. Output can be obtained by connecting a resistor (200 Ω typ.).
44	G$\overline{O}$			
46	B$\overline{O}$			
43, 45, 47	AVSS	—		Analog ground.
48	DVDD	—		Digital power supply.

Electrical Characteristics (f_{CLK}=85 MHz, AV_{DD}=DV_{DD}=5 V, R_{OUT}=200 Ω, V_{REF}=2.0 V, R_{IR}=3.3 kΩ, Ta=25°C)

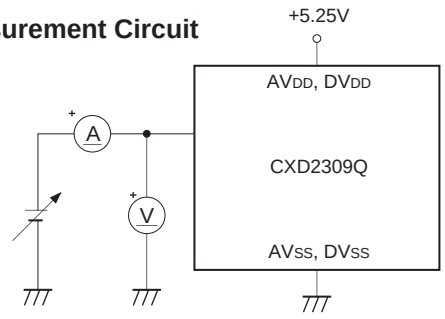
Item	Symbol	Measurement conditions		Min.	Typ.	Max.	Unit
Resolution	n				10		bit
Conversion speed	f_{CLK}	AV_{DD}=DV_{DD}=4.75 to 5.25 V Ta=–20 to +85 °C		0		85	MSPS
Integral non-linearity error	E_L	Endpoint		–2.0		2.0	LSB
Differential non-linearity error	E_D			–0.5		0.5	LSB
Precision guaranteed output voltage range	V_{OC}			1.8	1.92	2.0	V
Output full-scale voltage	V_{FS}			1.8	1.92	2.0	V
Output full-scale ratio *1	F_{SR}			0		3	%
Output full-scale current	I_{FS}			9.0	9.6	10	mA
Output offset voltage	V_{OS}	When “0000000000” data input				1	mV
Glitch energy	GE	R_{OUT}=100 Ω, 1 Vp-p output			50		pV•s
Crosstalk	CT	When 10 MHz sin wave input	F_{CLK}=50 MHz	40	42		dB
			F_{CLK}=85 MHz		40		
SN ratio	SNR	When 1 MHz sin wave input	F_{CLK}=50 MHz	50	55		dB
			F_{CLK}=85 MHz		50		
Supply current	I_{DD}	When 10 MHz sin wave output	F_{CLK}=50 MHz		48	58	mA
			F_{CLK}=85 MHz		55		
Analog input resistance	R_{IN}	VREF		1			MΩ
Input capacitance	C_I					9	pF
Output capacitance	C_O				125		pF
Digital input voltage	V_{IH}	AV_{DD}=DV_{DD}=4.75 to 5.25 V Ta=–20 to +75 °C		2.15			V
	V_{IL}					0.85	
Digital input current	I_{IH}	AV_{DD}=DV_{DD}=4.75 to 5.25 V Ta=–20 to +75 °C		–5		5	µA
	I_{IL}						
Setup time	ts			4			ns
Hold time	th			1			ns
Propagation delay time	t_{PD}				14		ns
Rise time	tr				26.5		ns
Fall time	tf				26.0		ns

*1 Full-scale output ratio = $\left| \frac{\text{Full-scale voltage of channel}}{\text{Average of the full-scale voltage of the channels}} - 1 \right| \times 100$ (%)

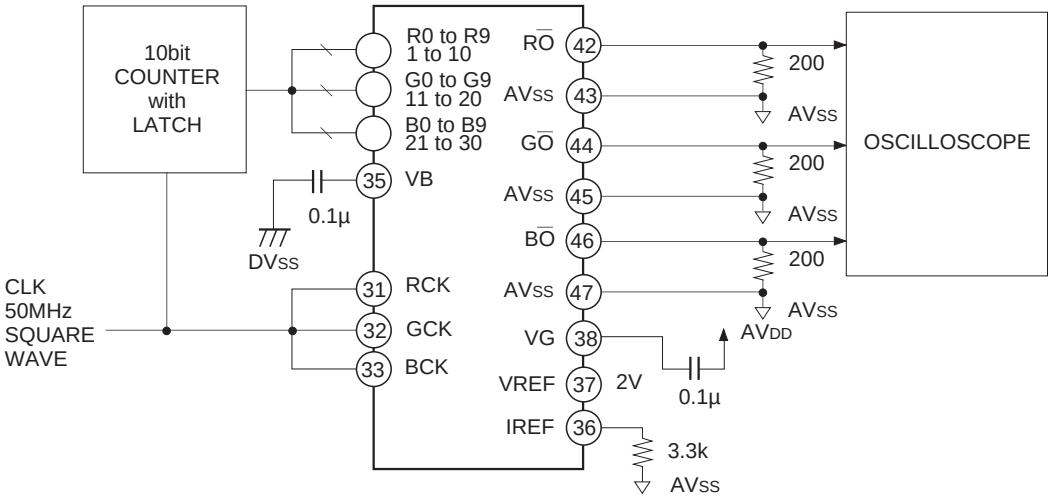
Electrical Characteristics Measurement Circuit

Analog Input Resistance
Digital Input Current

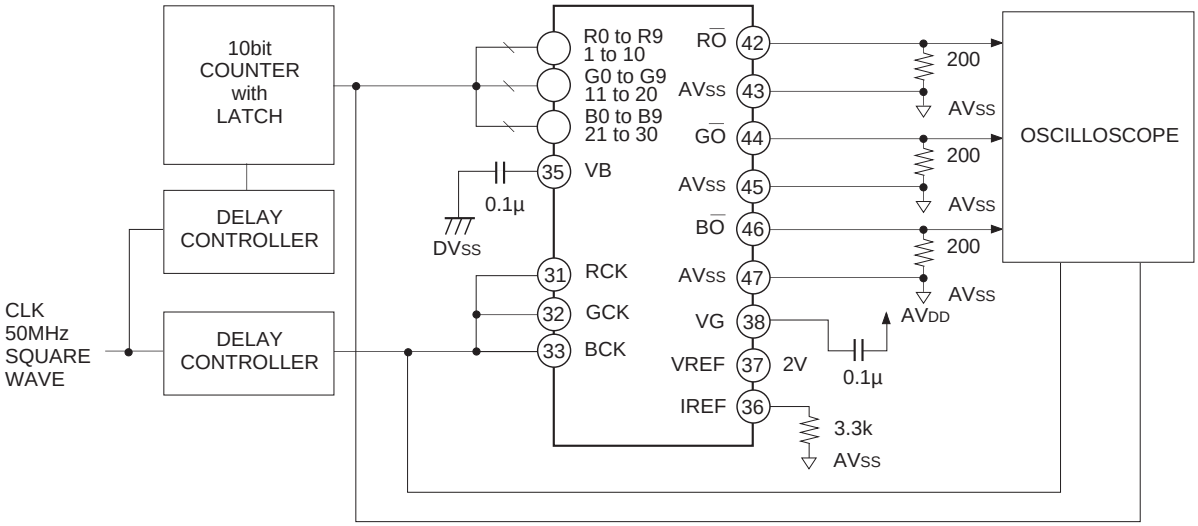
Measurement Circuit



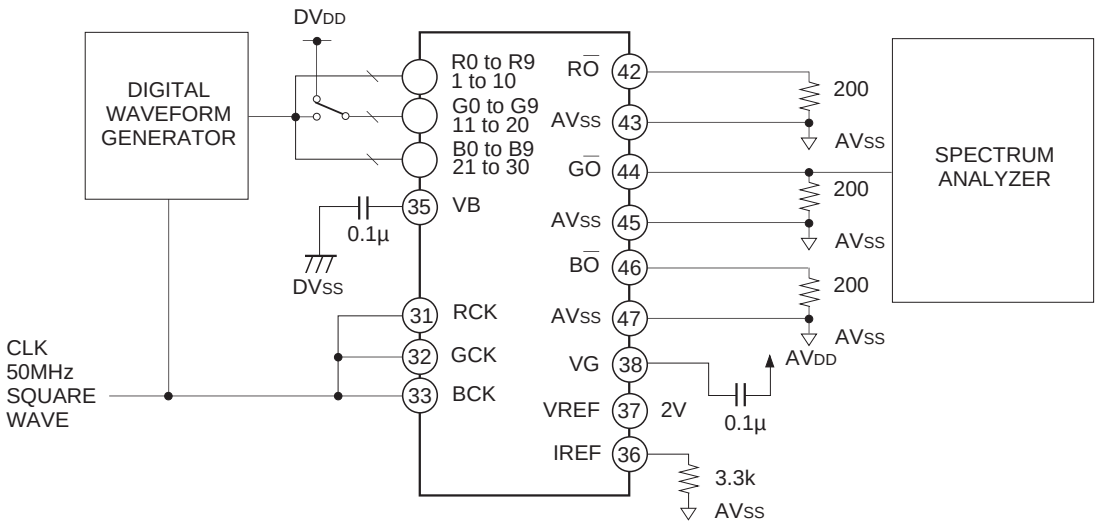
Conversion Rate Measurement Circuit



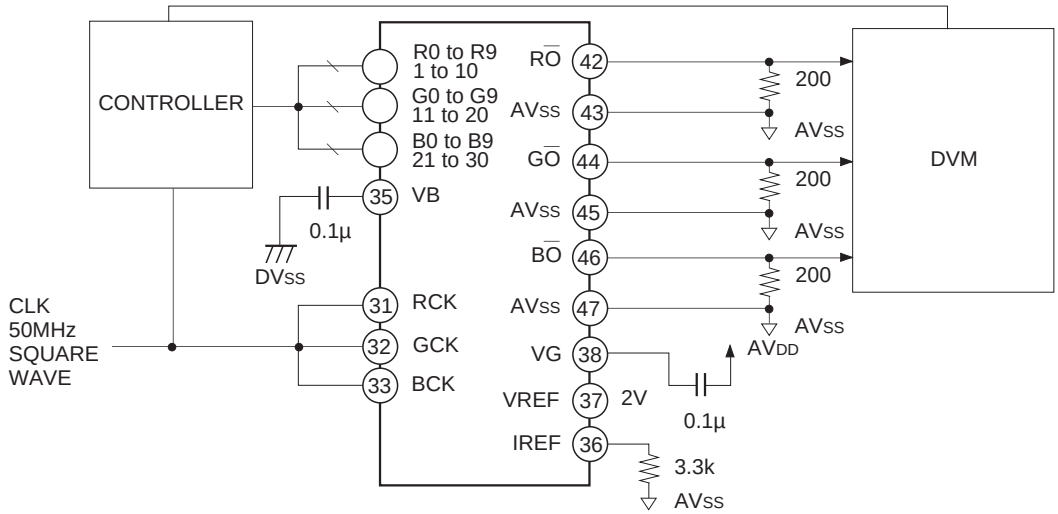
Setup Time
Hold Time } **Measurement Circuit**
Glitch Energy



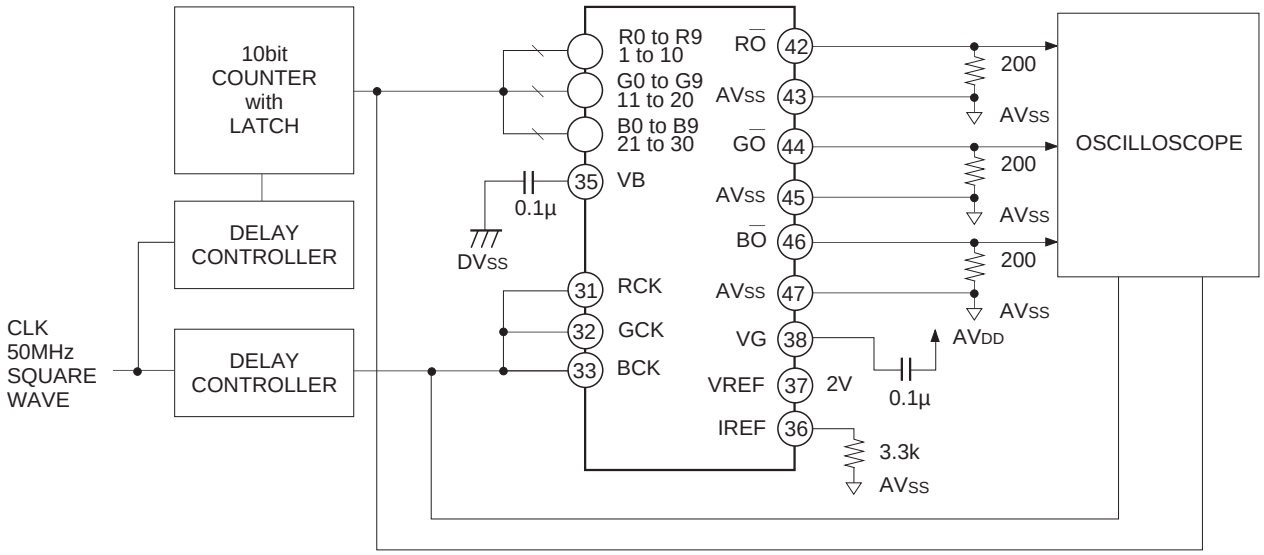
Crosstalk Measurement Circuit



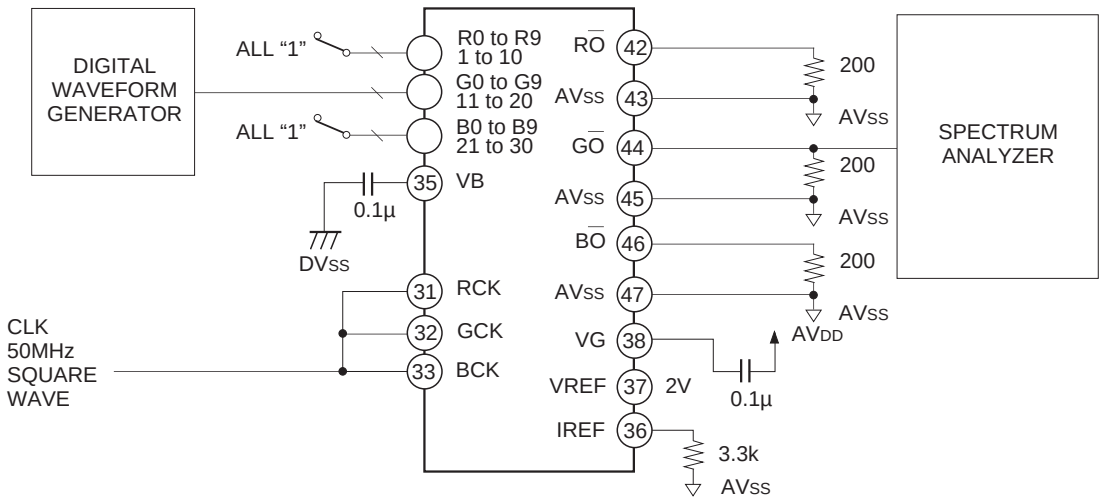
DC Characteristics Measurement Circuit



Propagation Delay Time Measurement Circuit

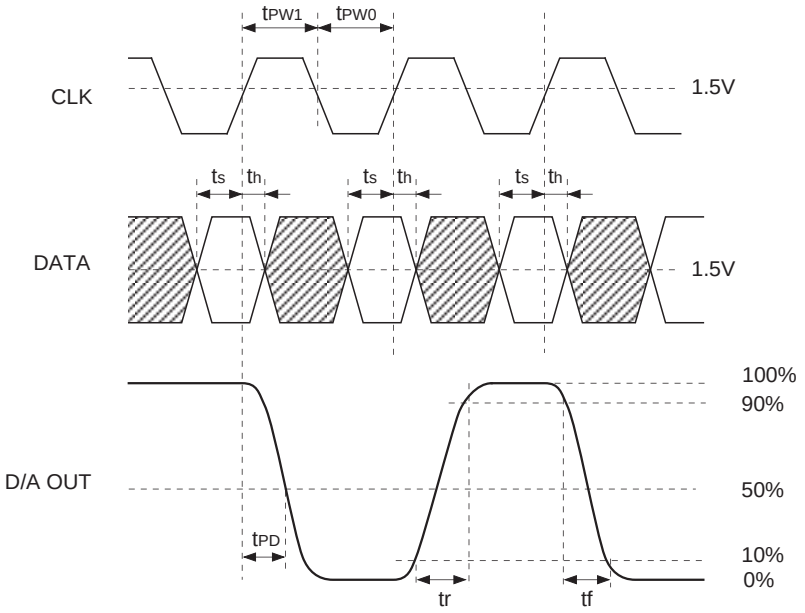


SNR Measurement Circuit



Description of Operation

Timing Chart



I/O Correspondence Table (output full-scale voltage: 2.00 V)

Input code	Output voltage
MSB LSB	
1 1 1 1 1 1 1 1 1 1	2.0 V
:	
1 0 0 0 0 0 0 0 0 0	1.0 V
:	
0 0 0 0 0 0 0 0 0 0	0 V

Notes on Operation

- Selecting the Output Resistance

  CXD2309Q is a current output type D/A converter. The output voltage can be obtained by connecting the resistor R_{OUT} to the current output pins $R\overline{O}$, $G\overline{O}$ and $B\overline{O}$.

  Specifications: Output full-scale voltage V_{FS} = 1.8 to 2.0 [V]

  Output full-scale current I_{FS} = 9.0 to 10.0 [mA]

  Calculate the output resistance from $V_{FS} = I_{FS} \times R_{OUT}$. Connect a resistance sixteen times the output resistance to the reference current output pin IREF. In some cases, as this value may not exist, a similar value can be used instead.

  Note that the V_{FS} will be the following.

  $$V_{FS} = V_{REF} \times 16R_{OUT}/R_{IR}$$

  V_{REF} is the voltage set at the reference voltage input pin VREF, R_{OUT} is the resistor to be connected to the current output pins $R\overline{O}$, $G\overline{O}$, $B\overline{O}$ and R_{IR} is the resistor to be connected to the IREF. Power consumption can be reduced by increasing the resistance, but this will on the contrary increase the glitch energy and data setting time. Set the best values according to the purpose of use.

- Correlation between Data and Clock

  For CXD2309Q to display the desired performance as a D/A converter, the data transmitted from outside and the clock must be synchronized properly. Adjust the setup time (ts) and hold time (th) as specified in “Electrical Characteristics”.

- Power supply, ground

  Separate the analog and digital signals around the device to reduce noise effects. Bypass the power supply pin to each ground with a 0.1 µF ceramics capacitor as near as possible to the pin for both the digital and analog signals.

- Latch up

  Analog and digital power supplies must be able to share the same power supply of the board. This is to prevent latch up caused by potential difference between the two pins when the power is turned on.

- IREF

  The I_{REF} pin is very sensitive to improve the AC characteristics. Pay attention for capacitance component not to attach to this pin because its output may become unstable.

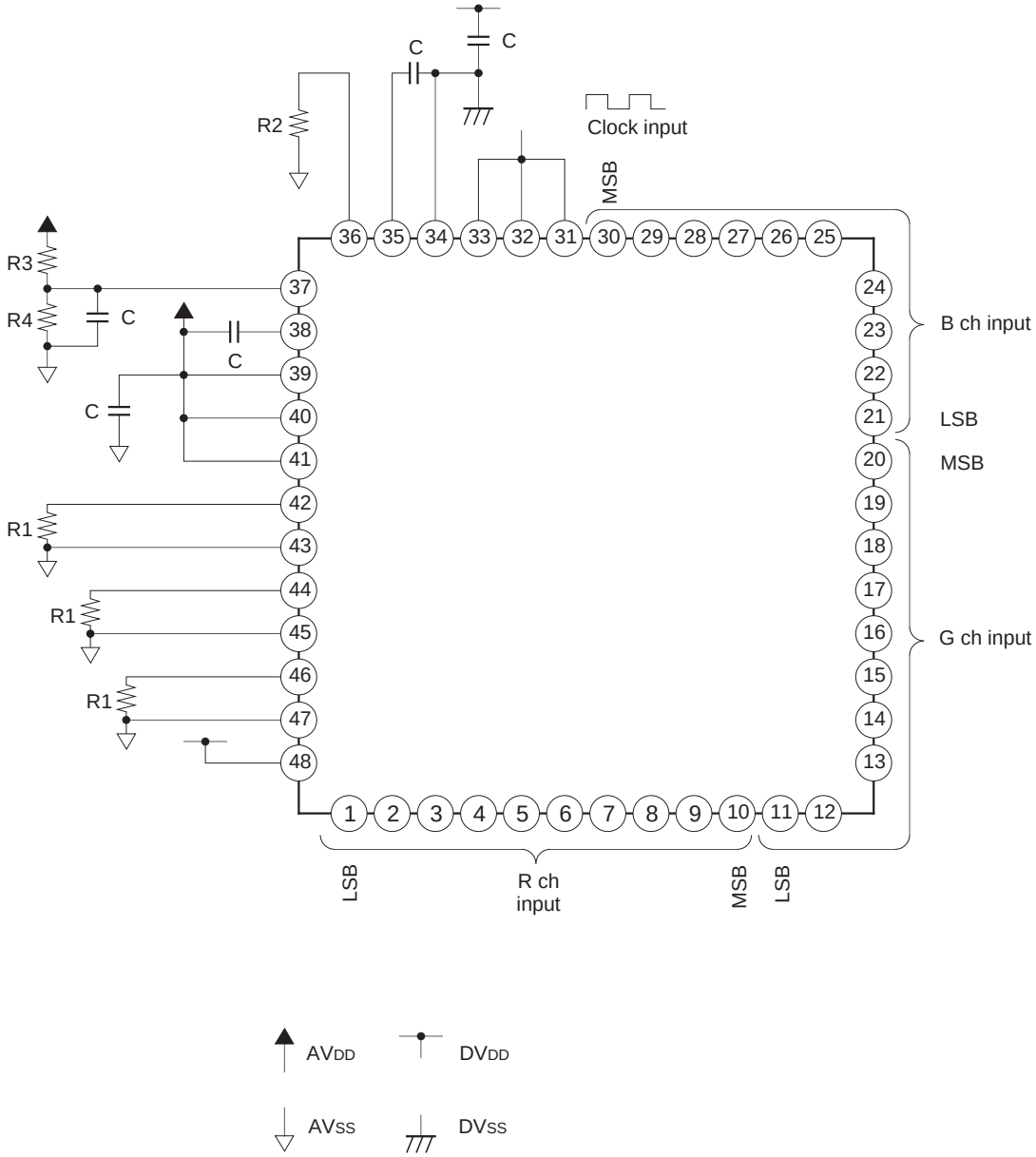
- VG pin

  It is recommended to use a 1 µF capacitor to improve the AC characteristics though the typical capacitance value externally connected to the VG pin is 0.1 µF.

- Output full-scale voltage

  For the applications using the RGB signal, the color balance may be broken up when the $R\overline{O}$, $G\overline{O}$ and $B\overline{O}$ output full-scale voltages are used with not adjustment.

Application Circuit



- When the power supply (AV_{DD} and DV_{DD}) is 5.0 V.
- R1=200 Ω
- R2=3.3 kΩ
- R3=3.0 kΩ
- R4=2.0 kΩ
- C=0.1 µF

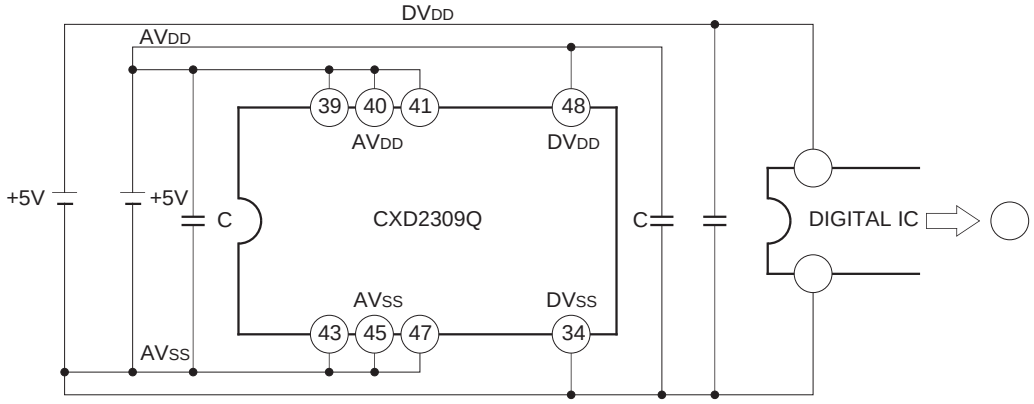
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Latch Up Prevention

The CX2309Q is a CMOS IC which requires latch up precautions. Latch up is mainly generated by the lag in the voltage rising time of AV_{DD} (Pin 39, 40 and 41) and DV_{DD} (Pin 48), when power supply is ON.

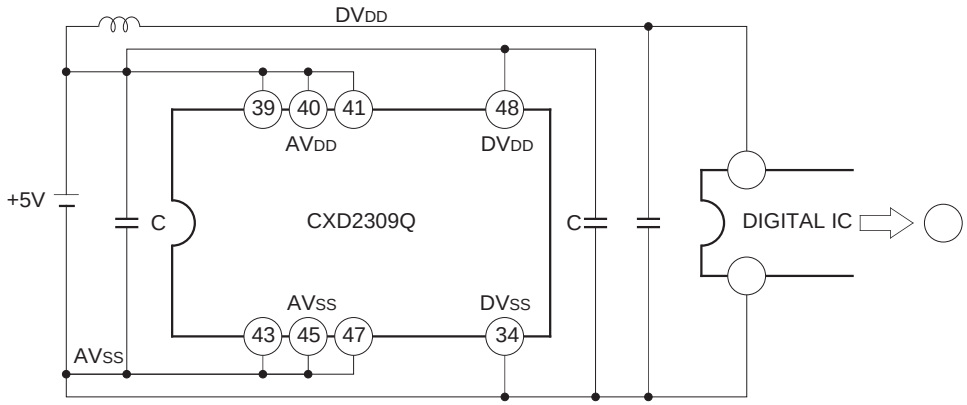
1. Correct usage

a. When analog and digital supplies are from different sources

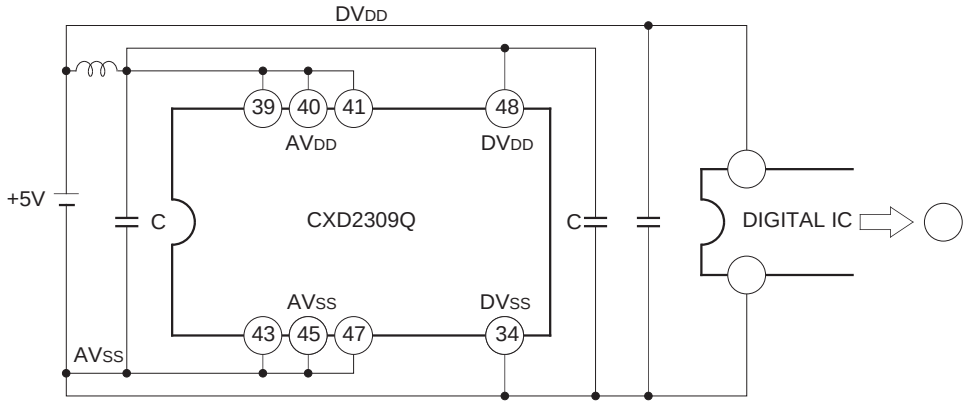


b. When analog and digital supplies are from a common source

(i)

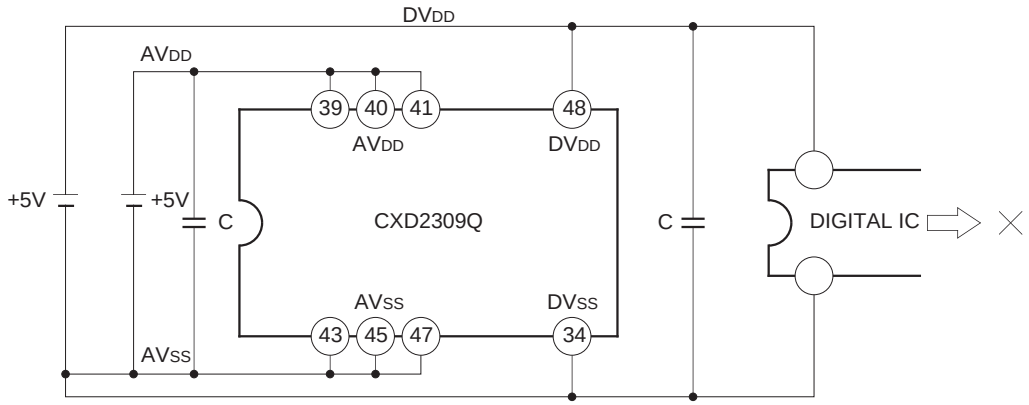


(ii)



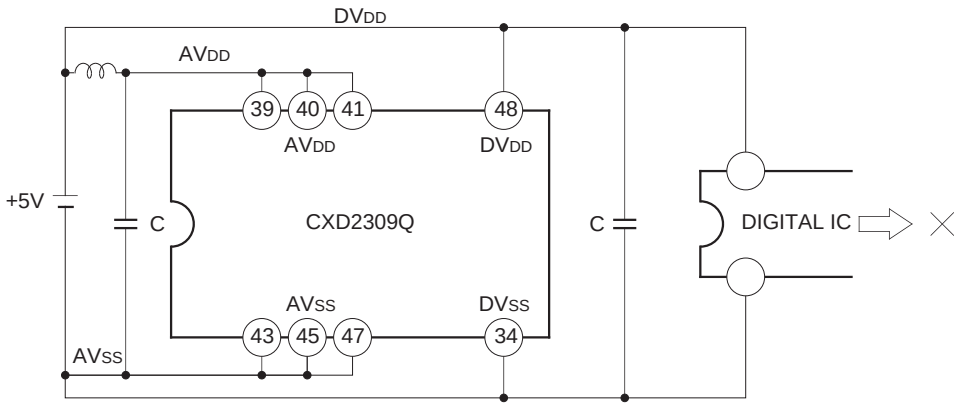
2. Example when latch up easily occurs

a. When analog and digital supplies are from different sources

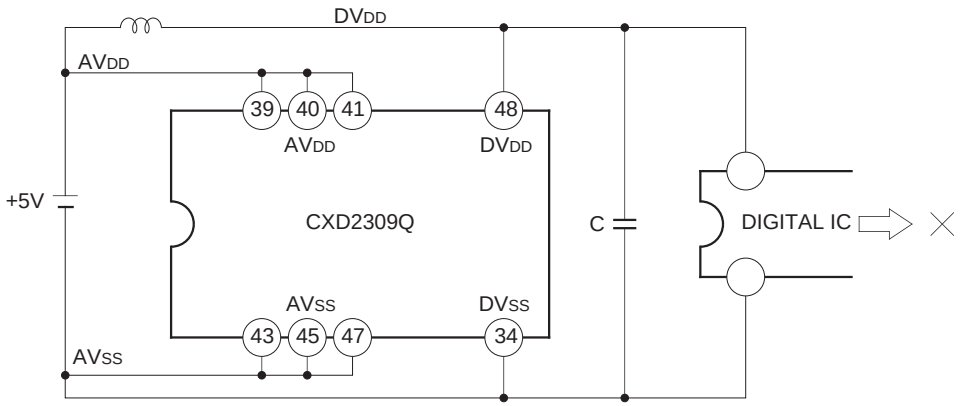


b. When analog and digital supplies are from common source

(i)



(ii)



Example of Representative Characteristics

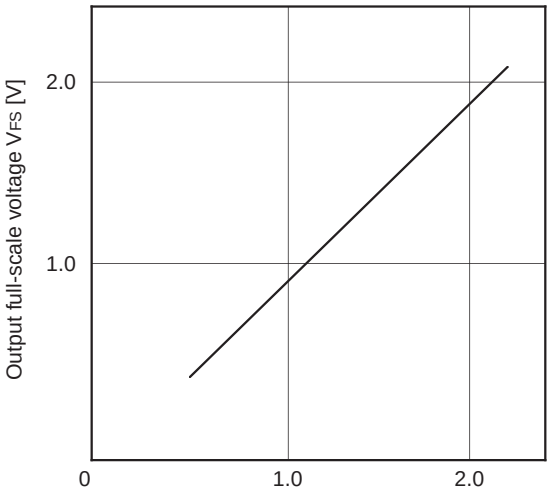


Fig. 1. Reference voltage vs. Output full-scale voltage

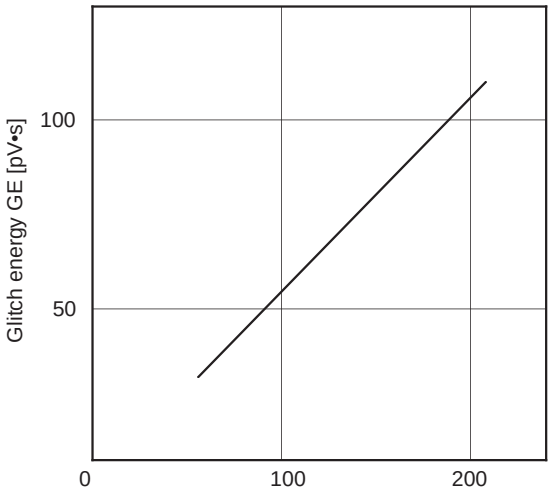


Fig. 2. Output resistance vs. Glitch energy

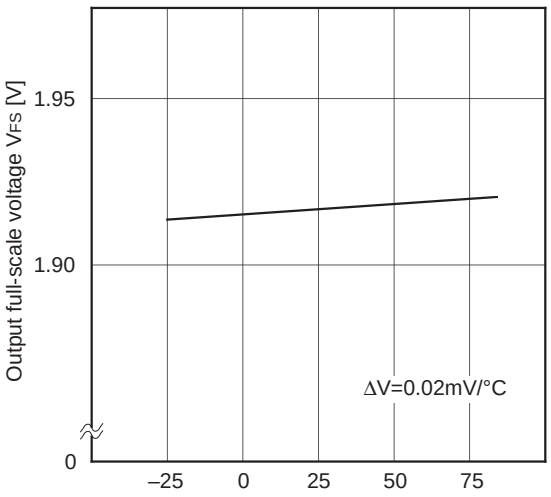


Fig. 3. Ambient temperature vs. Output full-scale voltage

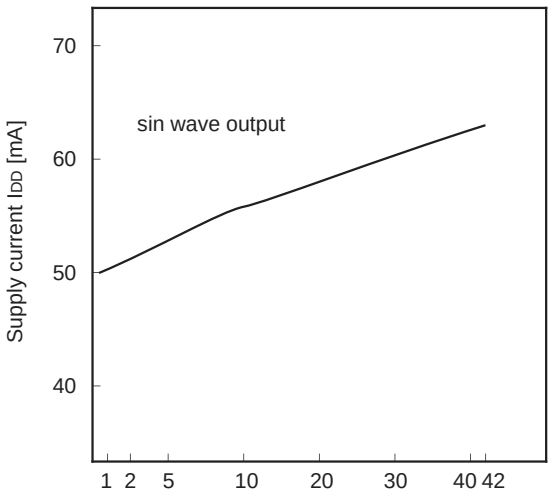


Fig. 4. Output frequency vs. Supply current

Standard Measurement Conditions

- $AV_{DD}=DV_{DD}=5.0$ V
- $V_{REF}=2.0$ V
- $F_{CLK}=85$ MHZ
- $R_{OUT}=200\ \Omega$
- $R_{IR}=3.3$ kΩ
- Ta=25 °C

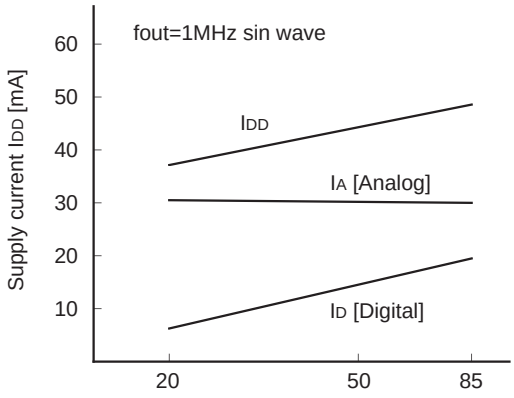


Fig. 5. Clock frequency vs. Supply current

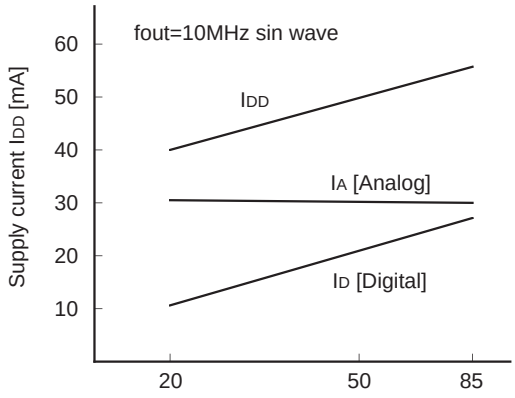


Fig. 6. Clock frequency vs. Supply current

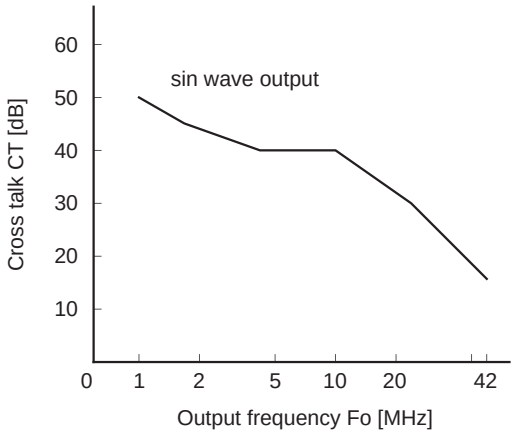


Fig. 7. Output frequency vs. Cross talk

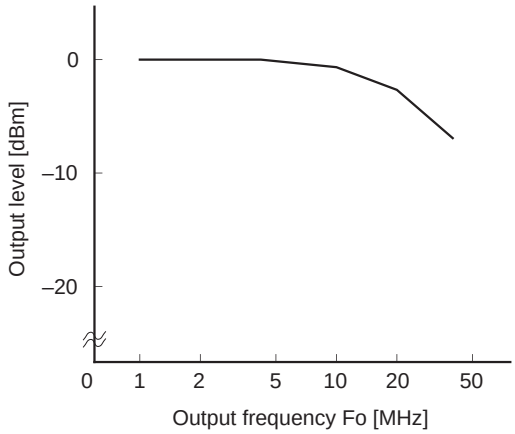


Fig. 8. Output frequency vs. Output level
(Including primary hold characteristics sinx/x)

Standard Measurement Conditions

- $AV_{DD}=DV_{DD}=5.0$ V
- $V_{REF}=2.0$ V
- $F_{CLK}=85$ MHZ
- $R_{OUT}=200\ \Omega$
- $R_{IR}=3.3\ k\Omega$
- Ta=25 °C

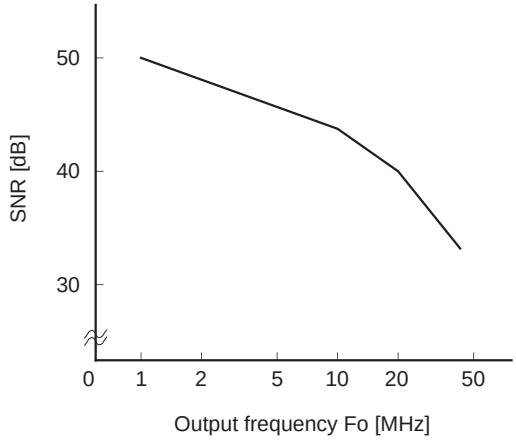


Fig. 9. Output frequency vs. SNR

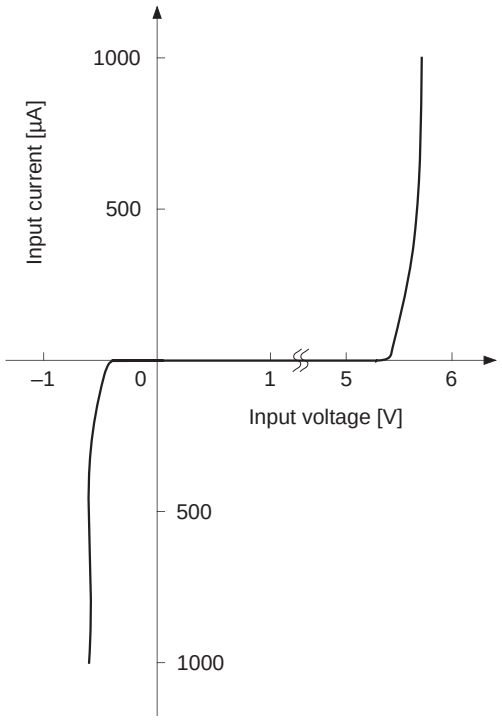


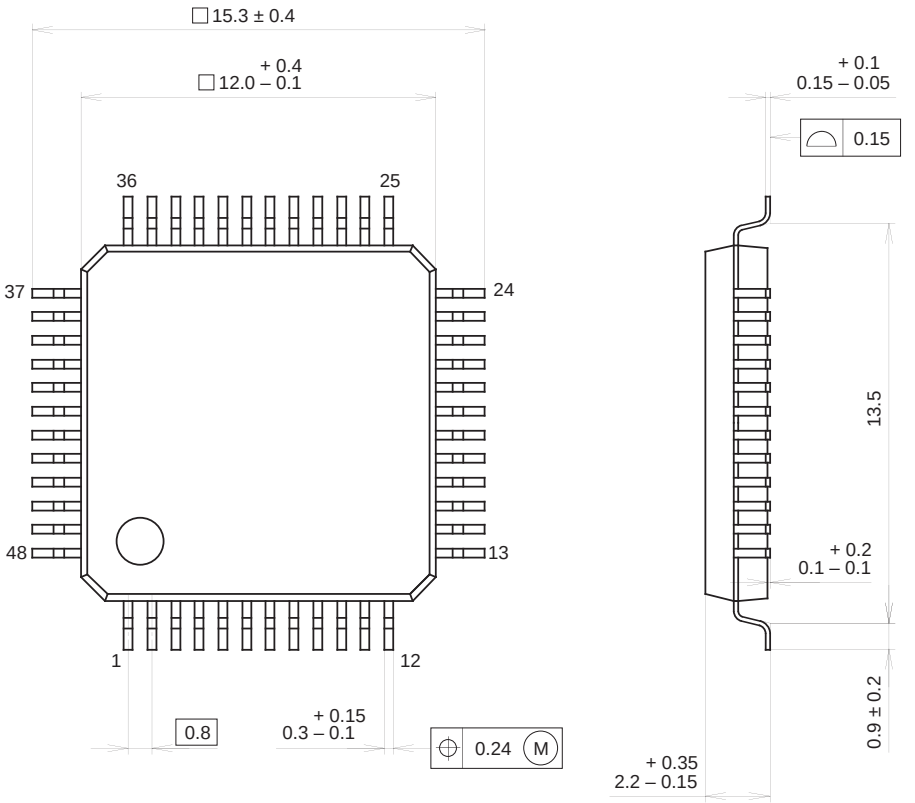
Fig. 10. Input terminal V-I characteristics

Standard Measurement Conditions

- AV_{DD}=DV_{DD}=5.0 V
- V_{REF}=2.0 V
- F_{CLK}=85 MHZ
- R_{OUT}=200 Ω
- R_{IR}=3.3 kΩ
- Ta=25 °C

Package Outline Unit : mm

48PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-48P-L04
EIAJ CODE	QFP048-P-1212
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.7g