

N- and P-Channel MOSFET

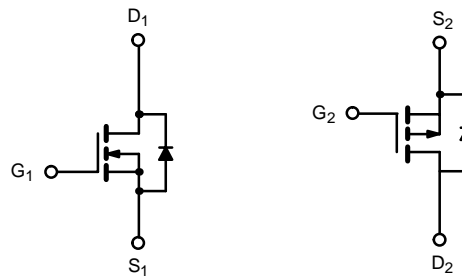
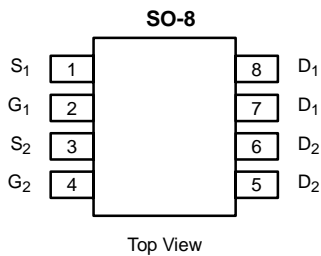
PRODUCT SUMMARY			
	V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
N-Channel	30	0.018 @ V _{GS} = 10 V	7.8
		0.027 @ V _{GS} = 4.5 V	6.4
P-Channel	-8	0.042 @ V _{GS} = -4.5 V	-5.0
		0.060 @ V _{GS} = -2.5 V	-4.0

FEATURES

- TrenchFET® Power MOSFET

APPLICATIONS

- Level Shift
- Load Switch



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	N-Channel		P-Channel		Unit
		10 sec.	Steady State	10 sec.	Steady State	
Drain-Source Voltage	V _{DS}	30		-8		V
Gate-Source Voltage	V _{GS}	±20		±8		
Continuous Drain Current (T _J = 150°C) ^{a, b}	T _A = 25°C	7.8	6.0	-5.0	-3.8	A
	T _A = 70°C	6.0	5.2	-3.6	-3.0	
Pulsed Drain Current	I _{DM}	30		-30		
Continuous Source Current (Diode Conduction) ^{a, b}	I _S	1.8	1.0	-1.8	1.0	W
Maximum Power Dissipation ^{a, b}	T _A = 25°C	2	1.20	2	1.2	
	T _A = 70°C	1.3	0.75	1.3	0.75	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150				°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	N-Channel		P-Channel		Unit
		Typ	Max	Typ	Max	
Maximum Junction-to-Ambient ^a	t ≤ 10 sec	50	62.5	50	62.5	°C/W
	Steady-State	85	105	85	105	
Maximum Junction-to-Foot (Drain)	Steady-State	30	40	30	40	

Notes

- a. Surface Mounted on FR4 Board.
b. t ≤ 10 sec

SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

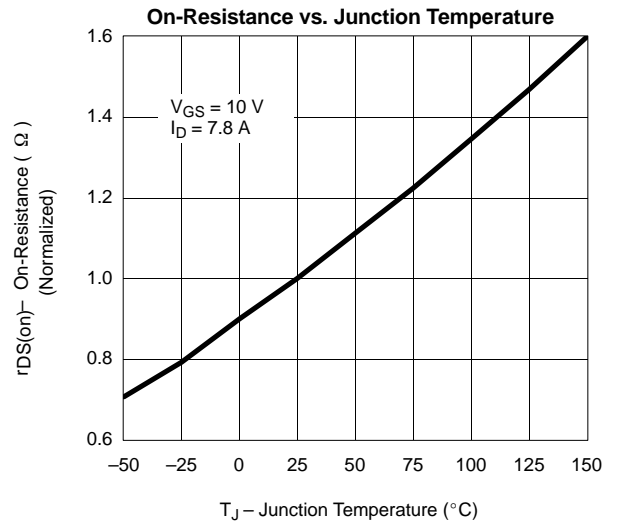
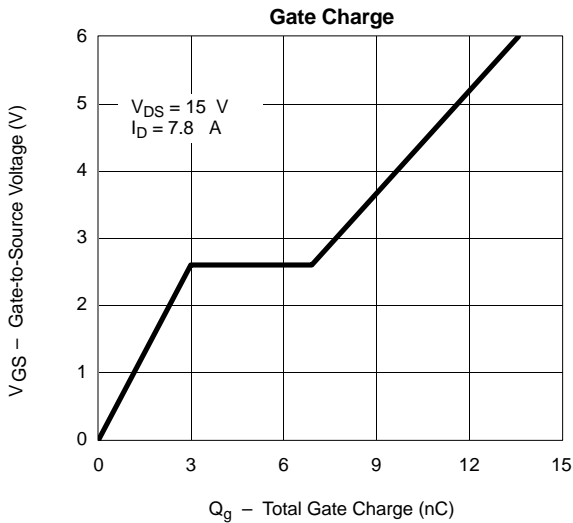
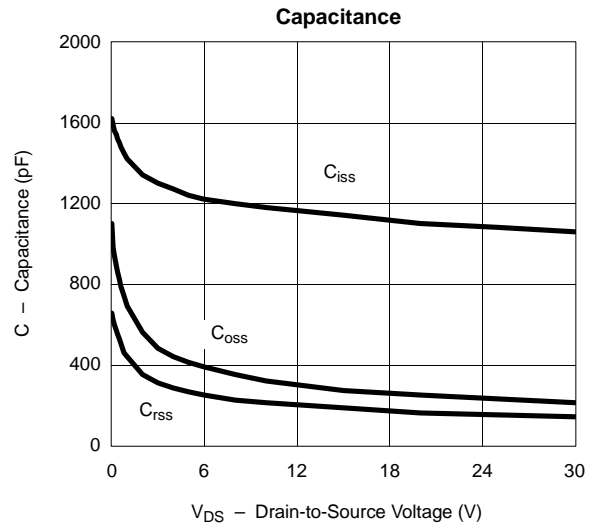
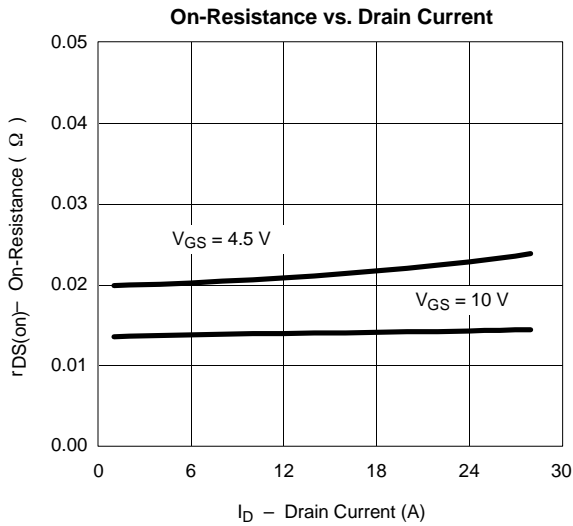
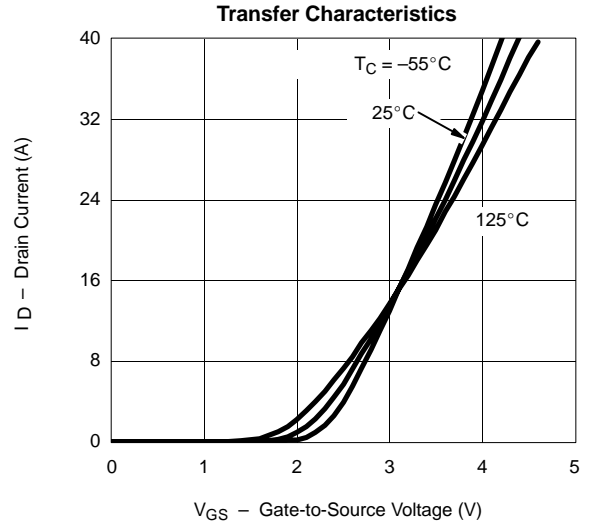
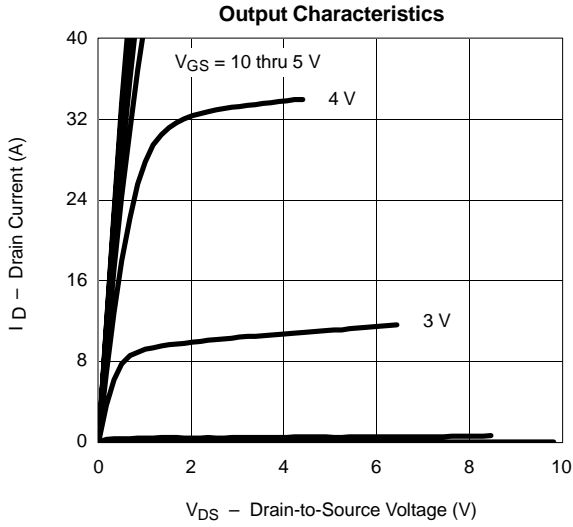
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.8		1.8	V
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-0.45		1.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V	N-Ch			±100	nA
		V _{DS} = 0 V, V _{GS} = ±8 V	P-Ch			±100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24 V, V _{GS} = 0 V	N-Ch			1	μA
		V _{DS} = -6.4 V, V _{GS} = 0 V	P-Ch			-1	
		V _{DS} = 24 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch			5	
		V _{DS} = -6.4 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch			-5	
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	N-Ch	20			A
		V _{DS} = -5 V, V _{GS} = -4.5 V	P-Ch	-20			
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 10 V, I _D = 7.8 A	N-Ch		0.015	0.018	Ω
		V _{GS} = -4.5 V, I _D = -5.0 A	P-Ch		0.030	0.042	
		V _{GS} = 4.5 V, I _D = 6.4 A	N-Ch		0.022	0.027	
		V _{GS} = -2.5 V, I _D = -4.0 A	P-Ch		0.048	0.060	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 7.8 A	N-Ch		18		S
		V _{DS} = -15 V, I _D = -5.0 A	P-Ch		12		
Diode Forward Voltage ^b	V _{SD}	I _S = 1.8 A, V _{GS} = 0 V	N-Ch		0.73	1.1	V
		I _S = -1.8 A, V _{GS} = 0 V	P-Ch		-0.75	-1.1	
Dynamic^a							
Total Gate Charge	Q _g	N-Channel V _{DS} = 15 V, V _{GS} = 5 V, I _D = 7.8 A P-Channel V _{DS} = -4 V, V _{GS} = -5 V, I _D = -5.0 A	N-Ch		11.5	20	nC
Gate-Source Charge	Q _{gs}		P-Ch		13.5	20	
			N-Ch		3		
Gate-Drain Charge	Q _{gd}		P-Ch		2.2		
			N-Ch		4		
Turn-On Delay Time	t _{d(on)}		P-Ch		3		
		N-Ch		15	25		
Rise Time	t _r	N-Channel V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω	N-Ch		8	15	ns
		P-Channel V _{DD} = -4 V, R _L = 4 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω	P-Ch		45	70	
Turn-Off Delay Time	t _{d(off)}	N-Ch		35	55		
		P-Ch		60	100		
Fall Time	t _f	N-Ch		10	20		
		P-Ch		55	85		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.8 A, di/dt = 100 A/μs	N-Ch		30	60	
			P-Ch		50	100	

Notes

- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

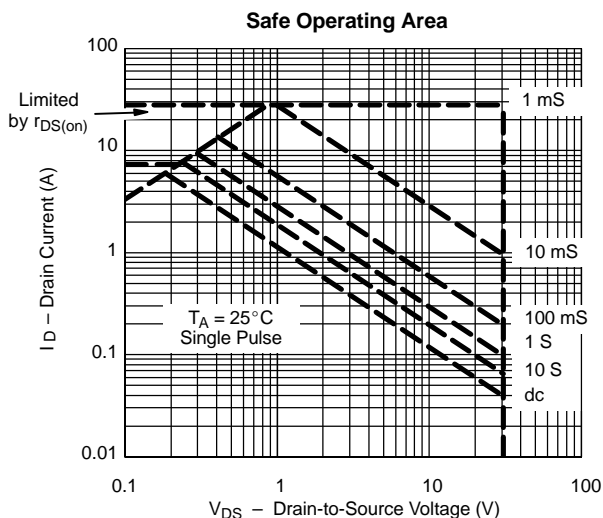
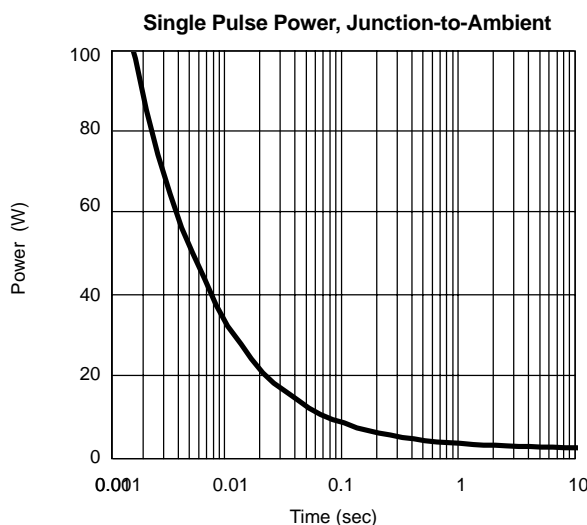
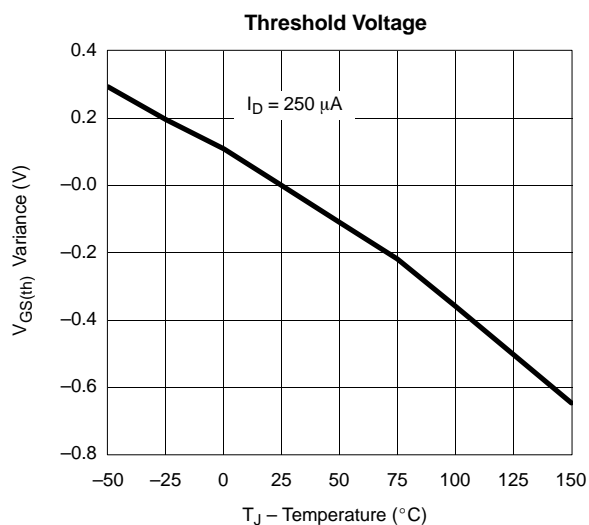
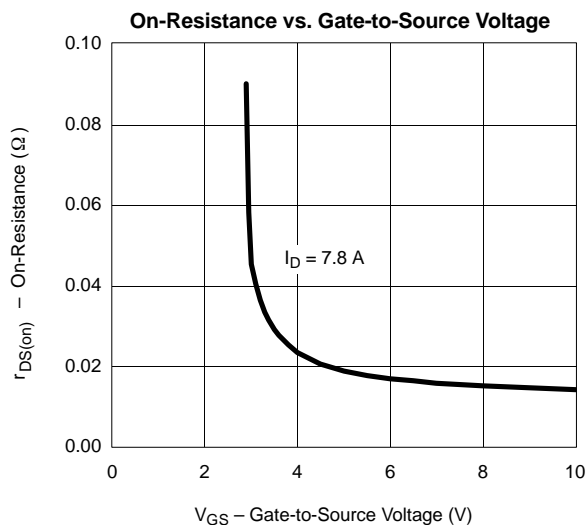
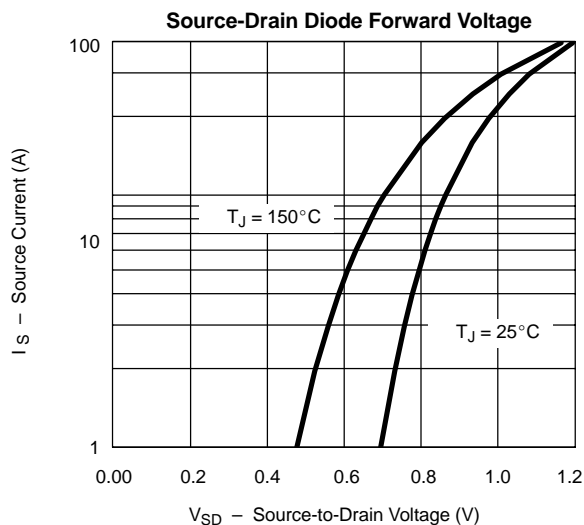


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL



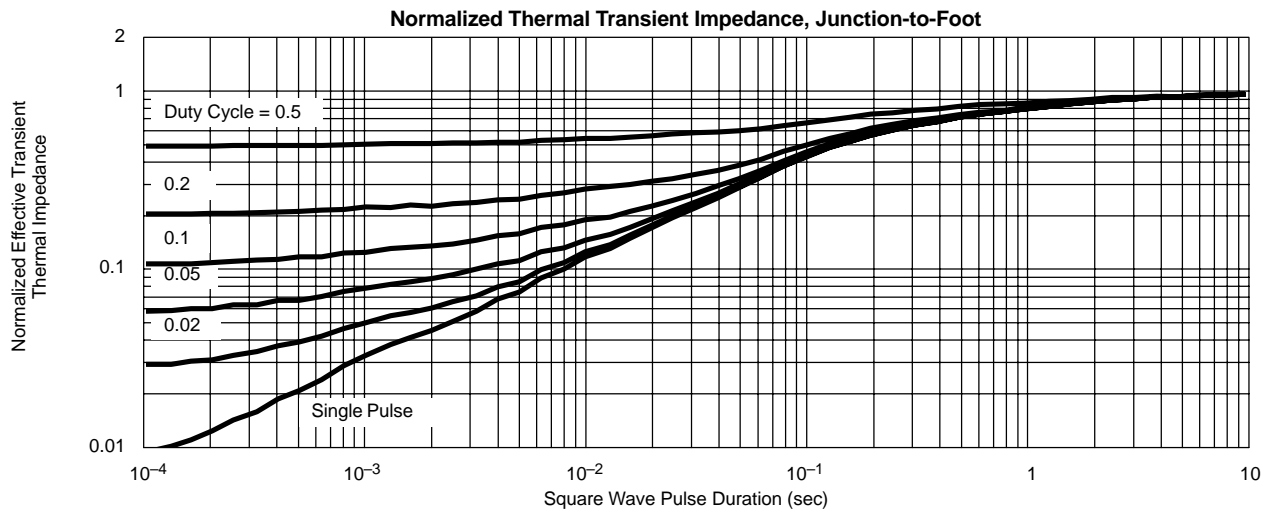
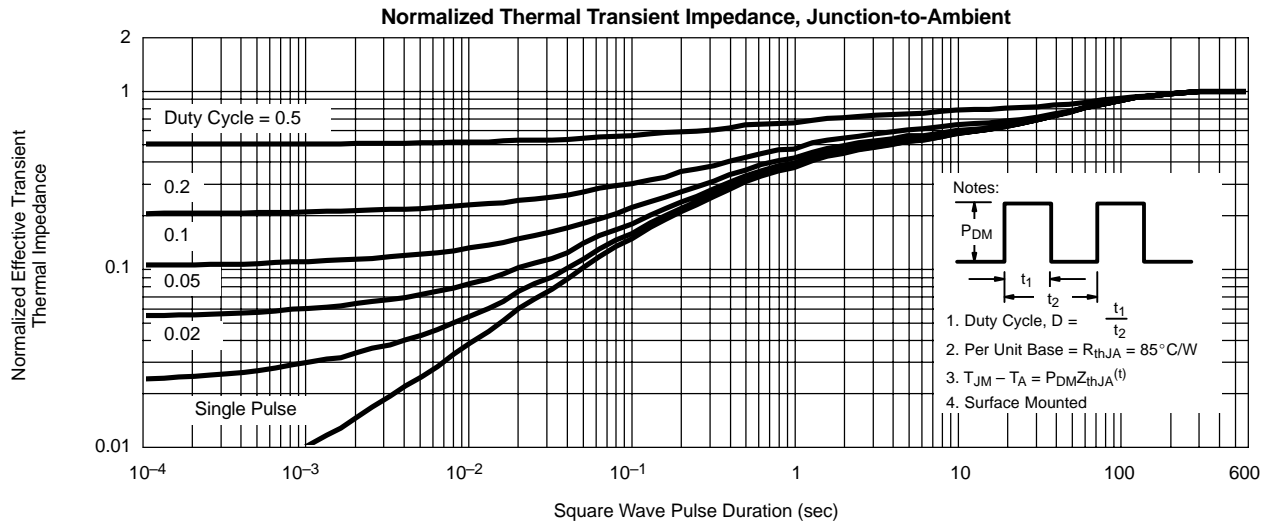
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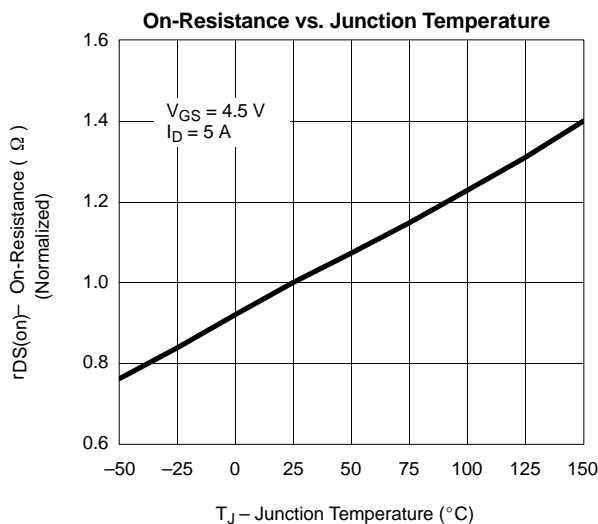
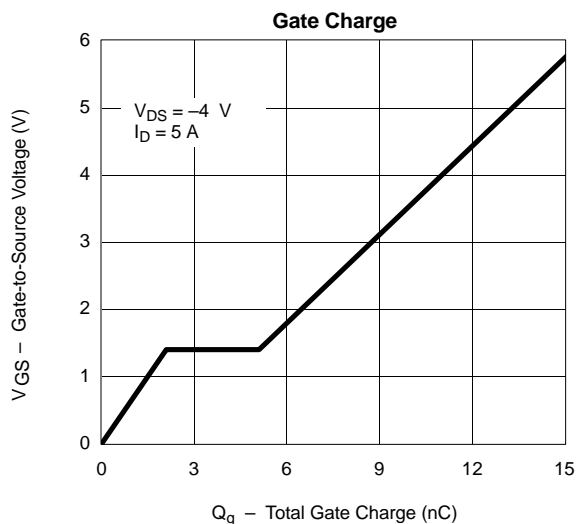
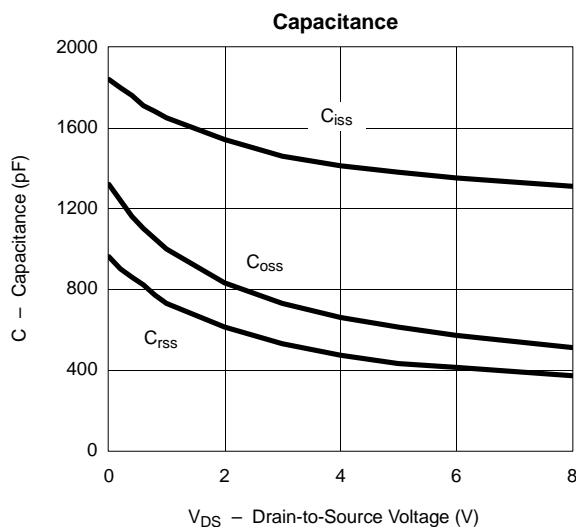
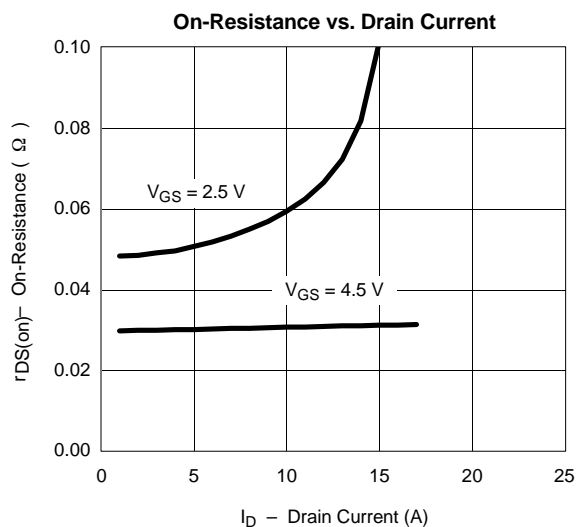
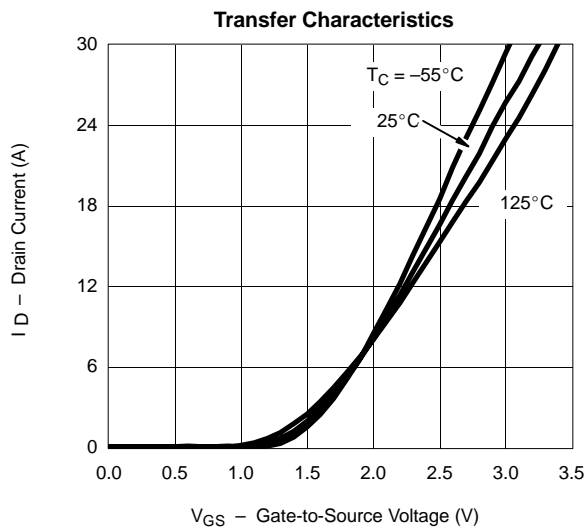
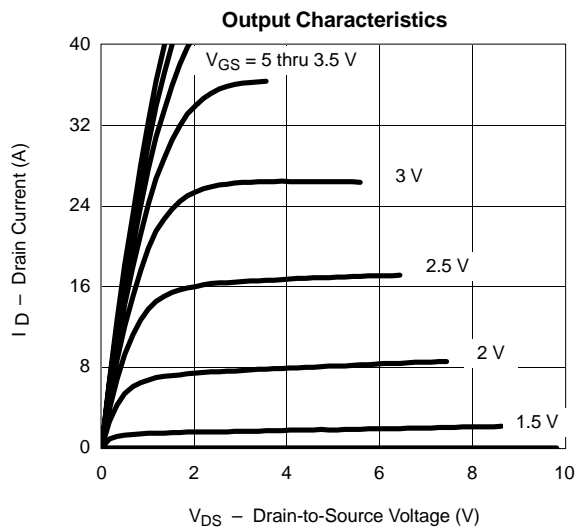


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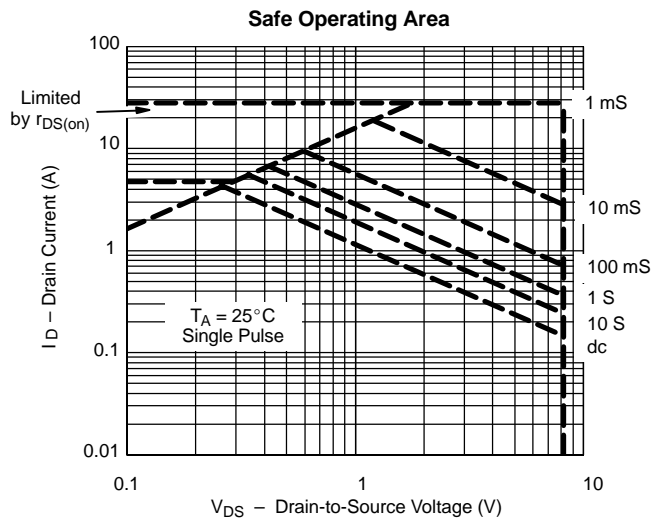
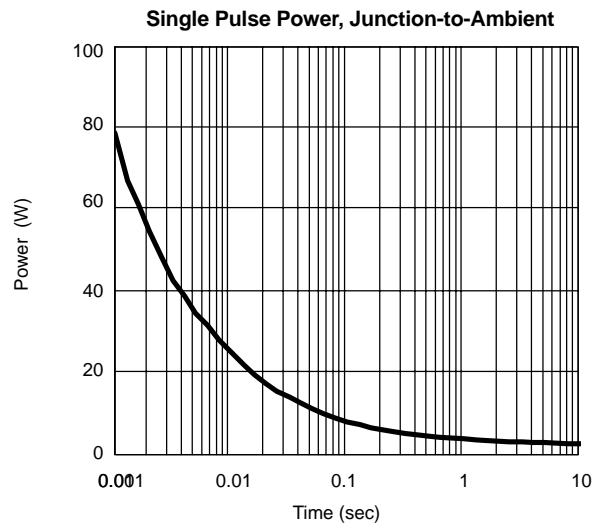
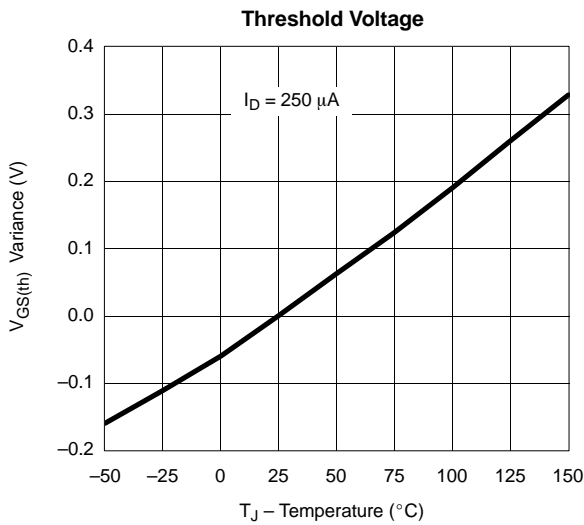
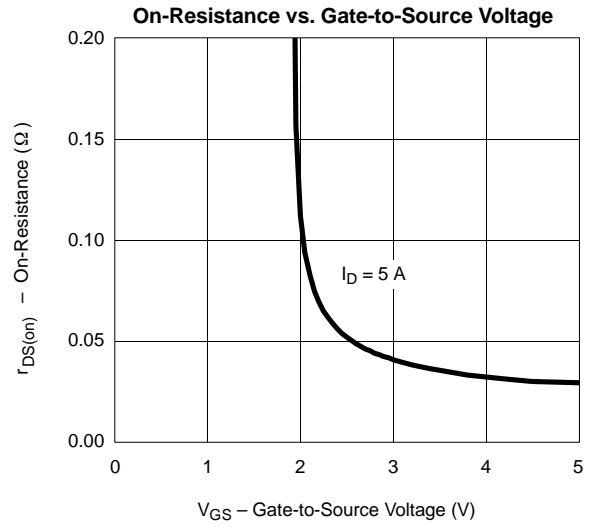
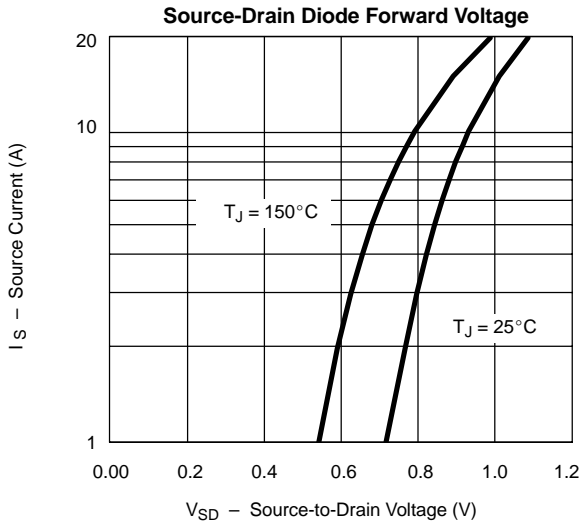
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

P-CHANNEL





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