

# DATA SHEET

## **BSP206**

P-channel enhancement mode  
vertical D-MOS transistor

Product specification  
File under Discrete Semiconductors, SC13B

April 1995

# P-channel enhancement mode vertical D-MOS transistor

**BSP206**

## DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

## QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Drain current (DC)	$-I_D$	max.	350 mA
Drain-source ON-resistance $-I_D = 200 \text{ mA}; -V_{GS} = 10 \text{ V}$	$R_{DS(on)}$	max.	6 $\Omega$
Gate threshold voltage	$-V_{GS(th)}$	max.	3.5 V

## FEATURES

- Very low  $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

## PINNING - SOT223

- 1 = gate
- 2 = drain
- 3 = source
- 4 = drain

## Marking code

BSP206

## PIN CONFIGURATION

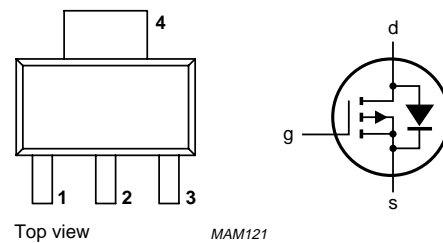


Fig.1 Simplified outline and symbol.

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### RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	350 mA
Drain current (peak)	$-I_{DM}$	max.	700 mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$ (note 1)	$P_{tot}$	max.	1.5 W
Storage temperature range	$T_{stg}$		-65 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

### THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j-a}$	=	83.3 K/W
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### Note

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the drain lead min. 6 cm<sup>2</sup>.

### CHARACTERISTICS

 $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $-I_D = 10\text{ }\mu\text{A}; V_{GS} = 0$	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current $-V_{DS} = 48\text{ V}; V_{GS} = 0$	$-I_{DSS}$	max.	1.0 $\mu\text{A}$
Gate-source leakage current $\pm V_{GS} = 20\text{ V}; V_{DS} = 0$	$\pm I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	$R_{DS(on)}$	typ. max.	4.5 $\Omega$ 6 $\Omega$
Transfer admittance $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$	$ Y_{fs} $	min. typ.	100 mS 200 mS
Input capacitance at $f = 1\text{ MHz};$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{iss}$	typ. max.	55 pF 70 pF
Output capacitance at $f = 1\text{ MHz};$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{oss}$	typ. max.	30 pF 45 pF
Feedback capacitance at $f = 1\text{ MHz};$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{rss}$	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) $-I_D = 200\text{ mA}; -V_{DD} = 50\text{ V};$ $-V_{GS} = 0\text{ to }10\text{ V}$	$t_{on}$	typ. max.	4 ns 8 ns
	$t_{off}$	typ. max.	15 ns 25 ns

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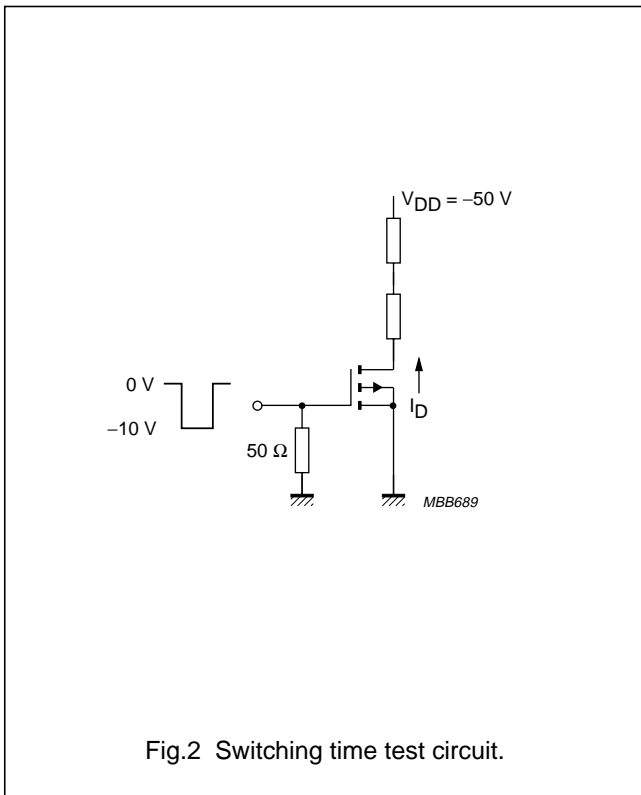


Fig.2 Switching time test circuit.

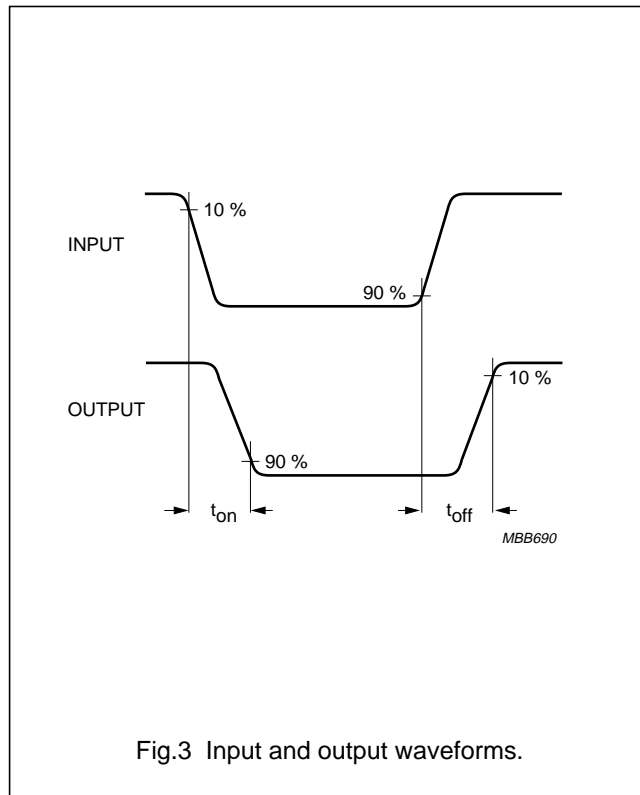


Fig.3 Input and output waveforms.

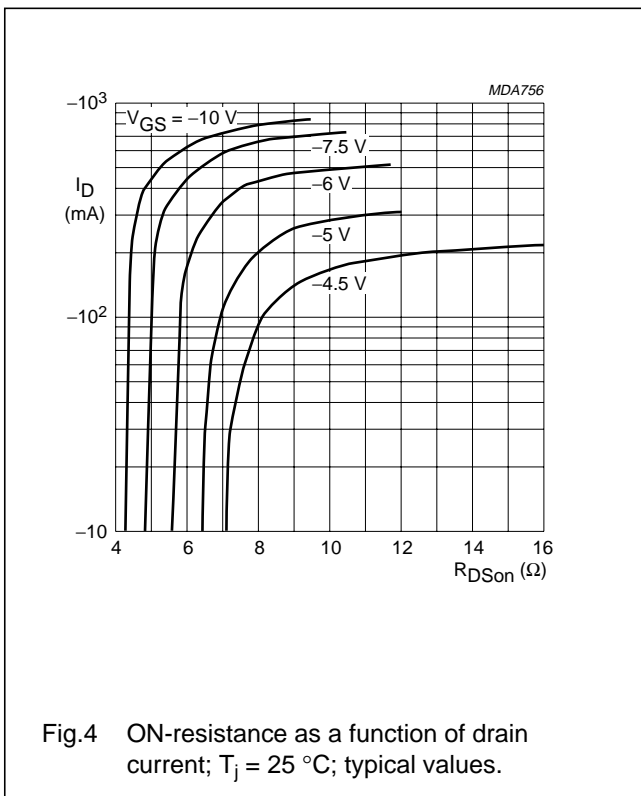


Fig.4 ON-resistance as a function of drain current;  $T_j = 25\text{ }^\circ\text{C}$ ; typical values.

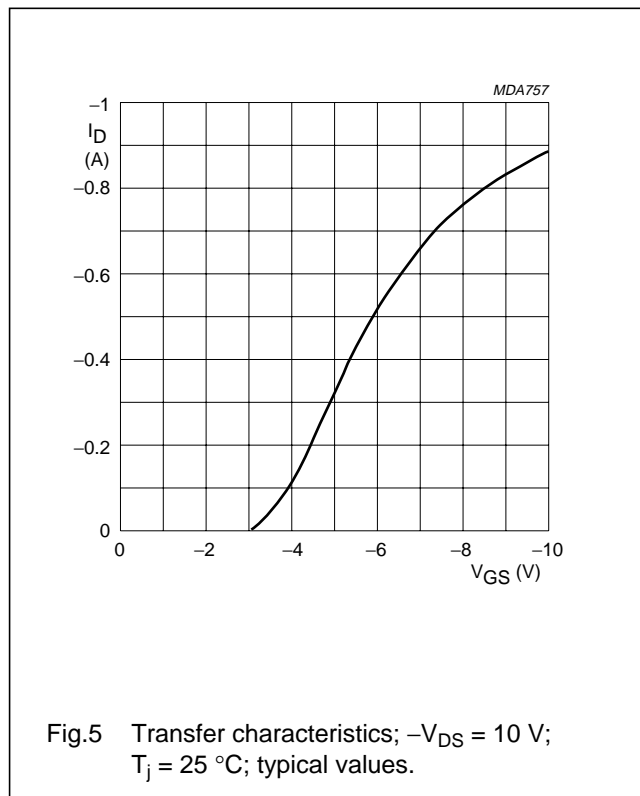
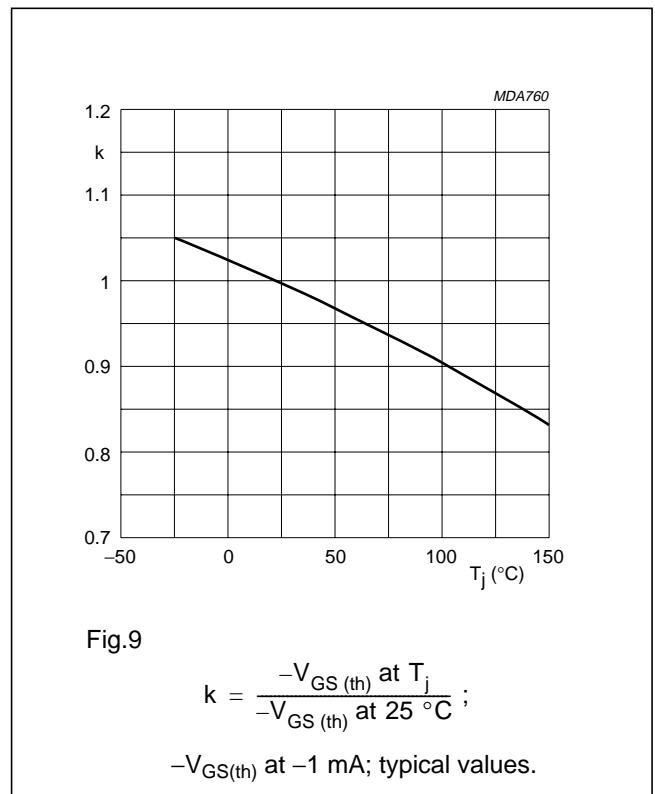
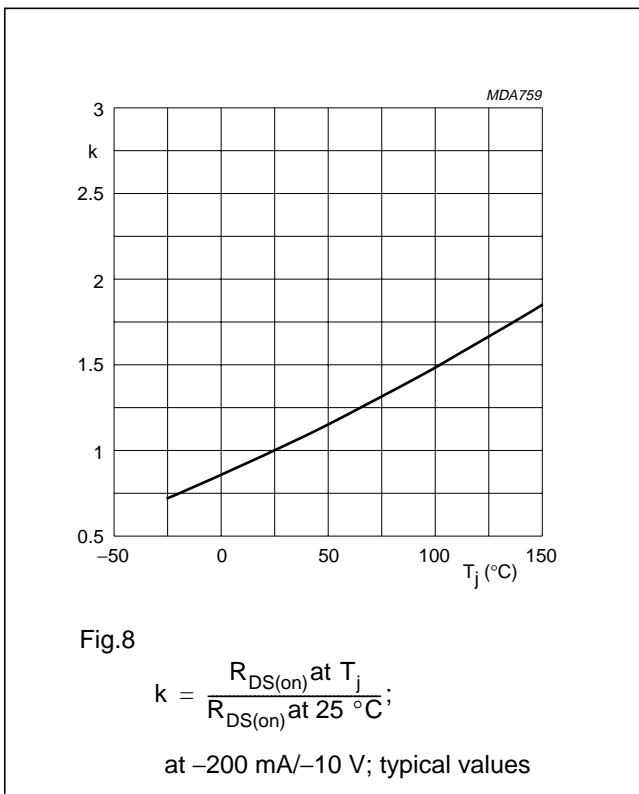
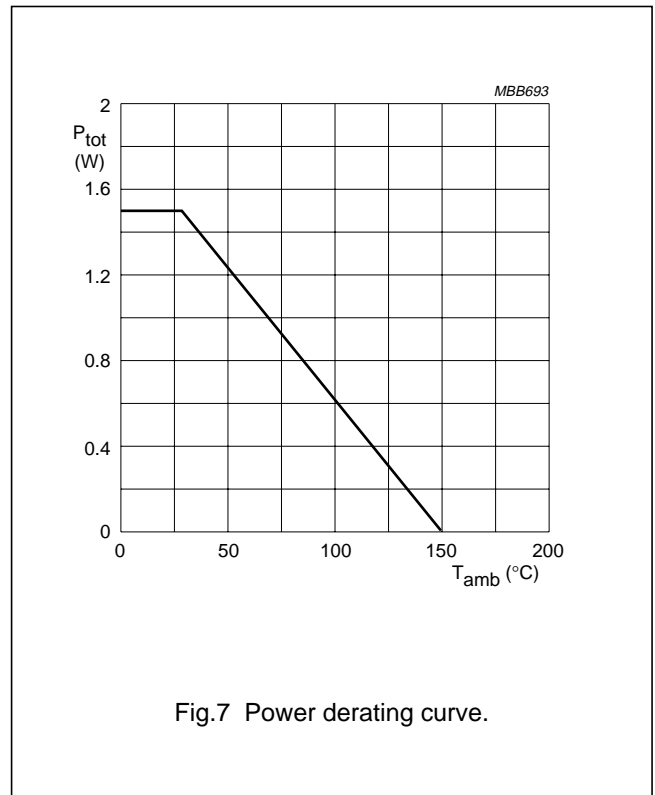
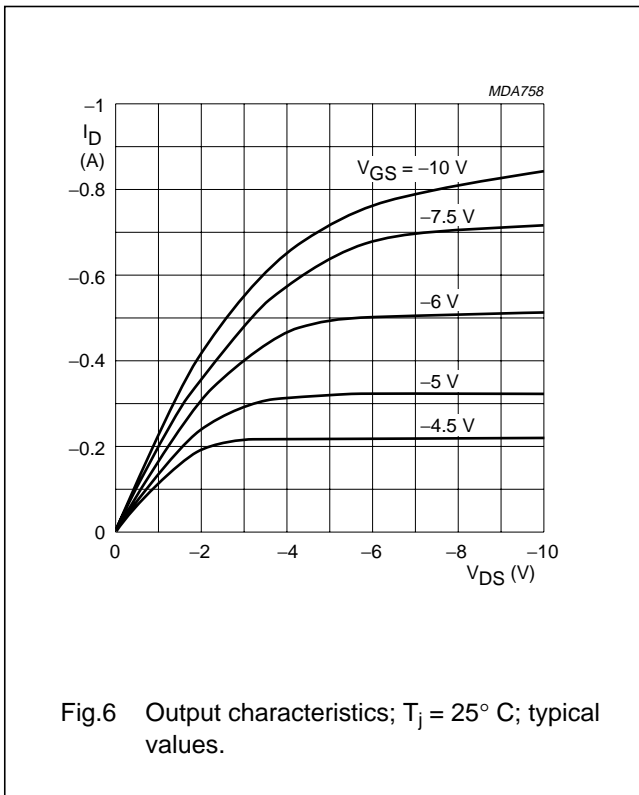


Fig.5 Transfer characteristics;  $-V_{DS} = 10\text{ V}$ ;  $T_j = 25\text{ }^\circ\text{C}$ ; typical values.

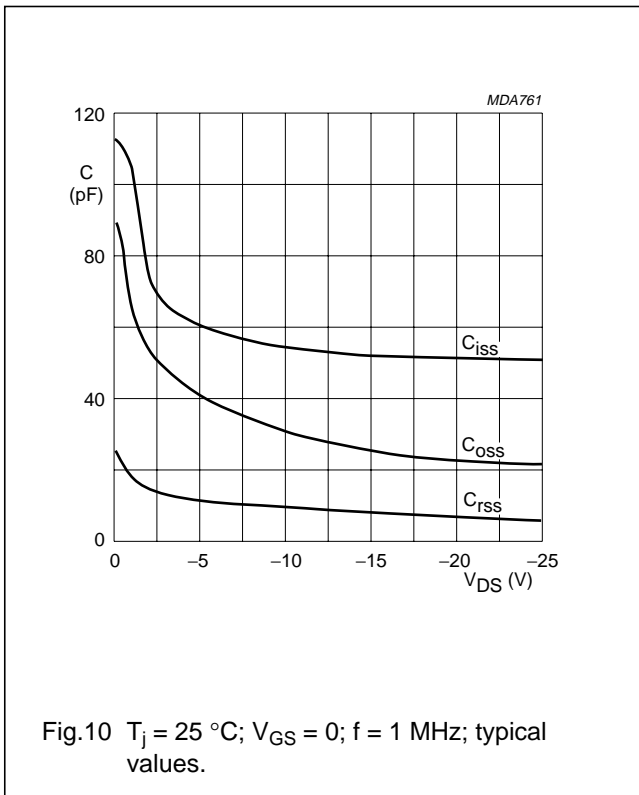
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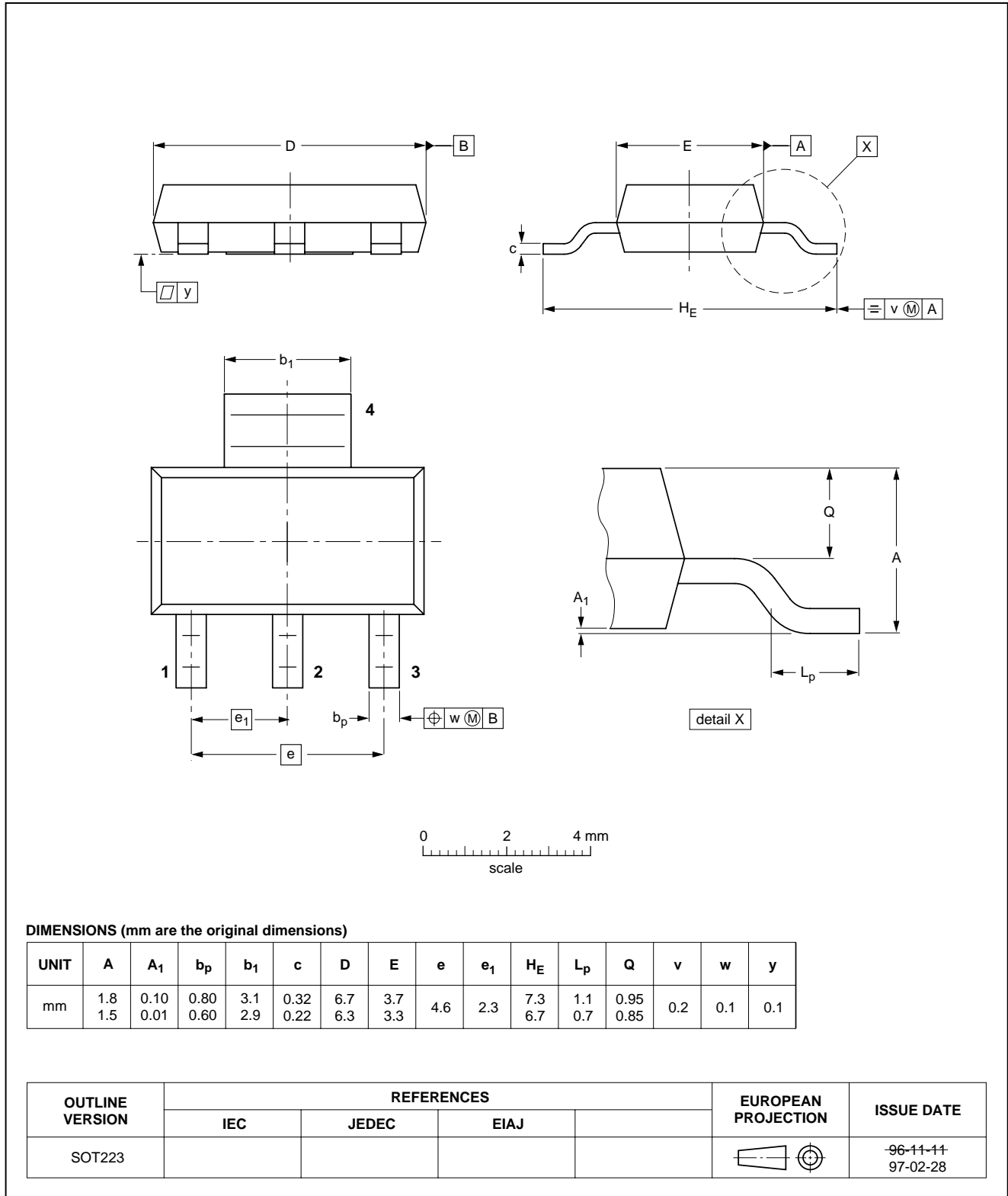
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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



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**BSP206****DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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**NOTES**

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