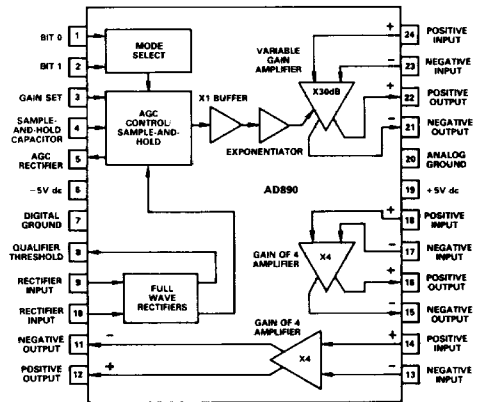


FEATURES

- An 80 MHz Bandwidth Permitting a 50 Mb/s Data Transfer Rate**
- A Variable Gain Amplifier with 30 dB max Gain and 40 dB Control Range**
- Two Gain of 4 RF Buffers**
- 200 Ω Differential Load Drive Capability**
- A Pair of Precision Rectifiers**
- AGC Level and Threshold Outputs**
- An Averaging, High Gain Sample-and-Hold for Accurate AGC Operation**
- Typical Gain Drift in Hold Mode: 0.2 dB/ms**
- Gains Trimmed and Temperature Compensated**
- AGC Operation Independent of AGC Level**
- Symmetrical AGC Attack/Decay Times**
- 1 μ s AGC Attack/Decay Times Using a 1000 pF External Capacitor**
- Suitable for Use as an Accurate Video Programmable Gain Amplifier**
- Dynamic Clamp Ensures Fast Recovery After Write to Read Transients**
- AGC RF Output Level Is Internally Preset**

AD890 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD890 is primarily intended for high performance disk subsystem use, and as such it is configured around the classic read channel processing block diagram. It is intended to be connected between the head preamplifier and the qualification circuitry required for digital data recovery. When used with the AD891 rigid disk data qualifier, data transfer rates in excess of 50 Mb/s can be processed.

A temperature-compensated AGC loop, with an exponential transfer characteristic, permits optimal settling and allows for predictable performance in the classic single integrator control loop configuration. Fast acquisition and low droop while in the hold mode allow for AGC operation to be performed within the sector header without compromising channel behavior when reading data.

The AD890 processing element has the flexibility to perform both continuous and sampled AGC functions; it is also ideal for embedded, dedicated, or mixed servo applications. Two user-defined filter/equalizer stages may be employed, thus allowing maximum design flexibility. This greatly simplifies the design of the overall channel characteristics. Using the AD890, the designer no longer needs to resort to passive techniques to isolate network functions; this avoids problems of signal loss and interaction. Two low offset, 100 MHz, full wave rectifiers provide the capability to track a 1 V peak signal. The rectifier generating

the "Qualifier Threshold" output may be used for creating a data qualification level. A second rectifier is used to drive the sample-and-hold circuitry.

The 80 MHz bandwidth of the AD890 ensures good phase linearity up to 50 MHz. Thus, data transfer rates in excess of 50 Mb/s can be supported with good error rates and predictable channel behavior.

The AD890 is available in both a 24-pin, slim-line cerdip package and in a 28-pin PLCC package and is specified to operate over the 0 to +70°C commercial temperature range.

SPECIFICATIONS (@ +25°C and ±5 V dc, unless otherwise noted)

| Parameter | Conditions | AD890J | | | Units |
|----------------------------------|---|---------------------|-------|-----------------|--------|
| | | Min | Typ | Max | |
| VARIABLE GAIN AMPLIFIER | | | | | |
| Maximum Gain ¹ | Up to 40 dB Gain Reduction Differential Differential 0 dB Gain Reduction Recommended p-p Differential 1 kΩ Load, p-p Differential | 29.0 | 30.0 | 31.0 | dB |
| ±3 dB Bandwidth | | 100 | | | MHz |
| Input Resistance | | 12 | 18 | | kΩ |
| Input Capacitance | | | 1 | 5 | pF |
| Input Voltage Noise | | | 5 | | nV/√Hz |
| Input Signal Range | | | 10 | 200 | mV |
| Max Output Signal Level | | | 2.4 | | V |
| Output Impedance | | | | 5 | Ω |
| Output DC Level | | | | 3.5 | V |
| Harmonic Distortion | | 0 dB Gain Reduction | | 0.15 | % |
| | 26 dB Gain Reduction | | 1.5 | % | |
| INPUT CLAMP² | | | | | |
| Turn-On Time | Differential | | 30 | | ns |
| Turn-Off Time | | | 200 | | ns |
| Input Signal Attenuation | | | 35 | | dB |
| On-State Input Impedance | | | 14 | | Ω |
| GAIN OF 4 BUFFER | | | | | |
| Nominal Gain | T _{min} to T _{max} Up to 26 dB Gain Reduction Differential Differential 100 MHz – 0 dB Gain Reduction Recommended p-p Differential 200 Ω Load, p-p Differential 300 mV Peak Output, 200 Ω Load | 12.25 | 12.75 | 13.25 | dB |
| Gain Variation | | | ±0.25 | | dB |
| ±3 dB Bandwidth | | | 160 | | MHz |
| Input Resistance | | | 100 | | kΩ |
| Input Capacitance | | | | 1 | pF |
| Input Voltage Noise ³ | | | | 7 | nV/√Hz |
| Input Common-Mode Range | | | -1.5 | +1.5 | V |
| Output Impedance | | | | 10 | Ω |
| Output Signal Level | | | | 1.3 | V |
| Max Output Signal Level | | | 4.8 | | V |
| Output DC Level | | | 2.5 | V | |
| Harmonic Distortion | | | 0.20 | % | |
| FULL WAVE RECTIFIER | | | | | |
| Input Signal Level | p-p Differential | 0.3 | | 3 | V |
| -3 dB Bandwidth | 100 mV @ 1 V Peak Input | 100 | | | MHz |
| Max Output Signal Level | | 1.5 | | | V |
| Output Impedance ⁴ | | | 25 | | Ω |
| DC Offset ⁴ | Relative to Ground | | 10 | ±20 | mV |
| AGC CONTROL SECTION | | | | | |
| Attack Time | 26 dB Gain Step – 1000 pF C _{SAMPLE} | | 1.0 | | μs |
| | 26 dB Gain Step – <50 pF C _{SAMPLE} | | 120 | | ns |
| Hold Time | 1 dB Gain Change – 1000 pF C _{SAMPLE} | | 10 | | ms |
| AGC Charge Current | | | 0.8 | | mA |
| AGC Control Range | | 36 | 40 | | dB |
| AGC Control Sensitivity | Per 20 mV Input | | 1 | | dB |
| AGC Control Linearity | 26 dB AGC Range | | | ±0.25 | dB |
| Set Level Input Range | For Specified Accuracy | 0 | | 800 | mV |
| | Nondestructive Input Range | -0.3 | | V _{CC} | V |
| MODE CONTROL SECTION | | | | | |
| TTL Compatible | V _{IH} = 2.7 Volts V _{IL} = 0.4 Volts | 2.0 | | 0.8 | V |
| V _{IH} | | | | | |
| V _{IL} | | | | 1 | μA |
| I _{IH} | | | -4.5 | -12.0 | μA |
| I _{IL} | | | | 50 | ns |
| Mode Switching Times | | | | | |
| POWER SUPPLY REQUIREMENTS | | | | | |
| Operating Range V _{CC} | | +4.5 | | +5.5 | V |
| Operating Range V _{EE} | | -4.68 | -5.2 | -5.72 | V |
| Quiescent Current | T _{min} to T _{max} | | | | |
| V _{CC} | Hold/Acquire/Set Gain Mode | 44 | 60 | 76 | mA |
| V _{EE} | Hold/Acquire/Set Gain Mode | 18 | 28 | 40 | mA |
| V _{CC} | Clamp Mode | 51 | 72 | 88 | mA |
| V _{EE} | Clamp Mode | 17 | 27 | 39 | mA |

NOTES

¹Gain calibrated in gain set mode with 0 volts applied to the Gain Set Pin.

²Clamp operation is specified with a source impedance of 200 Ω in series with 0.1 μF.

³Over the full 100 MHz bandwidth of the AD890, the worst-case rms signal-to-noise ratio is 40 dB or better with a 40 dB AGC range.

⁴Measured using a 4 kΩ resistor connected between the Qualifier Threshold Pin and V_{EE}.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ±7.5 V

RF Gain Stage Differential Input Voltage ±5.6 V

Storage Temperature Range

AD890JP, AD890JQ -65°C to +150°C

Operating Temperature Range¹

AD890JP, AD890JQ 0 to +70°C

Lead Temperature Range (Soldering 60 sec) +300°C

NOTE

¹28-pin PLCC package: θ_{JA} = 100°C/W;

24-pin cerdip package: θ_{JA} = 55°C/W.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Logic Assignments | Bit 0 | Bit 1 |
|-------------------|-------|-------|
| AGC Acquire | 0 | 0 |
| AGC Hold | 0 | 1 |
| Gain Set | 1 | 0 |
| Input Clamp | 1 | 1 |

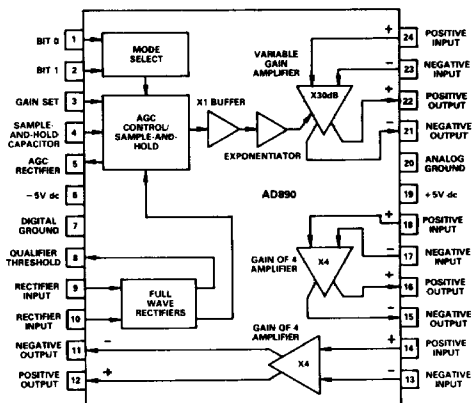
ORDERING GUIDE

| Model | Package | Package Options* |
|---------|---------------|------------------|
| AD890JQ | 24-Pin Cerdip | Q-24 |
| AD890JP | 28-Pin PLCC | P-28A |

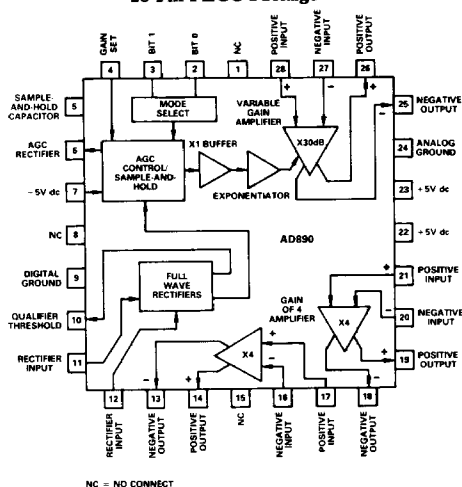
*See Section 20 for package outline information.

CONNECTION DIAGRAMS

24-Pin Cerdip Package



28-Pin PLCC Package



Typical Characteristics @ +25°C with ±5 V Supplies

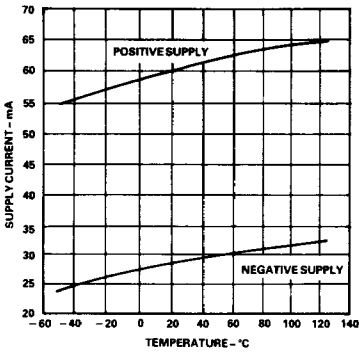


Figure 1. Supply Current vs. Temperature

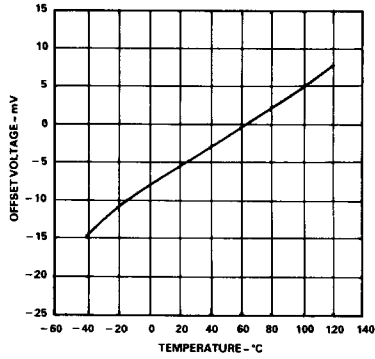


Figure 2. Rectifier Offset vs. Temperature

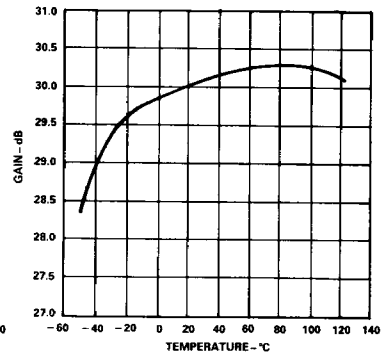


Figure 3. VGA Gain vs. Temperature

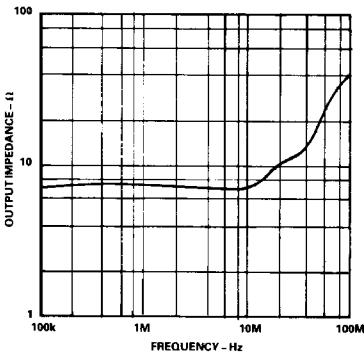


Figure 4. VGA Output Impedance vs. Frequency

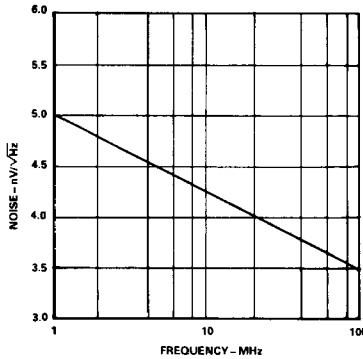


Figure 5. VGA Voltage Noise vs. Frequency

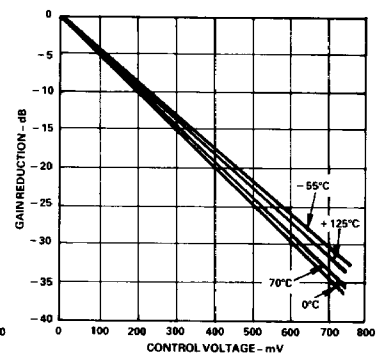


Figure 6. VGA Gain Reduction vs. Control Voltage

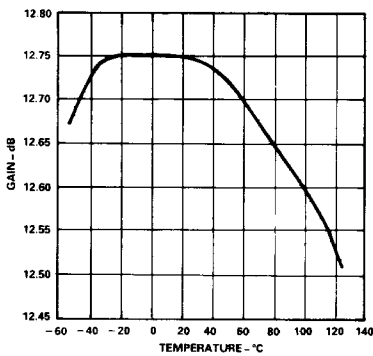


Figure 7. X4 Buffer Gain vs. Temperature

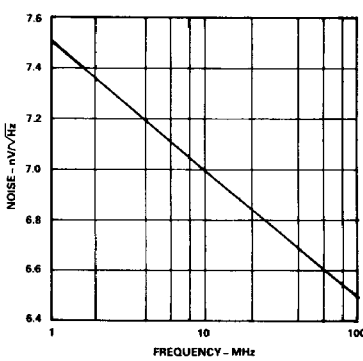


Figure 8. X4 Buffer Voltage Noise vs. Frequency

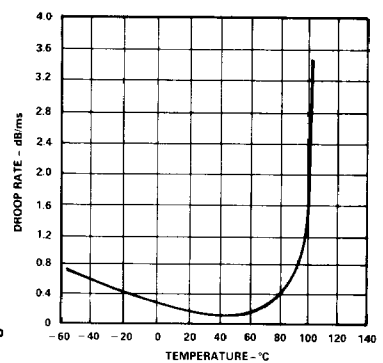


Figure 9. Hold-Mode Droop Rate vs. Temperature

GENERAL LAYOUT REQUIREMENTS

Almost 60 dB of total gain is available at 100 MHz. Care must be taken to ensure good RF practice in the PC layout to avoid oscillations in the 150 MHz–350 MHz region. A parallel combination of 0.1 μF and 0.01 μF ceramic bypass capacitors should be used as close to the supply pins as possible.

Additionally, a single pole RC filter applied at the input of each stage, with a cutoff in the region of 100 MHz–150 MHz, will help avoid oscillation problems. As a general rule, keep the connections to interstage components as short as possible; it is also recommended that any low pass filtering function which may be required by the system be performed between the VGA stage and the first X4 buffer amplifier. A ground plane should be used to surround any interstage components wherever possible. If these simple rules are followed, stable operation should be assured.

BIASING THE RF GAIN STAGES

The VGA Stage

The 30 dB variable gain stage is biased at a potential of one diode drop above analog ground. No additional dc bias is required, but ac coupling is necessary. The bias voltage is maintained during normal operation and during operation of the clamp. In order for the clamp to operate correctly with an emitter follower driven input, 50 Ω –100 Ω resistors should be placed in series with the input coupling capacitors. These resistors can be used in conjunction with a 5.1 pF shunt capacitor to limit the input bandwidth to 150 MHz. In the case of an open collector driven input with resistive termination, no additional series resistors are required.

The differential outputs have a nominal dc value of 1.5 V less than the positive supply. Internal 1300 Ω resistors provide bias current to the output emitter followers which operate with 2.7 mA nominal current. Output drive can be increased by an additional 2.5 mA by paralleling external resistors to either the analog ground or the negative power supply. However, caution should be exercised in order to avoid causing excess dissipation for the package. The recommended output level for the VGA is 300 mV p-p differential into 200 Ω loads.

The X4 Buffers

The inputs of these stages have no committed dc biasing, and an input bias current path must be provided. This path can normally be supplied via shunt resistors to analog ground which are generally part of the interstage filter termination networks. The inputs can be biased successfully within ± 1.5 V of analog ground.

Output drive can be increased in a similar manner to that described for the VGA stage. The nominal dc output level is 2.5 V with the internal 500 Ω load resistors connected to analog ground which provides a nominal standing current of 5 mA to the output emitter followers. This current can be increased by up to an additional 5 mA by paralleling external resistors to either analog ground or the negative power supply. As before, precautions to limit excessive overall power dissipation apply when steps are taken to increase the output drive capability.

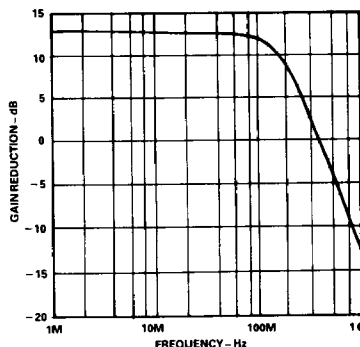


Figure 10. X4 Buffer Frequency Response (100 Ω in Series with 1 μF Load)

OPERATING THE FULL WAVE RECTIFIERS

The full wave rectifiers consist of two nearly identical stages. Full wave rectification is performed in each stage using two transistors whose emitters are connected together. The inputs to the two full wave rectifiers are biased at one diode drop above analog ground; therefore, ac coupling is recommended. The full wave rectifier outputs – “AGC Rectifier” and “Qualifier Threshold” – are connected directly to these commoned emitters. Thus, the normal output voltage with zero input signal applied is close to analog ground. The “AGC Rectifier” pin allows access to the output of the rectifier which drives the AGC sample-and-hold section of the AD890. The “Qualifier Threshold” pin allows access to the output of the threshold rectifier.

The AGC rectifier has an internal 2 k Ω resistive pull-down connected between analog ground and the negative power supply pin. The threshold line has no built in pull-down, in order to allow for a peak hold capability during thresholding. If a well controlled rectifier offset is required, an external 4 k Ω pull-down resistor at the “Qualifier Threshold” pin is recommended and will produce a nominal 10 mV offset.

THE AGC SAMPLE-AND-HOLD

The AGC sample-and-hold section performs averaging of the input waveform to set the RF average output level to 200 mV single ended, or 330 mV peak for a sinusoidal signal. Thus, without a peak hold capacitor at the “AGC Rectifier” pin, accurate AGC operation only occurs with sinusoidal input signals. An approximate 2 mA pull-down current is permanently present at the “AGC Rectifier” pin, and a capacitor may be added here to provide a degree of peak hold for AGC operation within non-sinusoidal fields. A capacitance value of less than 0.03 μF or less per μs of transition spacing is recommended. The addition of the capacitor alters the symmetry of the attack and decay rates of the rectifier, which is otherwise symmetric in operation. In order to ensure that the overall AGC response is the same for both high-to-low and low-to-high input level steps, it is necessary to make the rectifier attack and decay times at least a factor of two less than the AGC response time.

The AGC acquire time is approximately 1 μ s per 1000 pF of hold capacitor. A low leakage variety of hold capacitor, such as a silver mica, is necessary to ensure low droop rates. The "Gain Set" pin should be tied to analog ground if not used, in order to prevent excessive leakage which would otherwise affect the hold performance.

The AGC control potential is present at the "Sample-and-Hold Capacitor" pin. If control over open-loop gain is desired, based on AGC control potentials obtained during trial AGC operations, a FET input op amp should be used to buffer this node in order to avoid disturbing the hold operation.

USING THE AD890 AS A PROGRAMMABLE GAIN AMPLIFIER

The AD890 is ideally suited for use as an accurate video programmable gain amplifier. If the X4 buffers are utilized with the variable gain amplifier, nearly 60 dB of total gain is available at frequencies up to 100 MHz. The VGA gain and exponentiator scale factors are trimmed with respect to dc control potentials applied to the "Gain Set" pin. In this mode of operation (see Logic Assignments for bit pattern to be applied to the "Bit 0" and "Bit 1" pins), a 0 V dc potential applied to the "Gain Set" pin will produce a nominal VGA gain of 30 dB. With an additional 12.75 dB from each X4 buffer, total nominal gain is 55 dB. Each 20 mV increment of voltage applied will produce a 1 dB reduction in gain. A simple equation can be used to calculate the nominal gain of VGA in this mode:

$$VGA \text{ Gain (dB)} = (30 - V_{GAIN \text{ SET}} \times 50)$$

where $V_{GAIN \text{ SET}}$ is in volts.

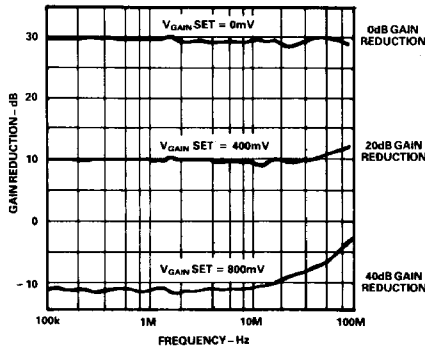


Figure 11. Frequency Response of VGA Gain for Different Gain Set Voltages

OPERATION WITH +5 V, +12 V SUPPLIES

Operation with +5 V (± 0.5 V) and +12 V (± 0.6 V) supplies is readily achieved. Figure 12 shows the AD890 configured for +5 V, +12 V operation. The analog and digital grounds must be connected to the +5 V line or to an available center tap of

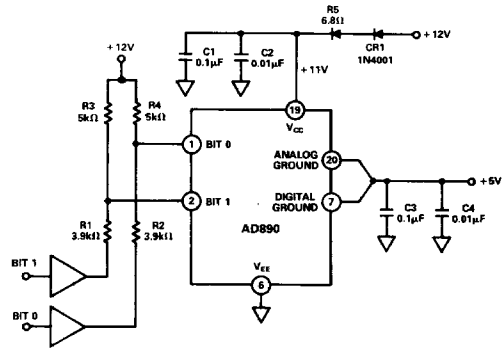


Figure 12. AD890 Connection for +5 V, +12 V Operation

the +12 V supply. Thus connected, a current of approximately 30 mA will flow in this line under normal operation. The input clamping action occurs with respect to this line, increasing its current by an additional 12 mA or so.

Both the +5 V and +12 V supplies should be RF bypassed to ground with at least two capacitors: values of 0.1 μ F and 0.01 μ F are recommended. In addition, some higher level of decoupling capacitance such as 3.3 μ F value may be desirable. Next, insert two 100 mA diodes in series with the +12 V supply. This helps to reduce overdissipation in the chip. Power supply decoupling should occur on the circuit side of the diode network.

Finally, mode control is achieved by using open collector drivers and resistors as shown; 5.1 V Zener diodes can be substituted for resistors R1 and R2. Internal diode clamping in the AD890 permits this mode of operation.

The mode switching times will be affected by resistor values chosen; this is due to the RC time constants formed by the resistors in conjunction with the input capacitance of the chip package.

INTEGRATING WITH THE AD891 RIGID DISK DRIVE DATA QUALIFIER

Figure 13 shows a typical application using the AD890 and AD891 connected together to create a 30 MHz channel (cerdip connections shown). This circuit includes a 5-pole 30 MHz Gaussian-to-6 dB transitional filter plus a second-order RLC time domain equalizer. A typical second-order, fully differential, passive delay-line differentiator interface for the AD891 is also included. (For a more detailed description of the delay-line differentiator, see the AD891 data sheet.) The analog and digital grounds should be connected at the power supply common.

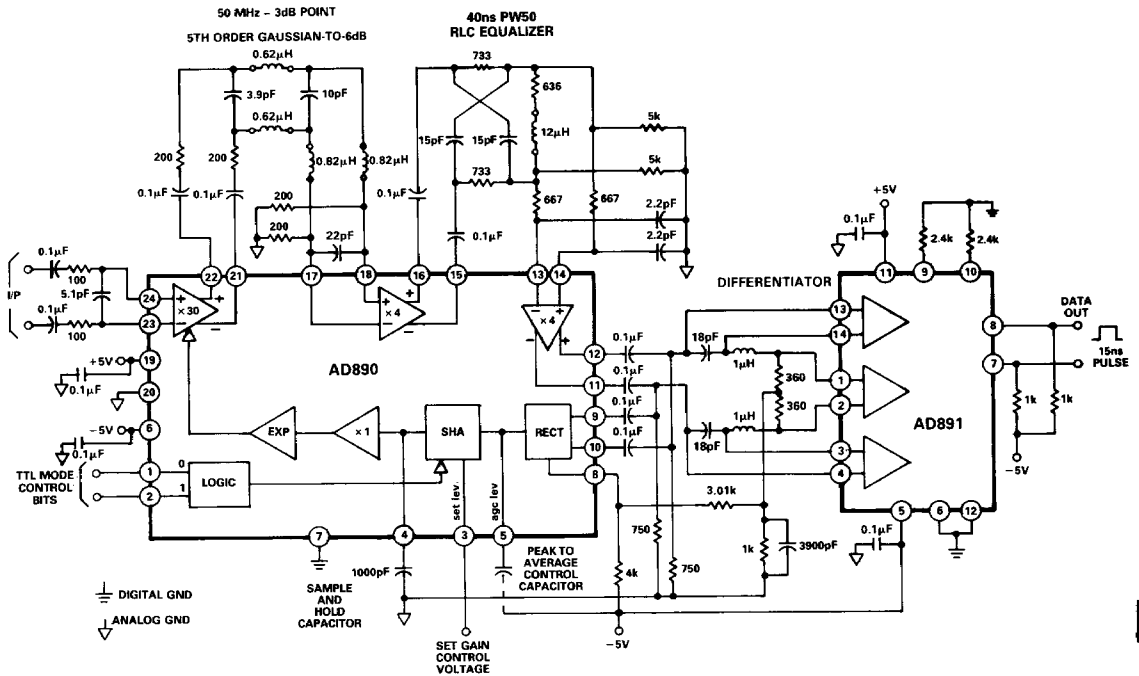


Figure 13. Typical AD890/AD891 Connection for a 30 MHz Channel

USING EQUALIZERS WITH THE AD890

The AD890 is ideal for applications where equalization is employed. The X4 buffer output drivers are designed to operate into 200 Ω loads, making tapped delay-line designs easy. Sum and differencing of different tap weights can be achieved by simple resistive dividers.

As an alternative, a simple RLC network can be implemented to provide a low cost, fully differential alternative to the three-tap, tapped delay-line equalizer which often is used for pulse slimming. Essentially, the equalizer shown in Figure 14 consists of an RC lattice, which provides the magnitude characteristic, together with an LR shunt section which acts to define the overall passband group delay and the ratio of minimum to maximum gains within the passband.

The network shown approximates a function of the form:

$$F(\omega\tau) = 1 - k \cos \omega\tau, \text{ where } k = 0.6, \text{ and } \tau = 36 \text{ ns.}$$

The circuit is optimized for a 120 ns transition PW50. Altering the 953 Ω resistor and the 24 µH inductor can change both k and τ, permitting cylinder dependent equalization to be performed, thus minimizing problems of overequalization. To alter k, the ratio of the 1.1 kΩ and 953 Ω resistors should be changed. To alter τ, the reactive element should be scaled proportionally. The equalizer in Figure 13 is optimized for k = 0.6 and τ = 12 ns.

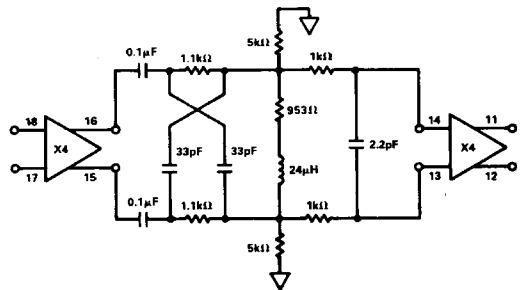


Figure 14. RLC Equalizer

It is important to note the benefits of fully differential (as opposed to single-ended) operation: (1) reduced harmonic distortion due to symmetric operation; (2) improved power supply noise rejection; (3) less insertion loss, allowing for reduced gain and, hence, improved distortion in stages prior to the equalizer.

The magnitude and group delay characteristics of this equalizer are shown in Figures 15 and 16, respectively.

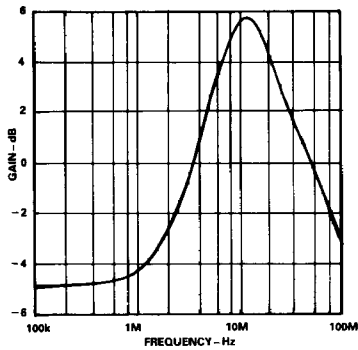


Figure 15. RLC Equalizer Magnitude Response

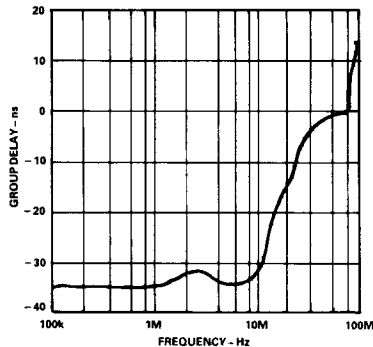


Figure 16. RLC Equalizer Group Delay Response

CHOICE OF LOW PASS FILTER WITH THE RECOMMENDED EQUALIZER

A fifth order, Gaussian-to-6 dB transitional filter is recommended for use with the equalizer. Such a low pass filter is shown in Figure 17. Low group delay ripple and high out-of-band rejection make this design work well with the recommended equalizer and the differentiator specified in the AD891 data sheet. The recommended location for the low pass filter is between the VGA and first X4 buffer. The equalizer should be placed between the first and second X4 buffers. This minimizes the potential for oscillations induced by interstage parasitic feedback.

The magnitude and group delay characteristics of this filter are shown in Figures 18 and 19, respectively.

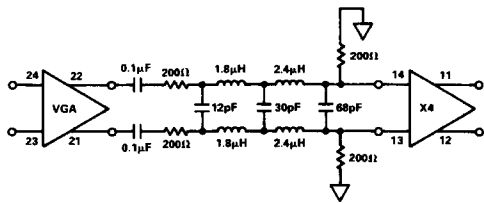


Figure 17. 5th Order Gaussian-to-6 dB Transitional Filter

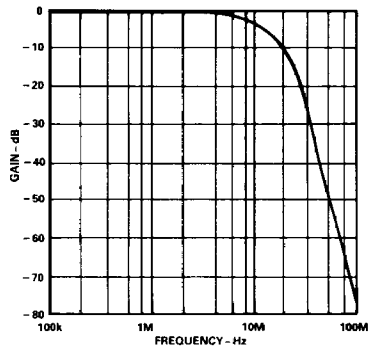


Figure 18. Gaussian Low-Pass Filter Magnitude Response

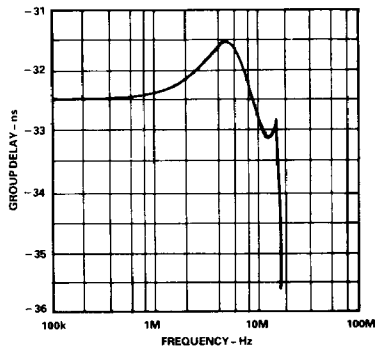


Figure 19. Gaussian Low-Pass Filter Group Delay Response