LR38666Y

One-chip System LSI for Digital Still Cameras

DESCRIPTION

The LR38666Y is a CMOS digital signal processor for color digital still camera systems of 1 310 k/ 2 140 k/ 3 300 k/3 370 k/4 200 k-pixel CCDs with primary color mosaic filters.

FEATURES

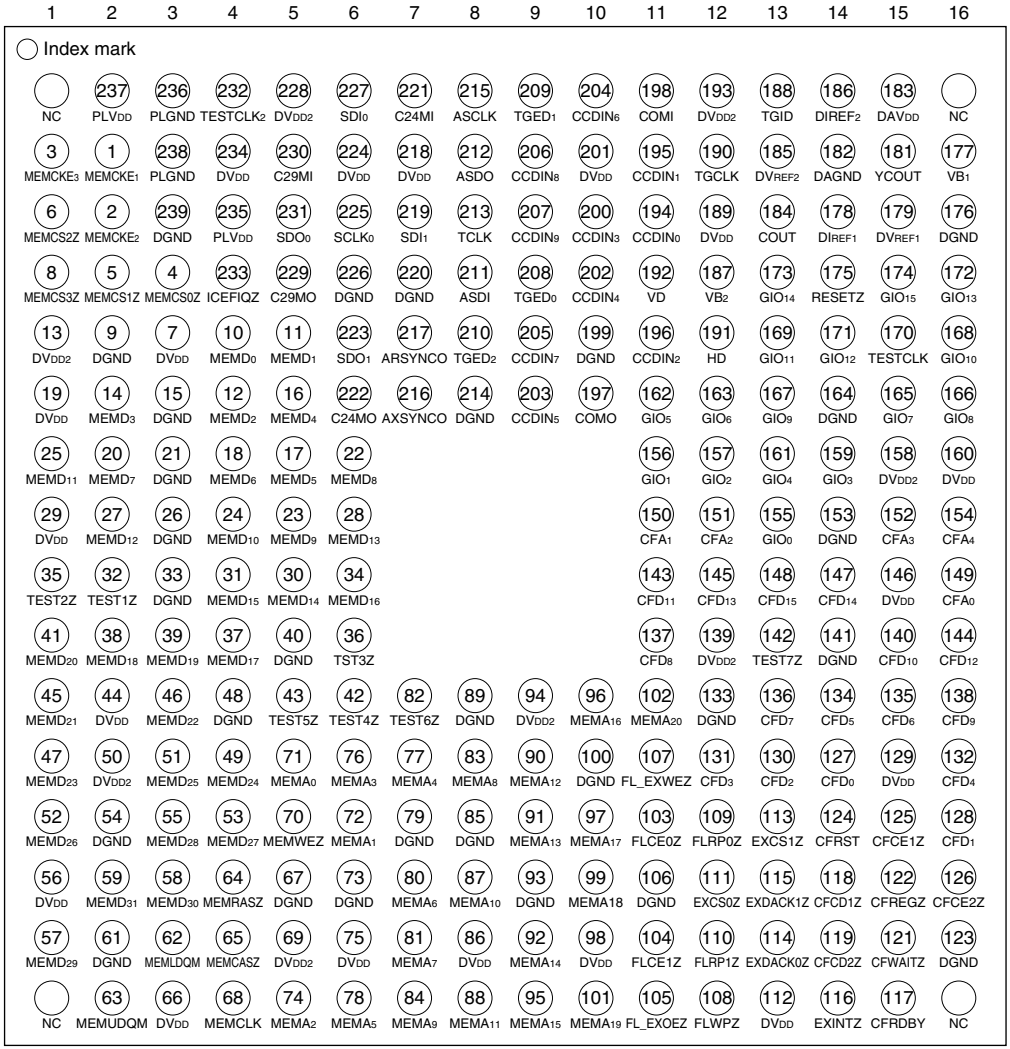
- ARM7TDMI is used as the CPU core
- CCD signal processor modules
  - Supported image size : 1 310 k/ 2 140 k/3 300 k/ 3 370 k/4 200 k pixels
  - R, G and B primary color mosaic filters : Bayer matrix, 10 bits per color
  - Built-in auto focus, auto exposure and auto white balance functions
  - Built-in digital clamp and gamma correction functions
- Video encoder module
  - Composite analog signal output mode : Switchable between NTSC and PAL
  - Built-in OSDC function
- JPEG encoding/decoding module : Built-in circuits for encoding and decoding
  - Encoding rate : Max. 66 ms per frame (for 1/10-compression in VGA mode)
  - Decoding rate : Max. 66 ms per frame (for decompression in VGA mode)

(Assuming that SDRAM is used and the internal bus is occupied by the JPEG module)

- SDRAM/flash memory controller module
- Synchronous/asynchronous SIO
- USB 1.0 is supported
- General purpose I/O ports
- Built-in audio I/F
- Built-in resizing function
- Built-in CompactFlash I/F
- Built-in SmartMedia I/F
- Power supplies
  - +2.5 V for digital/analog circuits
  - +3.3 V for digital circuits
- Package : 240-ball CSP (T-TFBGA240-1414)

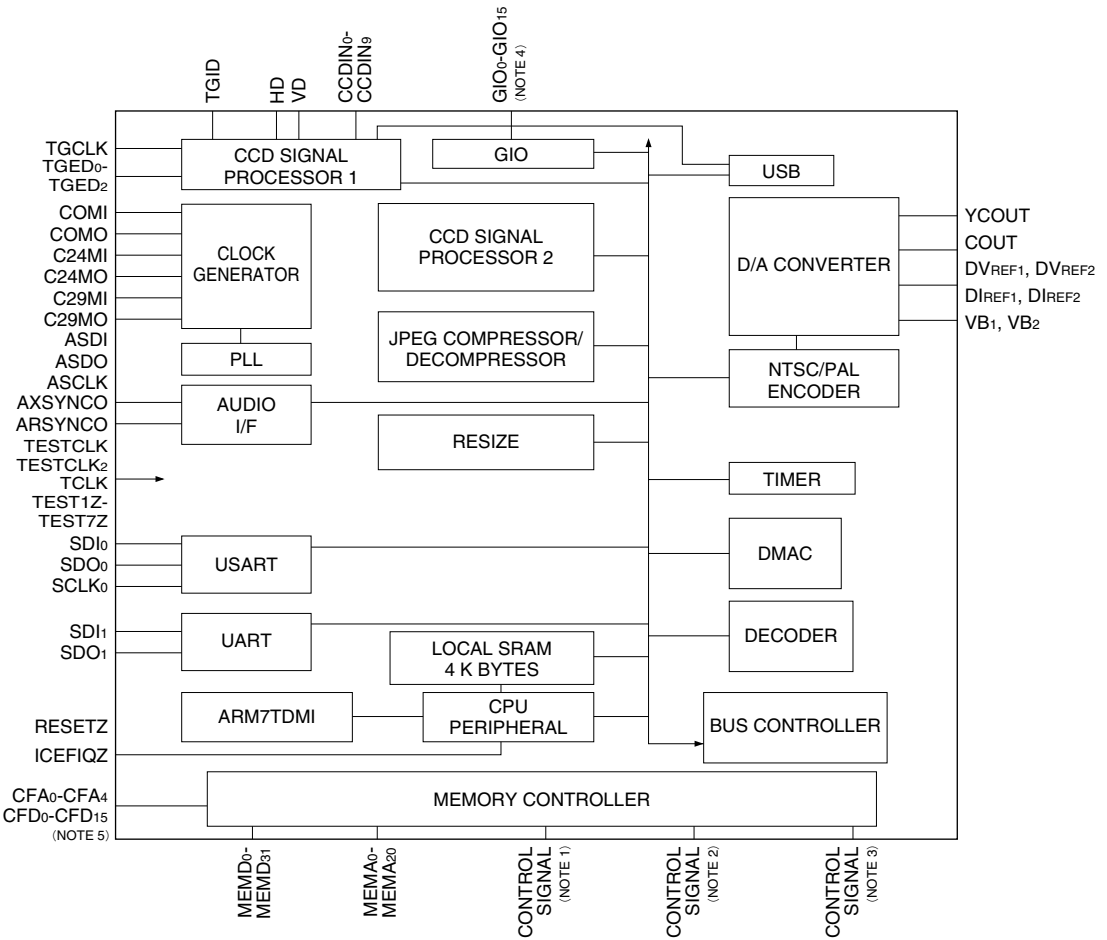
PIN CONNECTIONS

240-BALL CSP TOP VIEW



(T-TFBGA240-1414)

BLOCK DIAGRAM



NOTES :

1. Control signal for SDRAM
   MEMCLK, MEMLDQM, MEMUDQM, MEMWEZ, MEMCASZ, MEMRASZ, MEMCKE1, MEMCS0Z-MEMCS3Z
   Control signal for SDRAM or general purpose I/O.
   MEMCKE2 = GIO16, MEMCKE3 = GIO17 (set by register)
2. Control signal for flash memory and external device.
   FLCE0Z, FL_EXOEZ, FL_EXWEZ, FLWPZ, FLRP0Z, EXCS0Z, CFREGZ, CFRST, CFCE1Z to CFCE2Z
   Control signal for flash memory and external device or general purpose I/O
   FLCE1Z = GIO18, FLRP1Z = GIO19, EXCS1Z = GIO20 (set by register)
3. Input signal from external device
   EXDACK0Z, EXINTZ, CFWAITZ, CFRDBY
   Input signal from external device or general purpose I/O.
   EXDACK1Z = GIO21, CFCD1Z = GIO22, CFCD2Z = GIO23 (set by register)
4. General purpose I/O or PWM.
   GIO0 to GIO2 = CCDGEO0 to CCDGEO2, GIO9 = TX_VPO, GIO10 = TX_VMO, GIO11 = TX_OE_N, GIO12 = SUSPEND_N, GIO13 = RX_VPI, GIO14 = RX_VMI, GIO15 = RX_DATA (set by register)
5. Data I/O for CompactFlash or general purpose I/O.
   CFD8 = GIO24, CFD9 = GIO25, CFD10 = GIO26, CFD11 = GIO27, CFD12 = GIO28, CFD13 = GIO29, CFD14 = GIO30, CFD15 = GIO31 (set by register)

PIN DESCRIPTION

PIN NO.	COORDINATE	SYMBOL	IO SYMBOL	DESCRIPTION
1	2B	MEMCKE1	IO8	SDRAM clock enable, Block 1
2	2C	MEMCKE2	IO8	SDRAM clock enable, Block 2/GIO16
3	1B	MEMCKE3	IO8	SDRAM clock enable, Block 3/GIO17
4	3D	MEMCS0Z	IO8	SDRAM chip select, Block 0
5	2D	MEMCS1Z	IO8	SDRAM chip select, Block 1
6	1C	MEMCS2Z	IO8	16-bit data mode : SDRAM chip select, Block 2 32-bit data mode : Control MEMD15 to MEMD8 of SDRAM
7	3E	DVDD	–	Power supply (+3.3 V)
8	1D	MEMCS3Z	IO8	16-bit data mode : SDRAM chip select, Block 3 32-bit data mode : Control MEMD7 to MEMD0 of SDRAM
9	2E	DGND	–	Ground
10	4E	MEMD0	IO12U	Data I/O for SDRAM/flash memory/external device
11	5E	MEMD1	IO12U	
12	4F	MEMD2	IO12U	
13	1E	DVDD2	–	Internal power supply (+2.5 V)
14	2F	MEMD3	IO12U	Data I/O for SDRAM/flash memory/external device
15	3F	DGND	–	Ground
16	5F	MEMD4	IO12U	Data I/O for SDRAM/flash memory/external device
17	5G	MEMD5	IO12U	
18	4G	MEMD6	IO12U	
19	1F	DVDD	–	Power supply (+3.3 V)
20	2G	MEMD7	IO12U	Data I/O for SDRAM/flash memory/external device
21	3G	DGND	–	Ground
22	6G	MEMD8	IO12U	Data I/O for SDRAM/flash memory/external device
23	5H	MEMD9	IO12U	
24	4H	MEMD10	IO12U	
25	1G	MEMD11	IO12U	
26	3H	DGND	–	Ground
27	2H	MEMD12	IO12U	Data I/O for SDRAM/flash memory/external device
28	6H	MEMD13	IO12U	
29	1H	DVDD	–	Power supply (+3.3 V)
30	5J	MEMD14	IO12U	Data I/O for SDRAM/flash memory/external device
31	4J	MEMD15	IO12U	
32	2J	TEST1Z	IU	Test (Must be open.)
33	3J	DGND	–	Ground
34	6J	MEMD16	IO12U	Data I/O for SDRAM/external device/GIO16
35	1J	TEST2Z	IU	Test (Must be open.)
36	6K	TEST3Z	IU	
37	4K	MEMD17	IO12U	Data I/O for SDRAM/external device/GIO17
38	2K	MEMD18	IO12U	Data I/O for SDRAM/external device/GIO18
39	3K	MEMD19	IO12U	Data I/O for SDRAM/external device/GIO19

PIN NO.	COORDINATE	SYMBOL	IO SYMBOL	DESCRIPTION
40	5K	DGND	–	Ground
41	1K	$MEMD_{20}$	IO12U	Data I/O for SDRAM/external device/GIO_{20}
42	6L	TEST4Z	IU	Test (Must be open.)
43	5L	TEST5Z	IU	
44	2L	DV_{DD}	–	Power supply (+3.3 V)
45	1L	$MEMD_{21}$	IO12U	Data I/O for SDRAM/external device/GIO_{21}
46	3L	$MEMD_{22}$	IO12U	Data I/O for SDRAM/external device/GIO_{22}
47	1M	$MEMD_{23}$	IO12U	Data I/O for SDRAM/external device/GIO_{23}
48	4L	DGND	–	Ground
49	4M	$MEMD_{24}$	IO12U	Data I/O for SDRAM/external device/GIO_{24}
50	2M	DV_{DD2}	–	Internal power supply (+2.5 V)
51	3M	$MEMD_{25}$	IO12U	Data I/O for SDRAM/external device/GIO_{25}
52	1N	$MEMD_{26}$	IO12U	Data I/O for SDRAM/external device/GIO_{26}
53	4N	$MEMD_{27}$	IO12U	Data I/O for SDRAM/external device/GIO_{27}
54	2N	DGND	–	Ground
55	3N	$MEMD_{28}$	IO12U	Data I/O for SDRAM/external device/GIO_{28}
56	1P	DV_{DD}	–	Power supply (+3.3 V)
57	1R	$MEMD_{29}$	IO12U	Data I/O for SDRAM/external device/GIO_{29}
58	3P	$MEMD_{30}$	IO12U	Data I/O for SDRAM/external device/GIO_{30}
59	2P	$MEMD_{31}$	IO12U	Data I/O for SDRAM/external device/GIO_{31}
60	–	NC	–	Must be open.
61	2R	DGND	–	Ground
62	3R	MEMLDQM	O12	16-bit data mode : Control $MEMD_7$-$MEMD_0$ of SDRAM 32-bit data mode : Control $MEMD_{23}$-$MEMD_{16}$ of SDRAM
63	2T	MEMUDQM	O12	16-bit data mode : Control $MEMD_{15}$-$MEMD_8$ of SDRAM 32-bit data mode : Control $MEMD_{31}$-$MEMD_{24}$ of SDRAM
64	4P	MEMRASZ	O12	SDRAM row address strobe
65	4R	MEMCASZ	O12	SDRAM column address strobe
66	3T	DV_{DD}	–	Power supply (+3.3 V)
67	5P	DGND	–	Ground
68	4T	MEMCLK	IO12	SDRAM clock output (49.0908 MHz : double of C24MI input)
69	5R	DV_{DD2}	–	Internal power supply (+2.5 V)
70	5N	MEMWEZ	O12	SDRAM write enable
71	5M	$MEMA_0$	O12	Address for SDRAM/flash memory/external device
72	6N	$MEMA_1$	O12	
73	6P	DGND	–	Ground
74	5T	$MEMA_2$	O12	Address for SDRAM/flash memory/external device
75	6R	DV_{DD}	–	Power supply (+3.3 V)
76	6M	$MEMA_3$	O12	Address for SDRAM/flash memory/external device
77	7M	$MEMA_4$	O12	Address for SDRAM/flash memory/external device
78	6T	$MEMA_5$	O12	Address for SDRAM/flash memory/external device
79	7N	DGND	–	Ground

PIN NO.	COORDINATE	SYMBOL	IO SYMBOL	DESCRIPTION
80	7P	$MEMA_6$	O12	Address for SDRAM/flash memory/external device
81	7R	$MEMA_7$	O12	Address for SDRAM/flash memory/external device
82	7L	TEST6Z	IU	Test (Must be open.)
83	8M	$MEMA_8$	O12	Address for SDRAM/flash memory/external device
84	7T	$MEMA_9$	O12	Address for SDRAM/flash memory/external device
85	8N	DGND	–	Ground
86	8R	DV_{DD}	–	Power supply (+3.3 V)
87	8P	$MEMA_{10}$	O12	Address for SDRAM/flash memory/external device
88	8T	$MEMA_{11}$	O12	Address for SDRAM/flash memory/external device
89	8L	DGND	–	Ground
90	9M	$MEMA_{12}$	O12	Address for SDRAM/flash memory/external device
91	9N	$MEMA_{13}$	O12	Address for SDRAM/flash memory/external device
92	9R	$MEMA_{14}$	O12	Address for SDRAM/flash memory/external device
93	9P	DGND	–	Ground
94	9L	DV_{DD2}	–	Internal power supply (+2.5 V)
95	9T	$MEMA_{15}$	O12	Address for flash memory/external device/CompactFlash (CFA5)
96	10L	$MEMA_{16}$	O12	Address for flash memory/external device/CompactFlash (CFA6)
97	10N	$MEMA_{17}$	O12	Address for flash memory/external device/CompactFlash (CFA7)
98	10R	DV_{DD}	–	Power supply (+3.3 V)
99	10P	$MEMA_{18}$	O12	Address for flash memory/external device/CompactFlash (CFA8)
100	10M	DGND	–	Ground
101	10T	$MEMA_{19}$	O12	Address for flash memory/external device/CompactFlash (CFA9)
102	11L	$MEMA_{20}$	O12	Address for flash memory/external device/CompactFlash (CFA10)
103	11N	FLCE0Z	O8	Chip enable for flash memory, Block 0
104	11R	FLCE1Z	IO8	Chip enable for flash memory, Block 1/GIO_{18}
105	11T	FL_EXOEZ	O8	Output enable for flash memory/external device/CompactFlash
106	11P	DGND	–	Ground
107	11M	FL_EXWEZ	O8	Write enable for flash memory/external device/CompactFlash
108	12T	FLWPZ	O8	Write protect for flash memory
109	12N	FLRP0Z	O8	Reset/deep power down for flash memory, Block 0
110	12R	FLRP1Z	IO8	Reset/deep power down for flash memory, Block 1/GIO_{19}
111	12P	EXCS0Z	O8	Chip select 0 for external device
112	13T	DV_{DD}	–	Power supply (+3.3 V)
113	13N	EXCS1Z	IO8	Chip select 1 for external device/GIO_{20}
114	13R	EXDACK0Z	IU	Data acknowledge 0 for external device
115	13P	EXDACK1Z	IO8U	Data acknowledge 1 for external device/GIO_{21}
116	14T	EXINTZ	IU	External device interrupt
117	15T	CFRDBY	IU	CompactFlash/SmartMedia READY/BUSY
118	14P	CFCD1Z	IO8U	CompactFlash/SmartMedia card detect signal 1/GIO_{22}
119	14R	CFCD2Z	IO8U	CompactFlash card detect signal 2/SmartMedia write protect detect/GIO_{23}
120	–	NC	–	Must be open.

PIN NO.	COORDINATE	SYMBOL	IO SYMBOL	DESCRIPTION
121	15R	CFWAITZ	IU	CompactFlash −WAIT signal
122	15P	CFREGZ	IO8	CompactFlash −REG signal
123	16R	DGND	–	Ground
124	14N	CFRST	IO8	CompactFlash reset signal (RESET)/SmartMedia chip enable (−CE)
125	15N	CFCE1Z	IO8	Card enable 1 for CompactFlash (−CE1)
126	16P	CFCE2Z	IO8	Card enable 2 for CompactFlash (−CE2)
127	14M	CFD_0	IO8U	Data I/O for CompactFlash/SmartMedia
128	16N	CFD_1	IO8U	
129	15M	DV_{DD}	–	Power supply (+3.3 V)
130	13M	CFD_2	IO8U	Data I/O for CompactFlash/SmartMedia
131	12M	CFD_3	IO8U	
132	16M	CFD_4	IO8U	
133	12L	DGND	–	Ground
134	14L	CFD_5	IO8U	Data I/O for CompactFlash/SmartMedia
135	15L	CFD_6	IO8U	
136	13L	CFD_7	IO8U	
137	11K	CFD_8	IO8U	Data I/O for CompactFlash/GIO_{24}
138	16L	CFD_9	IO8U	Data I/O for CompactFlash/GIO_{25}
139	12K	DV_{DD2}	–	Internal power supply (+2.5 V)
140	15K	CFD_{10}	IO8U	Data I/O for CompactFlash/GIO_{26}
141	14K	DGND	–	Ground
142	13K	TEST7Z	IU	Test (Must be open.)
143	11J	CFD_{11}	IO8U	Data I/O for CompactFlash/GIO_{27}
144	16K	CFD_{12}	IO8U	Data I/O for CompactFlash/GIO_{28}
145	12J	CFD_{13}	IO8U	Data I/O for CompactFlash/GIO_{29}
146	15J	DV_{DD}	–	Power supply (+3.3 V)
147	14J	CFD_{14}	IO8U	Data I/O for CompactFlash/GIO_{30}
148	13J	CFD_{15}	IO8U	Data I/O for CompactFlash/GIO_{31}
149	16J	CFA_0	IO8	Address for CompactFlash/read enable for SmartMedia (−RE)
150	11H	CFA_1	IO8	Address for CompactFlash/write enable for SmartMedia (−WE)
151	12H	CFA_2	IO8	Address for CompactFlash/write protect for SmartMedia (−WP)
152	15H	CFA_3	IO8	Address for CompactFlash/address latch enable for SmartMedia (ALE)
153	14H	DGND	–	Ground
154	16H	CFA_4	IO8	Address for CompactFlash/command latch enable for SmartMedia (CLE)
155	13H	GIO_0	IO8	General purpose I/O (+3.3 V)/PWM/CCD general purpose output
156	11G	GIO_1	IO8	
157	12G	GIO_2	IO8	
158	15G	DV_{DD2}	–	Internal power supply (+2.5 V)

PIN NO.	COORDINATE	SYMBOL	IO SYMBOL	DESCRIPTION
159	14G	GIO_3	IO8	General purpose I/O (+3.3 V)/PWM
160	16G	DV_{DD}	–	Power supply (+3.3 V)
161	13G	GIO_4	IO8	General purpose I/O (+3.3 V)/PWM
162	11F	GIO_5	IO8	
163	12F	GIO_6	IO8	
164	14F	DGND	–	Ground
165	15F	GIO_7	IO8	General purpose I/O (+3.3 V)/PWM
166	16F	GIO_8	IO8	
167	13F	GIO_9	IO8	General purpose I/O (+3.3 V)/PWM/TX_VPO output for USB (send data +)
168	16E	GIO_{10}	IO8	General purpose I/O (+3.3 V)/PWM/TX_VMO output for USB (send data –)
169	13E	GIO_{11}	IO8	General purpose I/O (+3.3 V)/PWM/TX_OE_N output for USB (send enable)
170	15E	TESTCLK	I	Ground
171	14E	GIO_{12}	IO8	General purpose I/O (+3.3 V)/PWM/SUSPEND_N output for USB (suspend request)
172	16D	GIO_{13}	IO8	General purpose I/O (+3.3 V)/PWM/RX_VPI input from USB (receive data +)
173	13D	GIO_{14}	IO8	General purpose I/O (+3.3 V)/PWM/RX_VMI input from USB (receive data –)
174	15D	GIO_{15}	IO8	General purpose I/O (+3.3 V)/PWM/RX_DATA input from USB (receive enable)
175	14D	RESETZ	IS	Reset
176	16C	DGND	–	Ground
177	16B	VB_1	–	Biased voltage output 1
178	14C	DI_{REF1}	DAI_{REF}	DAC reference current output 1
179	15C	DV_{REF1}	DAV_{REF}	DAC full scaled reference voltage input 1
180	–	NC	–	Must be open.
181	15B	YCOUT	DAI	NTSC/PAL composite/luminance analog output (1 Vp-p : must be connected to 75 Ω.)
182	14B	DAGND	–	Ground for DAC
183	15A	DAV_{DD}	–	Power supply for DAC (+2.5 V)
184	13C	COUT	DAI	NTSC/PAL composite/chrominance analog output (1 Vp-p : must be connected to 75 Ω)
185	13B	DV_{REF2}	DAV_{REF}	DAC full-scale reference voltage input 2
186	14A	DI_{REF2}	DAI_{REF}	DAC reference current output 2
187	12D	VB_2	–	Bias voltage output 2
188	13A	TGID	I	Identification pulse for color line of CCD signal from TG (High at R-line)
189	12C	DV_{DD}	–	Power supply (+3.3 V)

PIN NO.	COORDINATE	SYMBOL	IO SYMBOL	DESCRIPTION
190	12B	TGCLK	I	Pixel clock input from TG
191	12E	HD	IO8	Horizontal synchronization pulse for CCD
192	11D	VD	IO8	Vertical synchronization pulse for CCD
193	12A	DV_{DD2}	–	Internal power supply (+2.5 V)
194	11C	$CCDIN_0$	I	RGB input from CCD
195	11B	$CCDIN_1$	I	
196	11E	$CCDIN_2$	I	
197	10F	COMO	OSC	24 MHz crystal oscillator output
198	11A	COMI	IA	24 MHz crystal oscillator input (for communication)
199	10E	DGND	–	Ground
200	10C	$CCDIN_3$	I	RGB input from CCD
201	10B	DV_{DD}	–	Power supply (+3.3 V)
202	10D	$CCDIN_4$	I	RGB input from CCD
203	9F	$CCDIN_5$	I	
204	10A	$CCDIN_6$	I	
205	9E	$CCDIN_7$	I	
206	9B	$CCDIN_8$	I	
207	9C	$CCDIN_9$	I	
208	9D	$TGED_0$	IO8	Serial signal output for setting register of TG
209	9A	$TGED_1$	IO8	
210	8E	$TGED_2$	O8	
211	8D	ASDI	IU	Input data for audio serial I/F
212	8B	ASDO	O8	Output data for audio serial I/F
213	8C	TCLK	I	Master clock input for audio serial I/F
214	8F	DGND	–	Ground
215	8A	ASCLK	O8	Shift clock for audio serial I/F
216	7F	AXSYNCO	O8	Transmit synchronous signal for audio serial I/F
217	7E	ARSYNCO	O8	Receive synchronous signal for audio serial I/F
218	7B	DV_{DD}	–	Power supply (+3.3 V)
219	7C	SDI_1	I	Input data for asynchronous serial I/F
220	7D	DGND	–	Ground
221	7A	C24MI	IA	24.5454 MHz crystal oscillator input (system clock)
222	6F	C24MO	OSC	24.5454 MHz crystal oscillator output
223	6E	SDO_1	O8	Output data for asynchronous serial I/F
224	6B	DV_{DD}	–	Power supply (+3.3 V)
225	6C	$SCLK_0$	IO8U	Clock for synchronous serial I/F
226	6D	DGND	–	Ground
227	6A	SDI_0	I	Input data for synchronous serial I/F
228	5A	DV_{DD2}	–	Internal power supply (+2.5 V)
229	5D	C29MO	OSC	29.5 MHz crystal oscillator output
230	5B	C29MI	IA	29.5 MHz crystal oscillator input (for PAL)

PIN NO.	COORDINATE	SYMBOL	IO SYMBOL	DESCRIPTION
231	5C	SDO_0	O8	Output data for synchronous serial I/F
232	4A	$TESTCLK_2$	I	Input signal for test (Must be connected to ground.)
233	4D	ICEFIQZ	IU	FIQ interrupt input for ROMICE (Must be open during normal operation.)
234	4B	DV_{DD}	–	Power supply (+3.3 V)
235	4C	PLV_{DD}	–	Power supply for PLL (+2.5 V)
236	3A	PLGND	–	Ground for PLL
237	2A	PLV_{DD}	–	Power supply for PLL (+2.5 V)
238	3B	PLGND	–	Ground for PLL
239	3C	DGND	–	Ground
240	–	NC	–	Must be open.

I : Input pin
IS : Schmidt input pin
IU : Input pin with pull-up resistor
O8 : Output pin
O12 : Output pin
IO8 : Input/output pin
IO8U : Input/output pin with pull-up resistor
IO12 : Input/output pin
IO12U : Input/output pin with pull-up resistor
DAI : Analog output pin
DAV_{REF} : Analog input pin for DAC
DAI_{REF} : Analog output pin for DAC
IA : Input pin for oscillation
OSC : Output pin for oscillation

REMARKS :

PIN TYPE (MAX. OUTPUT CURRENT)	APPLICABLE PINS
+3.3 V I/O pin (12 mA) or output pin	MEMLDQM, MEMUDQM, MEMCLK, MEMWEZ, MEMCASZ, MEMRASZ, $MEMA_0$ to $MEMA_{20}$
+3.3 V I/O pin (8 mA) or output pin	$MEMCKE_1$ to $MEMCKE_3$, MEMCS0Z to MEMCS3Z, FLCE0Z to FLCE1Z, FL_EXOEZ, FL_EXWEZ, FLWPZ, FLRP0Z to FLRP1Z, EXCS0Z to EXCS1Z, CFREGZ, CFRST, CFCE1Z to CFCE2Z, CFA_0 to CFA_4, GIO_0 to GIO_{15}, HD, VD, $TGED_0$ to $TGED_2$, ASDO, ASCLK, AXSYNCO, ARSYNCO, SDO_1, SDO_0
+3.3 V I/O pin (12 mA, 98 kΩ pull-up resistor installed)	$MEMD_0$ to $MEMD_{31}$
+3.3 V I/O pin (8 mA, 98 kΩ pull-up resistor installed) or input pin	TEST1Z to TEST7Z, EXDACK0Z to EXDACK1Z, EXINTZ, CFRDBY, CFWAITZ, CFD_0 to CFD_{15}, ASDI, $SCLK_0$, ICEFIQZ

NOTES :

1. When an I/O pin is set to "input", take care not to let the pin to have a floating address.
2. Keep test pins TEST1Z to TEST7Z normally open.
3. I/O pins $MEMCKE_2$, $MEMCKE_3$, FLCE1Z, FLRP1Z, EXCS1Z and MEMCLK are set to "output" when reset (RESETZ input is Low level), while other I/O pins are "input".

FUNCTIONAL DESCRIPTION

Oscillation Circuit

The PLL included in the LR38666Y divides or passes through the doubled frequency of the quartz crystal connected to I/O pins, and provides it to the internal logic circuits as shown in **Fig.1** and **Fig.2**.

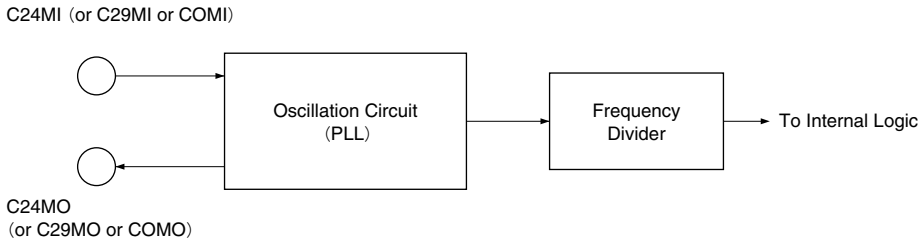


Fig. 1 Block Diagram of Oscillation Circuit

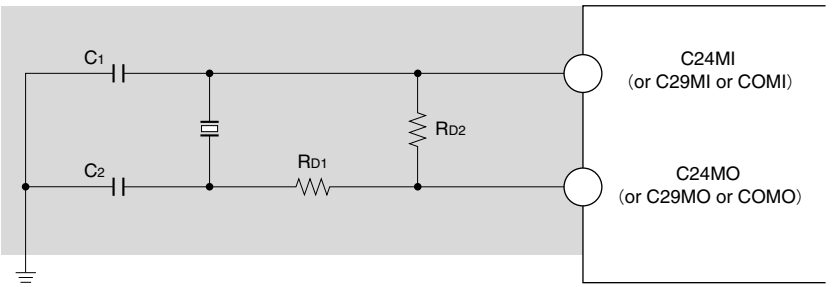


Fig. 2 Clock Input to Oscillation Circuit

Connection of Quartz Crystal (T_A = 0 to +70°C) : Example of Oscillation under Fundamental Frequencies

APPLICABLE PINS	FUNDAMENTAL FREQUENCY [MHz]	RECOMMENDED COEFFICIENT			
		C_1 [pF]	C_2 [pF]	R_{D1} [Ω]	R_{D2} [Ω]
C24MI, C24MO	24.5454	10	10	220	1 M
C29MI, C29MO	29.5000	10	10	220	1 M
COMI, COMO	24.0000	10	10	220	1 M

NOTES :

1. The oscillation circuit should be located as close to C24MI, C24MO (C29MI, C29MO, COMI, COMO) as possible.
2. Do not install other signal lines in the shaded area.
3. Perform due evaluation on the match between the LR38666Y and the quartz crystal.

Clock

The clock supplied to C24MI is doubled in frequency by an internal PLL and then is used as the main system clock. This clock is also used by the NTSC/PAL module in NTSC mode.

The clock supplied to C29MI is doubled in frequency by an internal PLL and then is used by the NTSC/PAL module in PAL mode only. The PAL mode allows clock oscillation. If the PAL mode is not used, fix the input level to High or Low. Note that, in NTSC mode, the accuracy of burst signals (deflection from the specified frequency) for video output depends on the accuracy of the clock supplied to C24MI. In PAL mode, the accuracy of burst signals (deflection from the specified frequency) for video output depends on the accuracy of the clock supplied to C29MI.

The clock supplied to COMI is doubled in frequency by an internal PLL and then is used by the UART, USART, USB and AUDIOIF modules. Only 24 MHz frequency can be used.

Note that the accuracy of the clock supplied to COMI influences the pulse width of the I/O signals.

Supply the clock (synchronized with CCD data) to TGCLK. Use as low a noise level signal as possible. Note that accuracy of the clock supplied to TCLK influences the accuracy of the clock of AUDIOIF.

If TCLK is not used, fix the input level to High or Low.

Power Supply Pins

Connect low noise power lines to the PLL power supply pin (PLV_{DD}), the PLL ground pin (PLGND), the DA converter power supply pin (DAV_{DD}) and the DA converter ground pin (DAGND).

Note that PLV_{DD} and DAV_{DD} are connected to DV_{DD2}, and PLGND and DAGND are connected to DGND inside the LR38666Y.

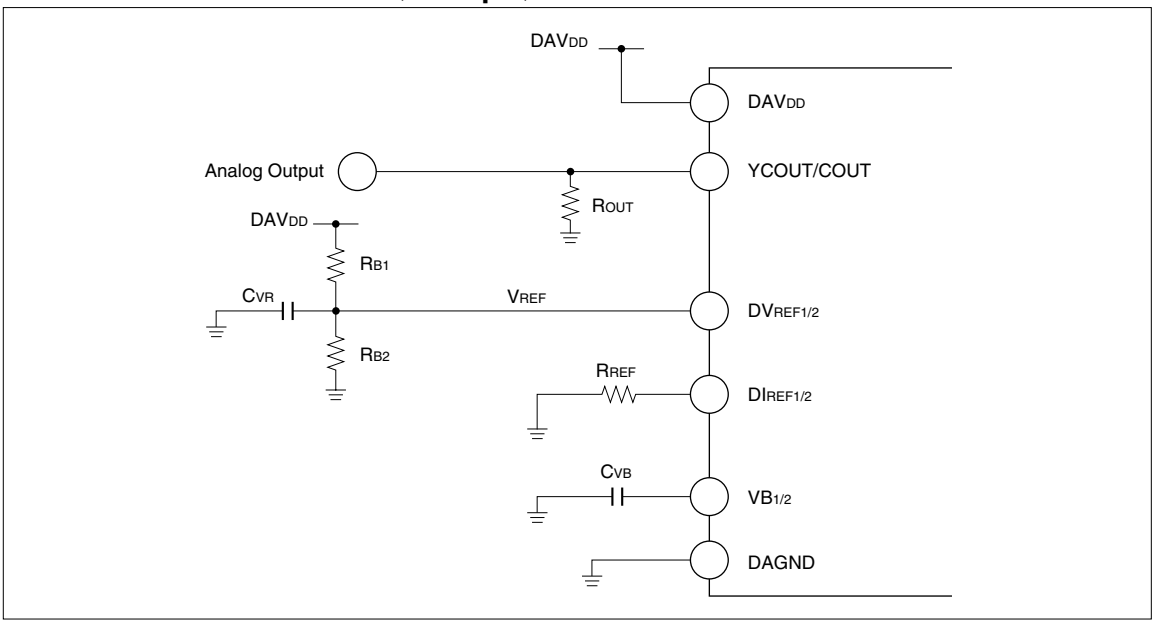
Power ON/OFF Sequence

Two power supplies are used with the LR38666Y. One (DV_{DD}) is used for I/O buffer and the other (DV_{DD2}) is used for the core logic circuits.

Power ON : Be sure to turn ON the internal power supply of DV_{DD2} first.

Power OFF : Be sure to turn OFF the I/O buffer of DV_{DD} first.

Recommended DAC Circuit (Example)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
I/O power supply voltage	DV_{DD}	−0.3 to +4.3	V
Internal power supply voltage	DV_{DD2}	−0.3 to +3.3	V
Input voltage	V_I	−0.3 to DV_{DD} + 0.3	V
Output voltage	V_O	−0.3 to DV_{DD} + 0.3	V
Storage temperature	T_{STG}	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power supply voltage	DV_{DD}	I/O digital power supply	3.0	3.3	3.6	V
	DV_{DD2}	Internal digital power supply	2.25	2.5	2.75	V
	DAV_{DD}	Analog power supply	2.25	2.5	2.75	V
Operating temperature	T_{OPR}		0	+25	+70	°C
Operating frequency	f_{OPR}	Maximum operating frequency		49.0908		MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics

(DV_{DD} = 3.3 V, DV_{DD2} = 2.5 V, T_A = 0 to +70˚C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}				0.2 DV_{DD}	V	1
Input "High" voltage	V_{IH}		0.8 DV_{DD}			V	
Positive trigger voltage	V_{T^+}		1.37			V	2
Negative trigger voltage	V_{T^-}				1.33	V	
Hysteresis	$V_{T^+} - V_{T^-}$		0.2			V	
Input leakage current	I_I	V_{IN} = 0 V to DV_{DD}	−1.0		+1.0	µA	3
		V_{IN} = DV_{DD} [with pull-up 98 kΩ]	−5.0		+5.0	µA	4
Input "Low" current	I_{IL}	V_{IN} = 0 V [with pull-up 98 kΩ]		−35		µA	4
Output "Low" voltage 1	V_{OL1}	I_{OL} = 8 mA			0.5	V	5
Output "High" voltage 1	V_{OH1}	I_{OH} = −8 mA	DV_{DD} – 0.5			V	
Output "Low" voltage 2	V_{OL2}	I_{OL} = 12 mA			0.5	V	6
Output "High" voltage 2	V_{OH2}	I_{OH} = −12 mA	DV_{DD} – 0.5			V	
Resolution	RES			9		Bit	7
Linearity error	EL	V_{REF} = 1.24 V R_{REF} = 4.8 kΩ R_{OUT} = 75 Ω C_{VB} = 0.1 µF	−3.0		+6.0	LSB	
Differential linearity error	ED		−1.0		+1.0	LSB	
Full-scale current	IFS			16.5		mA	
Output load resistance	R_{OUT}			75		Ω	
Reference voltage	V_{REF}		1.12	1.24	1.36	V	8
Reference resistance	R_{REF}			4.8		kΩ	9
Oscillation frequency 1	F_{OSC1}			24.5454		MHz	10
Oscillation frequency 2	F_{OSC2}			29.5000		MHz	11
Oscillation frequency 3	F_{OSC3}			24.0000		MHz	12
Supply current (a) (DV_{DD})	I_{DDa}	Input image display mode : 1/4 VGA		55		mA	13
Supply current (a) (DV_{DD2}, DAV_{DD}, PLV_{DD})	I_{DD2a}			115		mA	
Supply current (b) (DV_{DD})	I_{DDb}	Input image display & capture image mode : VGA		70		mA	14
Supply current (b) (DV_{DD2}, DAV_{DD}, PLV_{DD})	I_{DD2b}			125		mA	
Standby current (DV_{DD})	I_{DDSB}	waiting for ARM operation with 1/4 clock		25		mA	15
Standby current (DV_{DD2}, DAV_{DD}, PLV_{DD})	I_{DD2SB}			15		mA	

NOTES :

1. Applicable to IO symbols I, IU, IO8, IO8U, IO12, IO12U.
2. Applicable to IO symbol IS.
3. Applicable to IO symbols I, IO8, IO12, IS.
4. Applicable to IO symbols IU, IO8U, IO12U.
5. Applicable to IO symbols O8, IO8, IO8U.
6. Applicable to IO symbols O12, IO12, IO12U.
7. Applicable to IO symbol DAI.
8. Applicable to IO symbol DAV_{REF}.
9. External resistance value. Applicable to IO symbol DAI_{REF}.
10. Applicable to IO symbols IA (C24MI), OSC (C24MO).
11. Applicable to IO symbols IA (C29MI), OSC (C29MO).
12. Applicable to IO symbols IA (COMI), OSC (COMO).
13. Supply voltage DV_{DD} : 3.3 V, DV_{DD2} : 2.5 V
    Measuring conditions : 1 310 k-pixel CCD is used.
    CCD1 output image size 640 x 240,
    CCD2 output image size 320 x 240,
    16 bits external bus width, Local SRAM is not used.
    Always active modules :
    ARM, CCD1, CCD2, VENC, MEMC, DMAC
    Inactive modules :
    JPEG, SRAM, USART, UART, USB, RESIZE, PLL (for PAL), AUDIOIF, GIO
14. Supply voltage DV_{DD} : 3.3 V, DV_{DD2} : 2.5 V
    Measuring conditions : 1 310 k-pixel CCD is used.
    CCD1 output image size 640 x 480,
    CCD2 output image size 640 x 480,
    16 bits external bus width, Local SRAM is not used.
    Always active modules :
    ARM, CCD1, CCD2, JPEG, VENC, MEMC, DMAC
    Inactive modules :
    SRAM, USART, UART, USB, RESIZE, PLL (for PAL), AUDIOIF, GIO
15. Supply voltage DV_{DD} : 3.3 V, DV_{DD2} : 2.5 V
    Always active modules :
    ARM, MEMC, DMAC (Internal clock is divided into 1/4.)
    Inactive modules :
    JPEG, CCD1, CCD2, VENC, SRAM, USART, UART, USB, RESIZE, PLL (for PAL), AUDIOIF, GIO

AC Characteristics

SDRAM INTERFACE TIMING

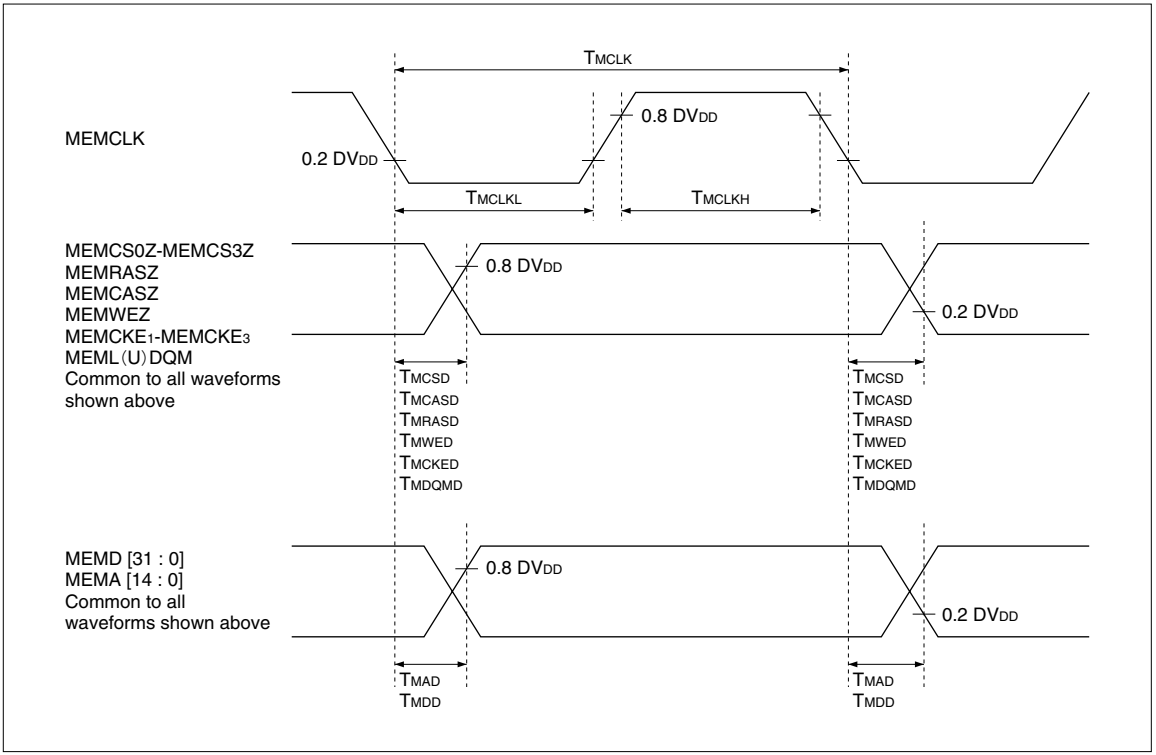


Fig. 3 SDRAM Output Timing

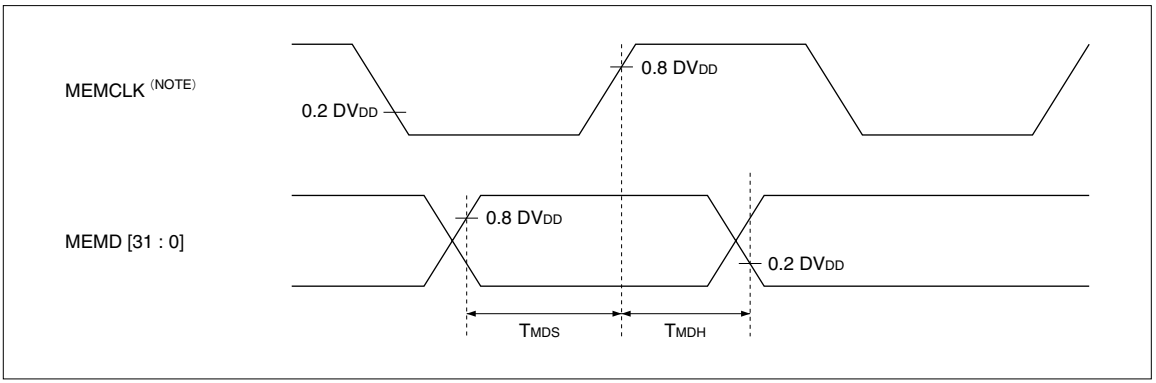


Fig. 4 SDRAM Input Timing

NOTE : MEMCLK is also used as the data latch clock inside the LR38666Y. Check the waveform of the incoming MEMCLK signal for no distortion.

(DV_{DD} = 3.3 V, DV_{DD2} = 2.5 V, C24MI = 24.5454 MHz, T_A = 0 to +70˚C)

PARAMETER	SYMBOL	CONDITIONS			UNIT	NOTE
		MIN.	TYP.	MAX.		
Clock cycle	T_{MCLK}	20			ns	2
Pulse width (High)	T_{MCLKH}	9			ns	2
Pulse width (Low)	T_{MCLKL}	9			ns	2
Chip select delay	T_{MCSD}	0		7	ns	1
MEMRASZ output delay	T_{MRASD}	0		7	ns	2
MEMCASZ output delay	T_{MCASD}	0		7	ns	2
Write enable delay	T_{MWED}	0		7	ns	2
Addressing delay	T_{MAD}	0		7	ns	2
$MEMCKE_1$ to $MEMCKE_3$ output delay	T_{MCKED}	0		7	ns	1
MEML(U)DQM output delay	T_{MDQMD}	0		7	ns	2
Data output delay (write cycle)	T_{MDD}	0		7	ns	2
Data setup delay (read cycle)	T_{MDS}	10			ns	
Data hold delay (read cycle)	T_{MDH}	3			ns	

NOTES :

1. Output load capacity C_L = 10 pF
2. Output load capacity C_L = 50 pF

FLASH MEMORY INTERFACE TIMING

• Read/write timing

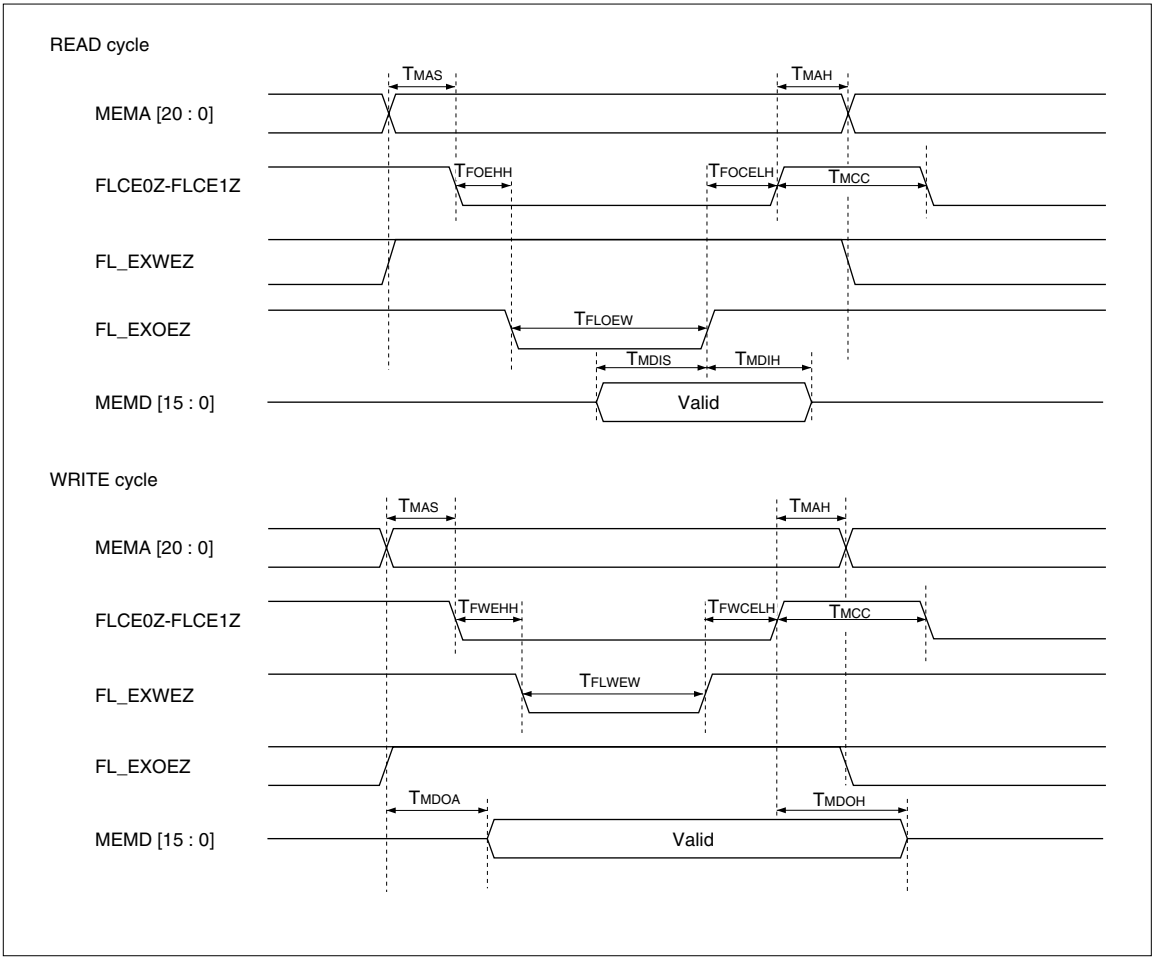


Fig. 5 Flash Memory Read/Write Cycle

(DV_{DD} = 3.3 V, DV_{DD2} = 2.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
Address output setup time (relative to the falling edge of FLCE0Z/1Z)	T_{MAS}	$T_{CNT0} - 5$		ns	2
		$T_{CNT5} - 5$			
Address output hold time (relative to the rising edge of FLCE0Z/1Z)	T_{MAH}	$T_{CNT4} - 5$		ns	2
		$T_{CNT9} - 5$			
Minimum "High" period of FLCE0Z/1Z	T_{MCC}	α		ns	1
"High" hold time of FL_EXOEZ (relative to the falling edge of FLCE0Z/1Z)	T_{FOEHH}	$T_{CNT1} - 5$	$T_{CNT1} + 5$	ns	2
"Low" pulse width of FL_EXOEZ	T_{FLOEW}	$T_{CNT2} - 5$	$T_{CNT2} + 5$	ns	2
"Low" hold time of FLCE0Z/1Z (relative to the rising edge of FL_EXOEZ)	T_{FOCELH}	$T_{CNT3} - 5$	$T_{CNT3} + 5$	ns	1
"High" hold time of FL_EXWEZ (relative to the falling edge of FLCE0Z/1Z)	T_{FWEHH}	$T_{CNT6} - 5$	$T_{CNT6} + 5$	ns	2
"Low" pulse width of FL_EXWEZ	T_{FLWEW}	$T_{CNT7} - 5$	$T_{CNT7} + 5$	ns	2
"Low" hold time of FLCE0Z/1Z (relative to the rising edge of FL_EXWEZ)	T_{FWCELH}	$T_{CNT8} - 5$	$T_{CNT8} + 5$	ns	1
MEMD input setup time (relative to the rising edge of FL_EXOEZ)	T_{MDIS}	$2T_{MCLK} - 5$		ns	
MEMD input hold time (relative to the rising edge of FL_EXOEZ)	T_{MDIH}	0		ns	
MEMD output delay (relative to the point at which the status of MEMA changes)	T_{MDOA}	$2T_{MCLK} - 5$	$2T_{MCLK} + 5$	ns	2
MEMD output hold time (relative to the rising edge of FLCE0Z/1Z)	T_{MDOH}	$T_{CNT9} + 2T_{MCLK} - 5$	$T_{CNT9} + 2T_{MCLK} + 5$	ns	2

NOTES :

1. Output load capacity C_L = 15 pF
2. Output load capacity C_L = 50 pF

T_{CNT0}, T_{CNT1}, T_{CNT2}, T_{CNT3}, T_{CNT4}, T_{CNT5}, T_{CNT6}, T_{CNT7}, T_{CNT8}, T_{CNT9} and α each has a value within the following range depending on the register setting. T_{MAS} corresponds to T_{CNT0} in read cycle and T_{CNT5} in write cycle, T_{MAH} corresponds to T_{CNT4} in read cycle and T_{CNT9} in write cycle.

T_{CNT0} : $1T_{MCLK}$ to $3T_{MCLK}$, T_{CNT1} : $0T_{MCLK}$ to $7T_{MCLK}$, T_{CNT2} : $3T_{MCLK}$ to $15T_{MCLK}$, T_{CNT3} : $0T_{MCLK}$ to $3T_{MCLK}$, T_{CNT4} : $1T_{MCLK}$ to $3T_{MCLK}$, T_{CNT5} : $1T_{MCLK}$ to $3T_{MCLK}$, T_{CNT6} : $0T_{MCLK}$ to $7T_{MCLK}$, T_{CNT7} : $3T_{MCLK}$ to $15T_{MCLK}$, T_{CNT8} : $0T_{MCLK}$ to $3T_{MCLK}$, T_{CNT9} : $1T_{MCLK}$ to $3T_{MCLK}$

α : Min. "High" period between read cycles : $3T_{MCLK} \leq (T_{CNT0} + T_{CNT4} + 1T_{MCLK}) \leq 7T_{MCLK}$

Min. "High" period from read cycle to write cycle : $3T_{MCLK} \leq (T_{CNT4} + T_{CNT5} + 1T_{MCLK}) \leq 7T_{MCLK}$

Min. "High" period from write cycle to read cycle : $3T_{MCLK} \leq (T_{CNT0} + T_{CNT9} + 1T_{MCLK}) \leq 7T_{MCLK}$

Min. "High" period between write cycles : $3T_{MCLK} \leq (T_{CNT5} + T_{CNT9} + 1T_{MCLK}) \leq 7T_{MCLK}$

• Flash memory hard reset timing

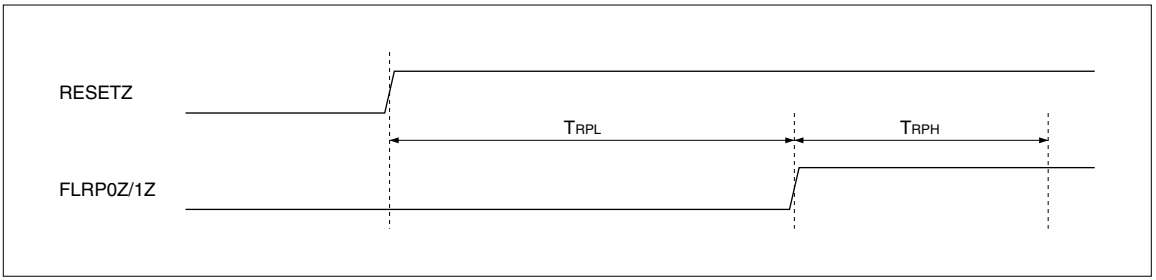


Fig. 6 Flash Memory Reset Cycle

(DVDD = 3.3 V, DVDD2 = 2.5 V, TA = 0 to +70˚C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
"Low" pulse period of FLRP0Z/1Z (relative to the rising edge of RESETZ)	TRPL	11TMCLK	12TMCLK	ns	1
"High" pulse period of FLRP0Z/1Z (relative to the rising edge of FLR0/1Z)	TRPH	98TMCLK		ns	1, 2

NOTES :

1. Output load capacity CL = 15 pF
2. When the internal bus of the LR38666Y accesses to the flash memory during TRPH, it is made to wait.

• Flash memory initialization timing

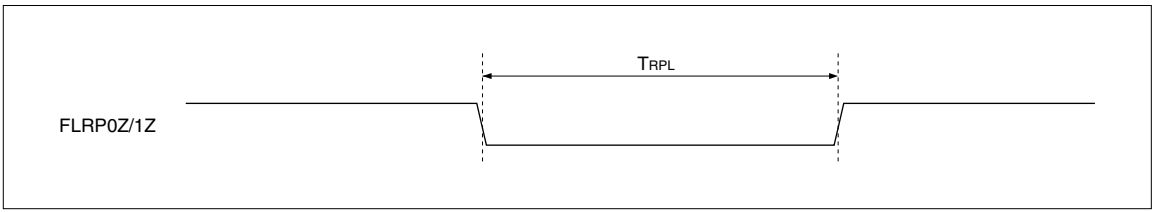


Fig. 7 Flash Memory Initialization Cycle

(DVDD = 3.3 V, DVDD2 = 2.5 V, TA = 0 to +70˚C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
"Low" pulse period of FLRP0Z/1Z	TRPL	12TMCLK	12TMCLK	ns	1

NOTE :

1. Output load capacity CL = 15 pF

INTERFACE TIMING OF OTHER DEVICES

• S-type device timing

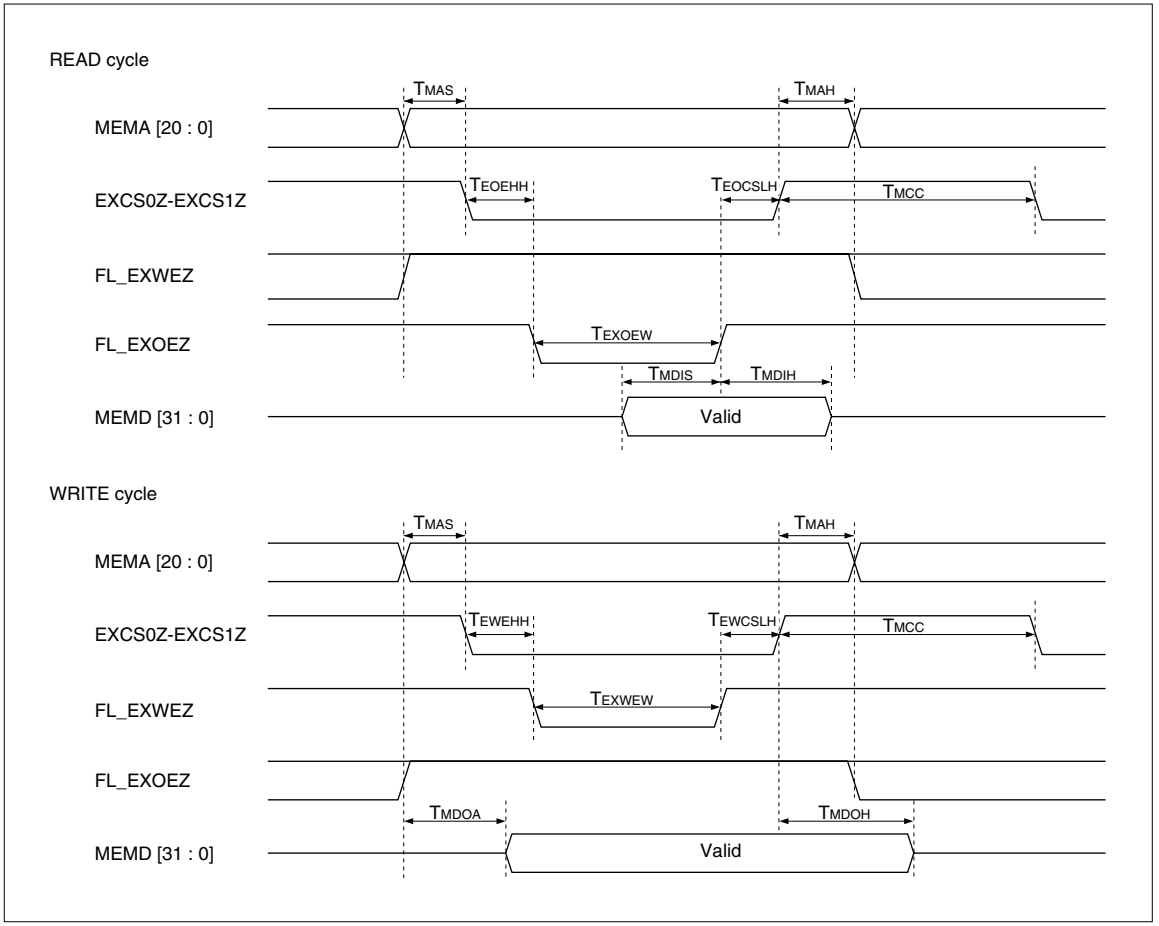


Fig. 8 S-type Device Read/Write Cycle

(DV_{DD} = 3.3 V, DV_{DD2} = 2.5 V, T_A = −10 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
Output setup period of MEMA (relative to the falling edge of EXCS0Z/1Z)	T_{MAS}	T_{CNT00} − 5 T_{CNT05} − 5		ns	2
Output hold period of MEMA (relative to the rising edge of EXCS0Z/1Z)	T_{MAH}	T_{CNT04} − 5 T_{CNT09} − 5		ns	2
Minimum "High" period of EXCS0Z/1Z	T_{MCC}	α		ns	1
"High" hold period of FL_EXOEZ (relative to the falling edge of EXCS0Z/1Z)	T_{EOEHH}	T_{CNT01} − 5	T_{CNT01} + 5	ns	2
"Low" pulse width of FL_EXOEZ	T_{EXOEW}	T_{CNT02} − 5	T_{CNT02} + 5	ns	2
"Low" hold period of EXCS0Z/1Z (relative to the rising edge of FL_EXOEZ)	T_{EWCSLH}	T_{CNT03} − 5	T_{CNT03} + 5	ns	1
"High" hold period of FL_EXWEZ (relative to the falling edge of EXCS0Z/1Z)	T_{EWEHH}	T_{CNT06} − 5	T_{CNT06} + 5	ns	2
"Low" pulse width of FL_EXWEZ	T_{EXWEW}	T_{CNT07} − 5	T_{CNT07} + 5	ns	2
"Low" hold period of EXCS0Z/1Z (relative to the rising edge of FL_EXWEZ)	T_{EWCSLH}	T_{CNT08} − 5	T_{CNT08} + 5	ns	1
Input setup period of MEMD (relative to the rising edge of FL_EXOEZ)	T_{MDIS}	2T_{MCLK} − 5		ns	
Input hold period of MEMD (relative to the rising edge of FL_EXOEZ)	T_{MDIH}	0		ns	
Output delay period of MEMD (relative to MEMA)	T_{MDOA}	2T_{MCLK} − 5	2T_{MCLK} + 5	ns	2
Output hold period of MEMD (relative to the rising edge of EXCS0Z/1Z)	T_{MDOH}	T_{CNT09} + 2T_{MCLK} − 5	T_{CNT09} + 2T_{MCLK} + 5	ns	2

NOTES :

1. Output load capacity C_L = 15 pF
2. Output load capacity C_L = 50 pF

T_{CNT00}, T_{CNT01}, T_{CNT02}, T_{CNT03}, T_{CNT04}, T_{CNT05}, T_{CNT06}, T_{CNT07}, T_{CNT08}, T_{CNT09} and α each has a value within the following range depending on the register setting.

T_{MAS} corresponds to T_{CNT00} in read cycle and T_{CNT05} in write cycle, and T_{CNT04} in read cycle and T_{CNT09} in write cycle.

T_{CNT00} : 1T_{MCLK} to 3T_{MCLK}, T_{CNT01} : 0T_{MCLK} to 3T_{MCLK}, T_{CNT02} : 3T_{MCLK} to 15T_{MCLK}, T_{CNT03} : 0T_{MCLK} to 7T_{MCLK}, T_{CNT04} : 1T_{MCLK} to 7T_{MCLK}, T_{CNT05} : 1T_{MCLK} to 3T_{MCLK}, T_{CNT06} : 0T_{MCLK} to 3T_{MCLK}, T_{CNT07} : 3T_{MCLK} to 15T_{MCLK}, T_{CNT08} : 0T_{MCLK} to 7T_{MCLK}, T_{CNT09} : 1T_{MCLK} to 7T_{MCLK}

α : Min. "High" period between read cycles : 3T_{MCLK} ≤ (T_{CNT00} + T_{CNT04} + 1T_{MCLK}) ≤ 11T_{MCLK}

Min. "High" period from read cycle to write cycle : 3T_{MCLK} ≤ (T_{CNT04} + T_{CNT05} + 1T_{MCLK}) ≤ 11T_{MCLK}

Min. "High" period from write cycle to read cycle : 3T_{MCLK} ≤ (T_{CNT00} + T_{CNT09} + 1T_{MCLK}) ≤ 11T_{MCLK}

Min. "High" period between write cycles : 3T_{MCLK} ≤ (T_{CNT05} + T_{CNT09} + 1T_{MCLK}) ≤ 11T_{MCLK}

• I-type timing

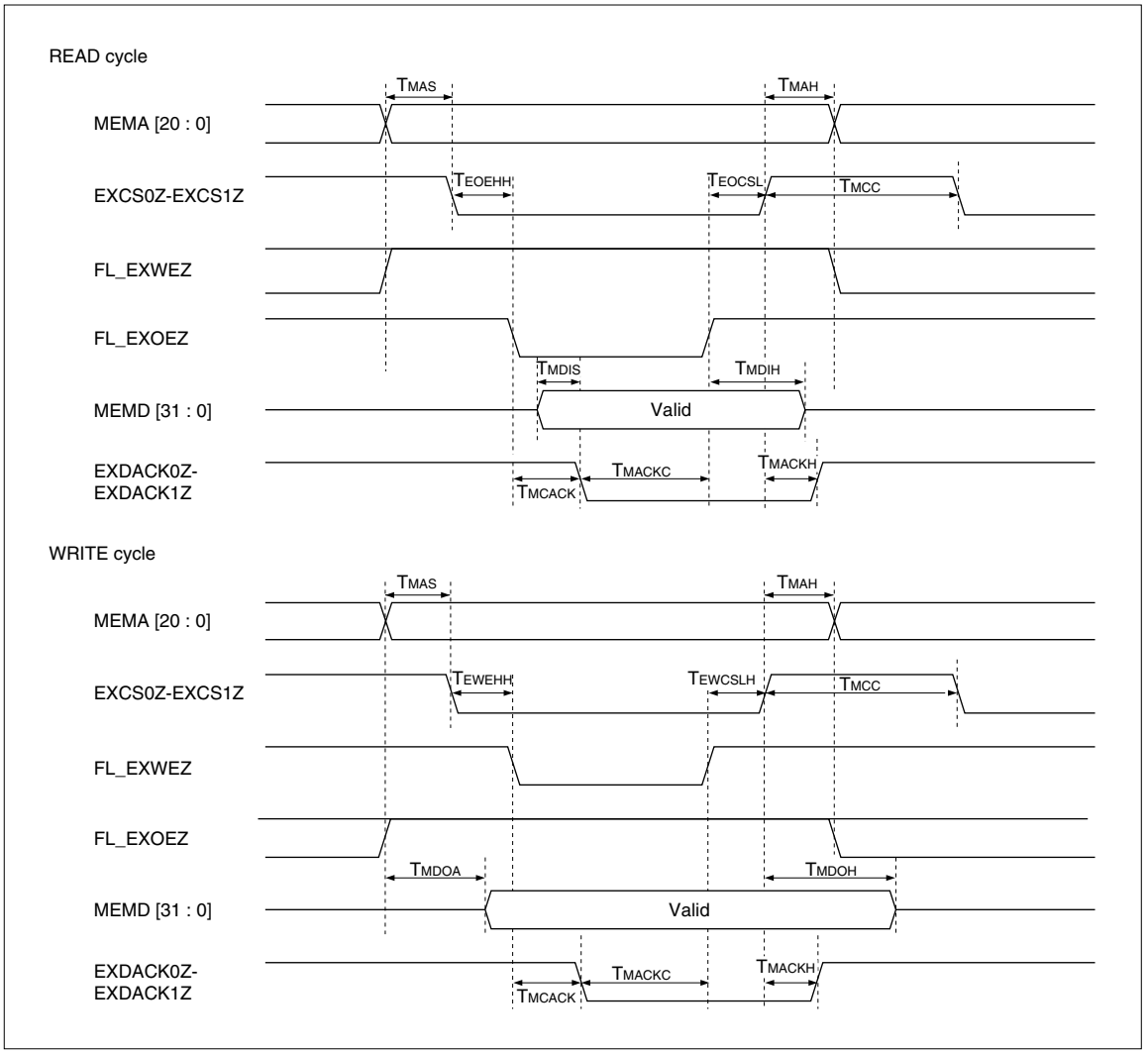


Fig. 9 I-type Read/Write Cycle

NOTE :

It is able to invert the polarity of EXDACK0Z/1Z by internal register.

(DV_{DD} = 3.3 V, DV_{DD2} = 2.5 V, T_A = −10 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
Output setup period of MEMA (relative to the falling edge of EXCS0Z/1Z)	T_{MAS}	T_{CNT10} − 5 T_{CNT14} − 5		ns	2
Output hold period of MEMA (relative to the rising edge of EXCS0Z/1Z)	T_{MAH}	T_{CNT13} − 5 T_{CNT17} − 5		ns	2
Minimum "High" period of EXCS0Z/1Z	T_{MCC}	α		ns	1
"High" hold period of FL_EXOEZ (relative to the falling edge of EXCS0Z/1Z)	T_{EOEHH}	T_{CNT11} − 5	T_{CNT11} + 5	ns	2
"Low" hold period of EXCS0Z/1Z (relative to the rising edge of FL_EXOEZ)	T_{EOCSLH}	T_{CNT12} − 5	T_{CNT12} + 5	ns	1
"High" hold period of FL_EXWEZ (relative to the falling edge of EXCS0Z/1Z)	T_{EWEHH}	T_{CNT15} − 5	T_{CNT15} + 5	ns	2
"Low" hold period of EXCS0Z/1Z (relative to the rising edge of FL_EXWEZ)	T_{EWCSLH}	T_{CNT16} − 5	T_{CNT16} + 5	ns	1
Input setup period of MEMD (relative to the falling edge of EXDACK0Z/1Z)	T_{MDIS}	0		ns	
Input hold period of MEMD (relative to the rising edge of FL_EXOEZ)	T_{MDIH}	0		ns	
Output delay period of MEMD (relative to MEMA)	T_{MDOA}	2T_{MCLK} − 5	2T_{MCLK} + 5	ns	2
Output hold period of MEMD (relative to the rising edge of EXCS0Z/1Z)	T_{MDOH}	T_{CNT17} + 2T_{MCLK} − 5	T_{CNT17} + 2T_{MCLK} + 5	ns	2
Setup period of EXDACK0Z/1Z (relative to the falling edge of FL_EXOEZ, FL_EXWEZ)	T_{MCACK}	0		ns	
Rising period of FL_EXOEZ/FL_EXWEZ (relative to the falling edge of EXDACK0Z/1Z)	T_{MACKC}	2T_{MCLK} − 5	3T_{MCLK} + 5	ns	2
Hold period of EXDACK0Z/1Z (relative to the rising edge of EXCS0Z/1Z)	T_{MACKH}	0		ns	

NOTES :

1. Output load capacity C_L = 15 pF
2. Output load capacity C_L = 50 pF

T_{CNT10}, T_{CNT11}, T_{CNT12}, T_{CNT13}, T_{CNT14}, T_{CNT15}, T_{CNT16}, T_{CNT17}, and α each has a value within the following range depending on the register setting. T_{MAS} corresponds to T_{CNT10} in read cycle and T_{CNT14} in write cycle. T_{MAH} corresponds to T_{CNT13} in read cycle and T_{CNT17} in write cycle.

T_{CNT10} : 1T_{MCLK} to 3T_{MCLK}, T_{CNT11} : 0T_{MCLK} to 3T_{MCLK}, T_{CNT12} : 0T_{MCLK} to 3T_{MCLK}, T_{CNT13} : 1T_{MCLK} to 3T_{MCLK}, T_{CNT14} : 1T_{MCLK} to 3T_{MCLK}, T_{CNT15} : 0T_{MCLK} to 3T_{MCLK}, T_{CNT16} : 0T_{MCLK} to 3T_{MCLK}, T_{CNT17} : 1T_{MCLK} to 3T_{MCLK}

α : Min. "High" period between read cycles : 3T_{MCLK} ≤ (T_{CNT10} + T_{CNT13} + 1T_{MCLK}) ≤ 7T_{MCLK}

Min. "High" period from read cycle to write cycle : 3T_{MCLK} ≤ (T_{CNT13} + T_{CNT14} + 1T_{MCLK}) ≤ 7T_{MCLK}

Min. "High" period from write cycle to read cycle : 3T_{MCLK} ≤ (T_{CNT10} + T_{CNT17} + 1T_{MCLK}) ≤ 7T_{MCLK}

Min. "High" period between write cycles : 3T_{MCLK} ≤ (T_{CNT14} + T_{CNT17} + 1T_{MCLK}) ≤ 7T_{MCLK}

• M-type timing

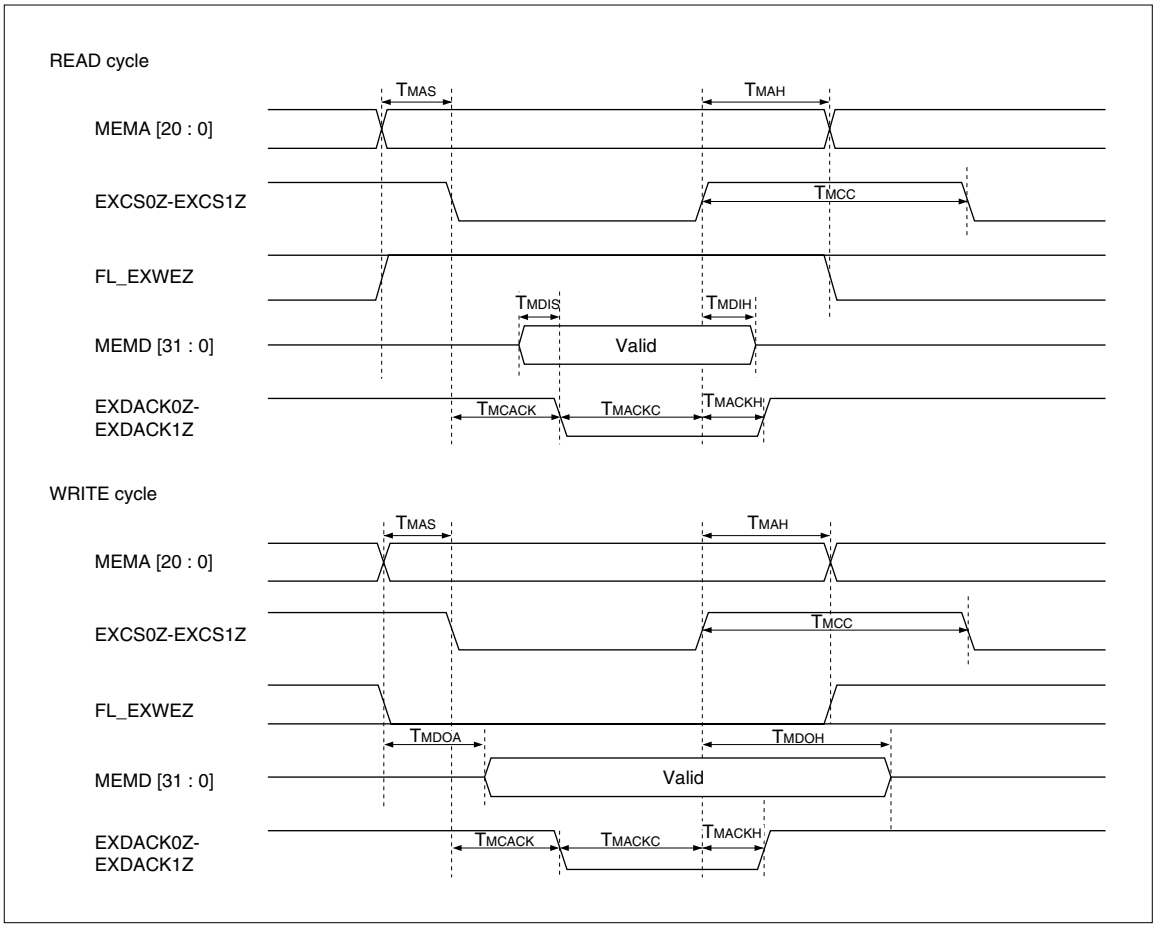


Fig. 10 M-type Read/Write Cycle

NOTE :

It is able to invert the polarity of EXDACK0Z/1Z by internal register.

(DV_{DD} = 3.3 V, DV_{DD2} = 2.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
Output setup period of MEMA (relative to the falling edge of EXCS0Z/1Z)	T_{MAS}	T_{CNT20} – 5 T_{CNT22} – 5		ns	2
Output hold period of MEMA (relative to the rising edge of EXCS0Z/1Z)	T_{MAH}	T_{CNT21} – 5 T_{CNT23} – 5		ns	2
Minimum "High" period of EXCS0Z/1Z	T_{MCC}	α		ns	1
Input setup period of MEMD (relative to the falling edge of EXDACKZ)	T_{MDIS}	0		ns	
Input hold period of MEMD (relative to the rising edge of EXCS0Z/1Z)	T_{MDIH}	0		ns	
Output delay period of MEMD (relative to MEMA)	T_{MDOA}	$2T_{MCLK}$ – 5	$2T_{MCLK}$ + 5	ns	2
Output hold period of MEMD (relative to the rising edge of EXCS0Z/1Z)	T_{MDOH}	T_{CNT23} + $2T_{MCLK}$ – 5	T_{CNT23} + $2T_{MCLK}$ + 5	ns	2
Setup period of EXDACK0Z/1Z (relative to the falling edge of EXCS0Z/1Z)	T_{MCACK}	0		ns	
Rising period of EXCS0Z/1Z (relative to the falling edge of EXDACK0Z/1Z)	T_{MACKC}	$2T_{MCLK}$ – 5	$3T_{MCLK}$ + 5	ns	1
Hold period of EXDACK0Z/1Z (relative to the rising edge of EXCS0Z/1Z)	T_{MACKH}	0		ns	

NOTES :

1. Output load capacity C_L = 15 pF
2. Output load capacity C_L = 50 pF

T_{CNT20}, T_{CNT21}, T_{CNT22}, T_{CNT23}, and α each has a value within the following range depending on the register setting. T_{MAS} corresponds to T_{CNT20} in read cycle and T_{CNT22} in write cycle, and T_{MAH} corresponds to T_{CNT21} in read cycle and T_{CNT23} in write cycle.

T_{CNT20} : $1T_{MCLK}$ to $3T_{MCLK}$, T_{CNT21} : $1T_{MCLK}$ to $3T_{MCLK}$, T_{CNT22} : $1T_{MCLK}$ to $3T_{MCLK}$, T_{CNT23} : $1T_{MCLK}$ to $3T_{MCLK}$

α : Min. "High" period between read cycles : $3T_{MCLK} \leq (T_{CNT20} + T_{CNT21} + 1T_{MCLK}) \leq 7T_{MCLK}$

Min. "High" period from read cycle to write cycle : $3T_{MCLK} \leq (T_{CNT21} + T_{CNT22} + 1T_{MCLK}) \leq 7T_{MCLK}$

Min. "High" period from write cycle to read cycle : $3T_{MCLK} \leq (T_{CNT20} + T_{CNT23} + 1T_{MCLK}) \leq 7T_{MCLK}$

Min. "High" period between write cycles : $3T_{MCLK} \leq (T_{CNT22} + T_{CNT23} + 1T_{MCLK}) \leq 7T_{MCLK}$

• CompactFlash attribute memory access timing

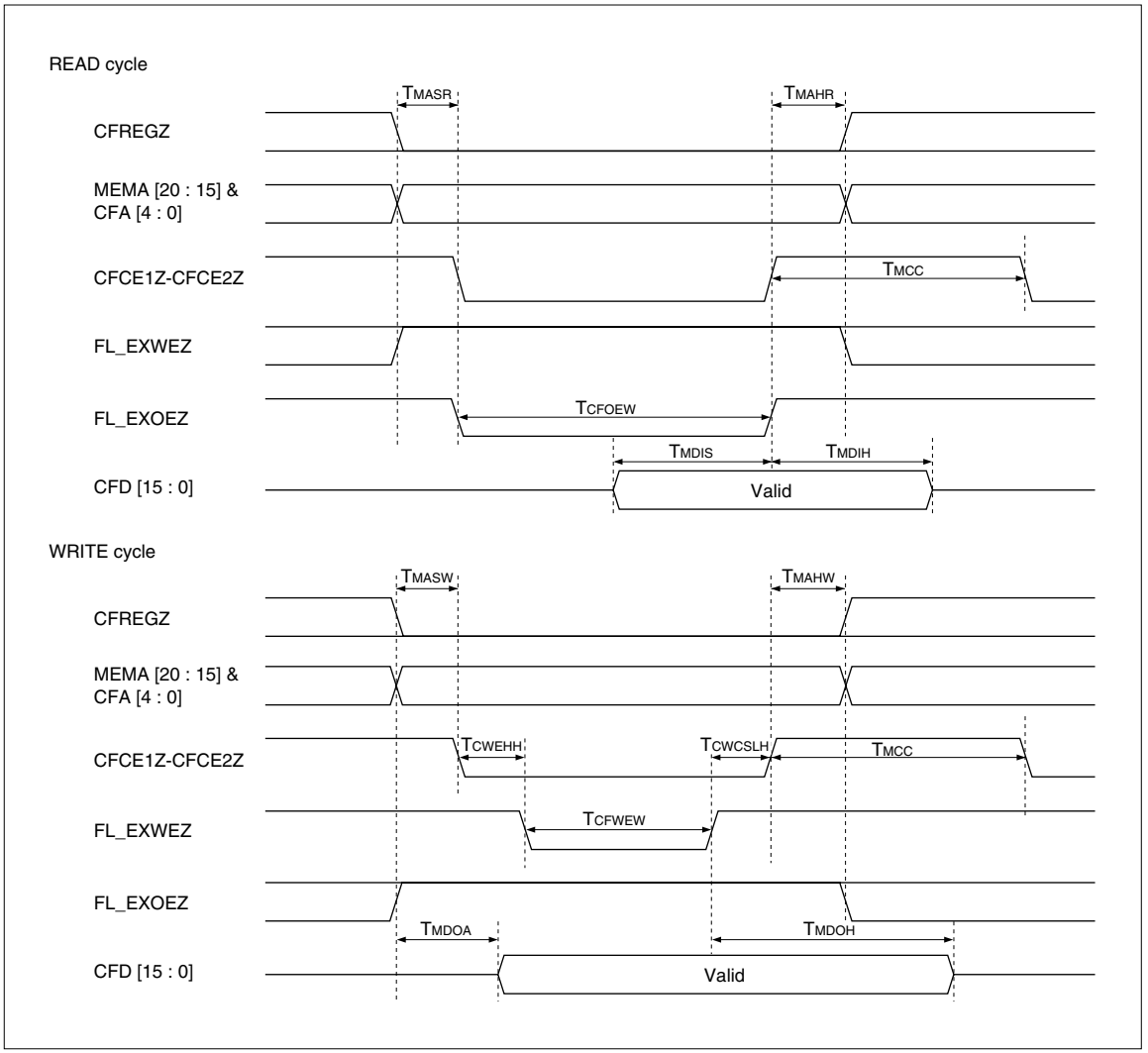


Fig. 11 CompactFlash Attribute Memory Read/Write Cycle

(DV_{DD} = 3.3 V, DV_{DD2} = 2.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
Output setup period of MEMA [20 : 15] & CFA at reading (relative to the falling edge of CFCE1Z/2Z)	T_{MASR}	$2T_{MCLK}$ – 5		ns	2
Output setup period of MEMA [20 : 15] & CFA at writing (relative to the falling edge of CFCE1Z/2Z)	T_{MASW}	T_{MCLK} – 5		ns	2
Output hold period of MEMA [20 : 15] & CFA at reading (relative to the rising edge of CFCE1Z/2Z)	T_{MAHR}	$3T_{MCLK}$ – 5		ns	2
Output hold period of MEMA [20 : 15] & CFA at writing (relative to the rising edge of CFCE1Z/2Z)	T_{MAHW}	T_{MCLK} – 5		ns	2
Minimum "High" period of CFCE1Z/2Z	T_{MCC}	$3T_{MCLK}$ – 5		ns	1
"Low" pulse width of FL_EXOEZ	T_{CFOEW}	$17T_{MCLK}$ – 5	$17T_{MCLK}$ + 5	ns	1
"High" hold period of FL_EXWEZ (relative to the falling edge of CFCE1Z/2Z)	T_{CWEHH}	$2T_{MCLK}$ – 5	$2T_{MCLK}$ + 5	ns	1
"Low" pulse width of FL_EXWEZ	T_{CFWEW}	$8T_{MCLK}$ – 5	$8T_{MCLK}$ + 5	ns	1
"Low" hold period of CFCE1Z/2Z (relative to the rising edge of FL_EXWEZ)	T_{CWCSLH}	$2T_{MCLK}$ – 5	$2T_{MCLK}$ + 5	ns	1
Input setup period of CFD (relative to the rising edge of FL_EXOEZ)	T_{MDIS}	$2T_{MCLK}$ – 5		ns	
Input hold period of CFD (relative to the rising edge of FL_EXOEZ)	T_{MDIH}	0		ns	
Output delay period of CFD (relative to MEMA [20 : 15] & CFA)	T_{MDOA}	$2T_{MCLK}$ – 5	$2T_{MCLK}$ + 5	ns	1
Output hold period of CFD (relative to the rising edge of FL_EXWEZ)	T_{MDOH}	$5T_{MCLK}$ – 5	$5T_{MCLK}$ + 5	ns	1

NOTES :

1. Output load capacity C_L = 50 pF
2. MEMA [20 : 15] output load capacity C_L = 50 pF, CFA [4 : 0] output load capacity C_L = 30 pF.

• CompactFlash common memory access timing

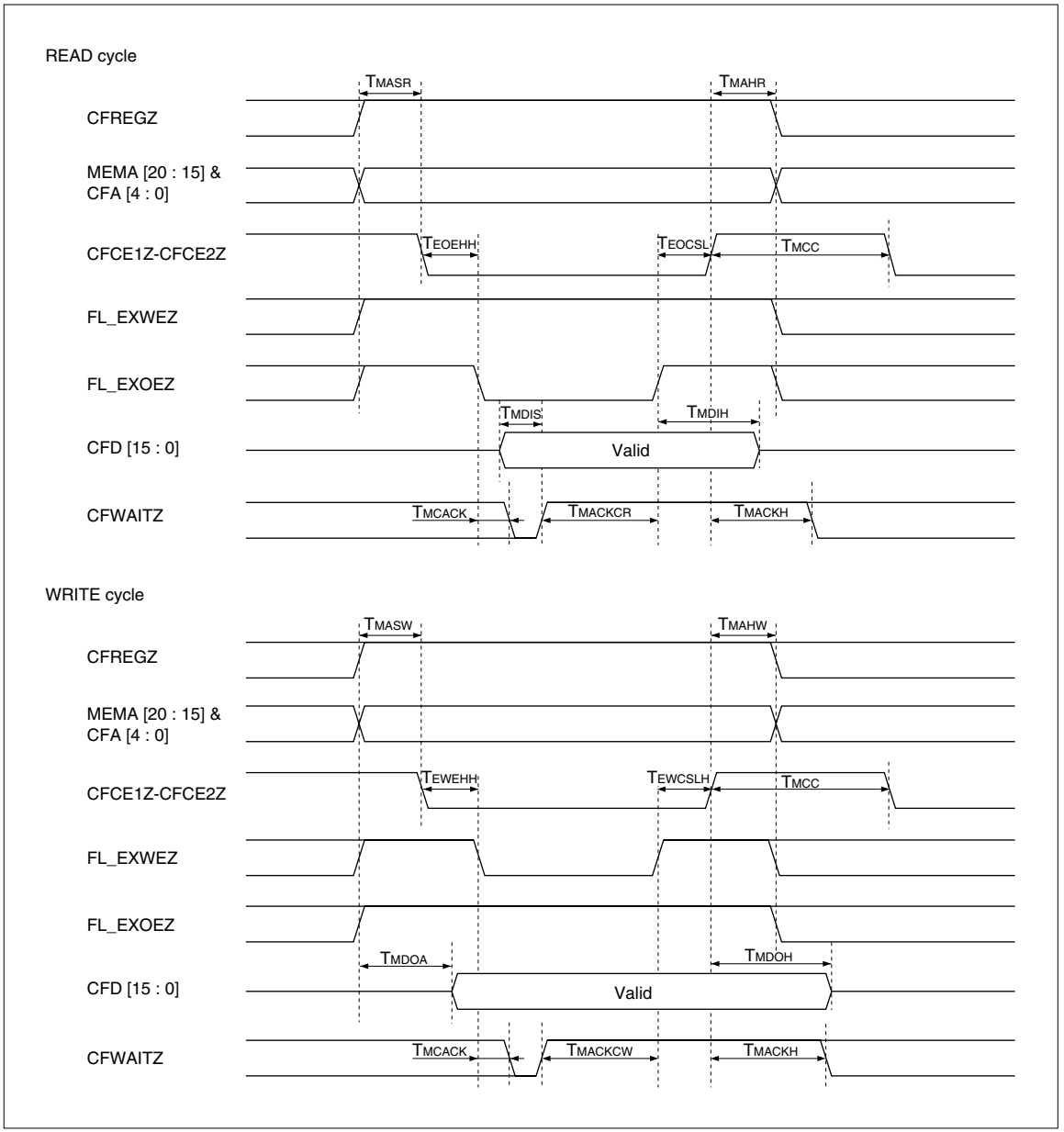


Fig. 12 CompactFlash Common Memory Read/Write Cycle

(DV_{DD} = 3.3 V, DV_{DD2} = 2.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
Output setup period of MEMA [20 : 15] & CFA at reading (relative to the falling edge of CFCE1Z/2Z)	T_{MASR}	T_{MCLK} – 5		ns	2
Output setup period of MEMA [20 : 15] & CFA at writing (relative to the falling edge of CFCE1Z/2Z)	T_{MASW}	T_{MCLK} – 5		ns	2
Output hold period of MEMA [20 : 15] & CFA at reading (relative to the rising edge of CFCE1Z/2Z)	T_{MAHR}	2T_{MCLK} – 5		ns	2
Output hold period of MEMA [20 : 15] & CFA at writing (relative to the rising edge of CFCE1Z/2Z)	T_{MAHW}	T_{MCLK} – 5		ns	2
Minimum "High" period of CFCE1Z/2Z	T_{MCC}	3T_{MCLK} – 5		ns	1
"High" hold period of FL_EXOEZ (relative to the falling edge of CFCE1Z/2Z)	T_{EOEHH}	T_{MCLK} – 5	T_{MCLK} + 5	ns	1
"Low" hold period of CFCE1Z/2Z (relative to the rising edge of FL_EXOEZ)	T_{EOCSLH}	2T_{MCLK} – 5	2T_{MCLK} + 5	ns	1
"High" hold period of FL_EXWEZ (relative to the falling edge of CFCE1Z/2Z)	T_{EWEHH}	T_{MCLK} – 5	T_{MCLK} + 5	ns	1
"Low" hold period of CFCE1Z/2Z (relative to the rising edge of FL_EXWEZ)	T_{EWCSLH}	2T_{MCLK} – 5	2T_{MCLK} + 5	ns	1
Input setup period of CFD (relative to the rising edge of CFWAITZ)	T_{MDIS}	0		ns	
Input hold period of CFD (relative to the rising edge of FL_EXOEZ)	T_{MDIH}	0		ns	
Output delay period of CFD (relative to MEMA [20 : 15] & CFA)	T_{MDOA}	2T_{MCLK} – 5	2T_{MCLK} + 5	ns	1
Output hold period of CFD (relative to the rising edge of CFCE1Z/2Z)	T_{MDOH}	5T_{MCLK} – 5	5T_{MCLK} + 5	ns	1
Determination period of CFWAITZ (relative to the falling edge of FL_EXOEZ/FL_EXWEZ)	T_{MCACK}		2T_{MCLK} + 5	ns	
Rising period of FL_EXOEZ (relative to the rising edge of CFWAITZ)	T_{MACKCR}	2T_{MCLK} – 5	3T_{MCLK} + 5	ns	1
Rising period of FL_EXWEZ (relative to the rising edge of CFWAITZ)	T_{MACKCW}	4T_{MCLK} – 5	5T_{MCLK} + 5	ns	1
Hold period of CFWAITZ (relative to the rising edge of EXDACK0Z/1Z)	T_{MACKH}	0		ns	

NOTES :

1. Output load capacity C_L = 50 pF
2. MEMA [20 : 15] output load capacity C_L = 50 pF, CFA [4 : 0] output load capacity C_L = 30 pF.

• SmartMedia access timing

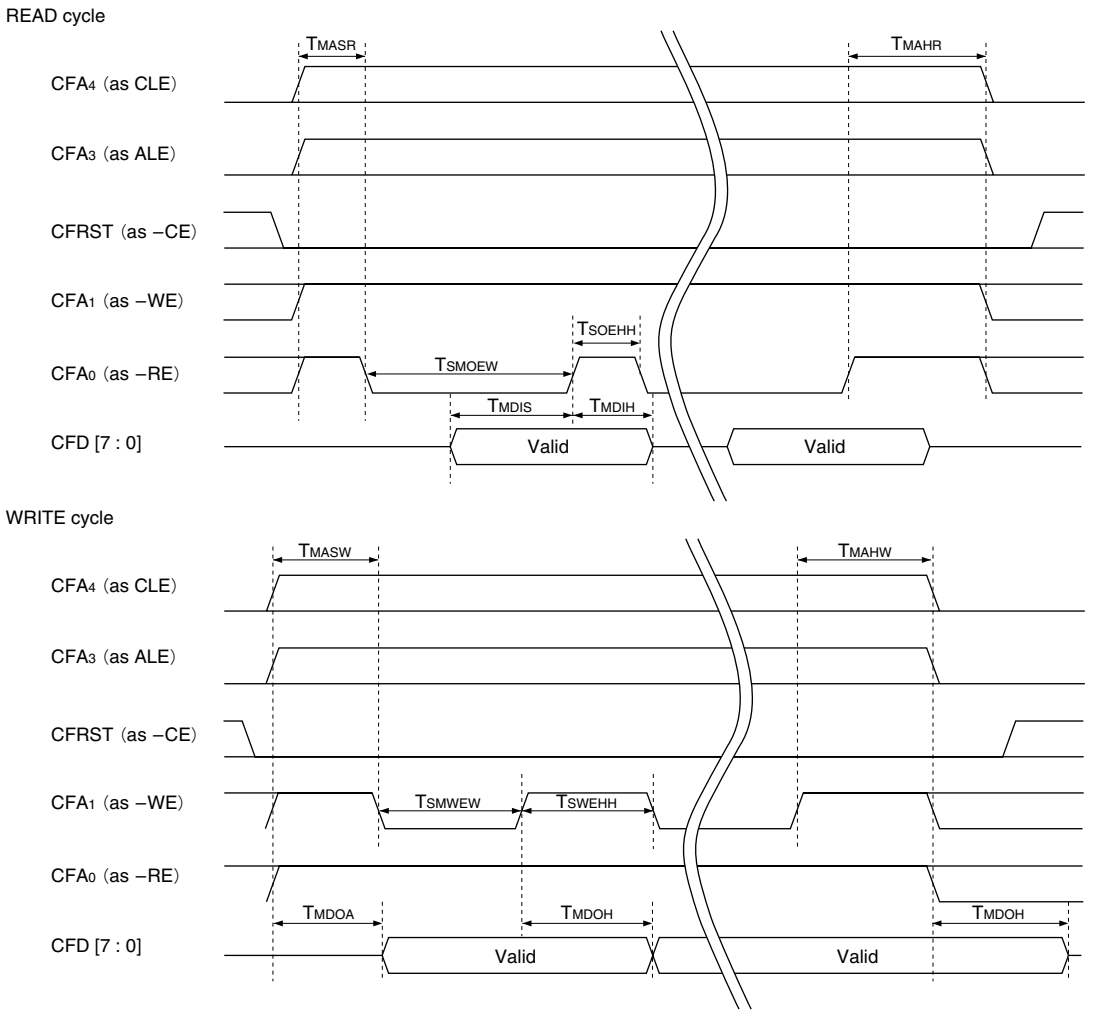


Fig. 13 SmartMedia Read/Write Cycle

(DV_{DD} = 3.3 V, DV_{DD2} = 2.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
Output setup period of CLE, ALE, –WE at reading (relative to the falling edge of –RE)	T_{MASR}	$2T_{MCLK}$ – 5		ns	1
Output setup period of CLE, ALE, –RE at writing (relative to the falling edge of –WE)	T_{MASW}	$2T_{MCLK}$ – 5		ns	1
Output hold period of CLE, ALE, –WE at reading (relative to the rising edge of –RE)	T_{MAHR}	$3T_{MCLK}$ – 5		ns	1
Output hold period of CLE, ALE, –RE at writing (relative to the rising edge of –WE)	T_{MAHW}	$3T_{MCLK}$ – 5		ns	1
"Low" pulse width of –RE	T_{SMOEW}	$4T_{MCLK}$ – 5	$4T_{MCLK}$ + 5	ns	1
"High" pulse width of –RE	T_{SOEHH}	$2T_{MCLK}$ – 5	$2T_{MCLK}$ + 5	ns	1
"Low" pulse width of –WE	T_{SMWEW}	$3T_{MCLK}$ – 5	$3T_{MCLK}$ + 5	ns	1
"High" pulse width of –WE	T_{SWEHH}	$2T_{MCLK}$ – 5	$2T_{MCLK}$ + 5	ns	
Input setup period of CFD [7 : 0] (relative to the rising edge of –RE)	T_{MDIS}	$2T_{MCLK}$ – 5		ns	
Input hold period of CFD [7 : 0] (relative to the rising edge of –RE)	T_{MDIH}	0		ns	
Output delay period of CFD [7 : 0] (relative to the rising edge of CLE, ALE)	T_{MDOA}	$2T_{MCLK}$ – 5	$2T_{MCLK}$ + 5	ns	1
Output hold period of CFD [7 : 0] (relative to the rising edge of –WE)	T_{MDOH}	$2T_{MCLK}$ – 5	$2T_{MCLK}$ + 5	ns	1

NOTE :

1. Output load capacity C_L = 50 pF

USB TIMING

• USB transmitting timing

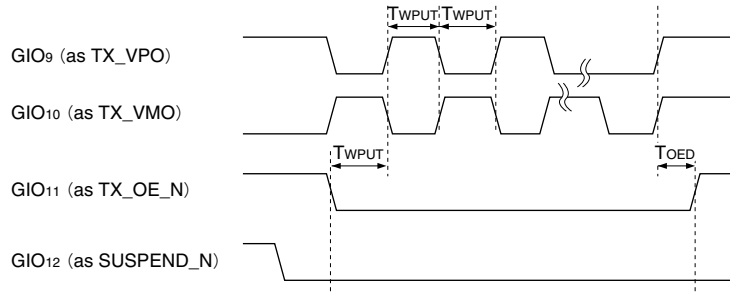


Fig. 14 USB Transmitting Cycle

(DV_{DD} = 3.3 V, DV_{DD2} = 2.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS			UNIT	NOTE
		MIN.	TYP.	MAX.		
Transmission period of 1 bit	T_{WPUT}	80	83	86	ns	1, 2
Output delay period of TX_OE_N	T_{OED}	162	167	172	ns	2

NOTES :

1. When "High" or "Low" continues for N bits period, it is $(48\ MHz)^{-1} \times 4 \times N \pm 3$ ns.
2. Output load capacity C_L = 15 pF
3. USB module will be reset when SE_0 status (GIO_{13} = GIO_{14} = "Low") is input longer than 2.5 µs, in transmitting, so choose USB transceiver IC carefully.

• USB receiving timing

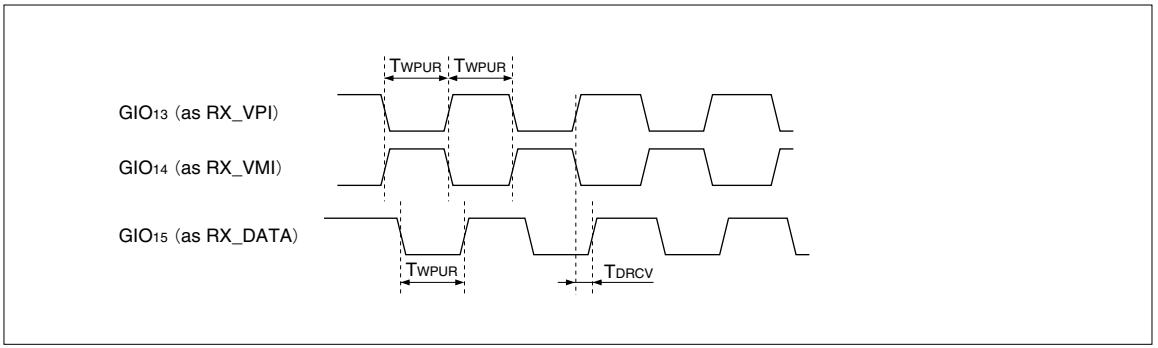


Fig. 15 USB Receiving Cycle

(DV_{DD} = 3.3 V, DV_{DD2} = 2.5 V, T_A = 0 to +70˚C)

PARAMETER	SYMBOL	CONDITIONS			UNIT	NOTE
		MIN.	TYP.	MAX.		
Receiving period of 1 bit	T_{WPUR}	68	83	98	ns	1
Permissible delay period of received data	T_{DRCV}	0		14	ns	

NOTE :

1. When "High" or "Low" continues for N bits period, it is $(48\ MHz)^{-1}$ x 4 x N±3 ns.

UART TIMING

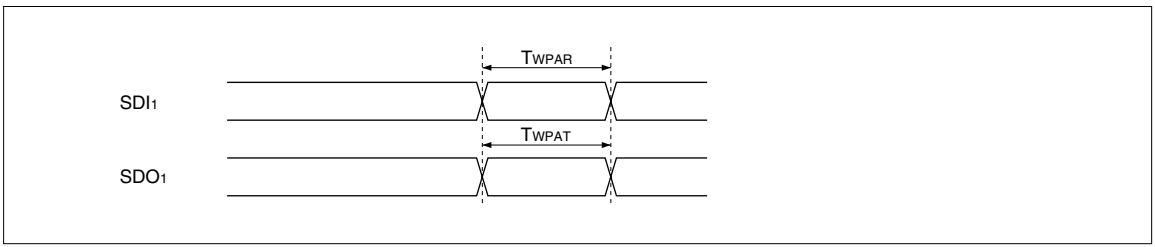


Fig. 16 UART Communication Cycle

(DV_{DD} = 3.3 V, DV_{DD2} = 2.5 V, T_A = 0 to +70˚C)

PARAMETER	SYMBOL	CONDITIONS			UNIT	NOTE
		MIN.	TYP.	MAX.		
SDI_1 input pulse width	T_{WPAR}	8.57			µs	2
SDO_1 output pulse width	T_{WPAT}	8.57			µs	1, 2

NOTES :

1. Output load capacity C_L = 15 pF
2. The baud rate is assumed to be 115.2 k bps.

USART TIMING

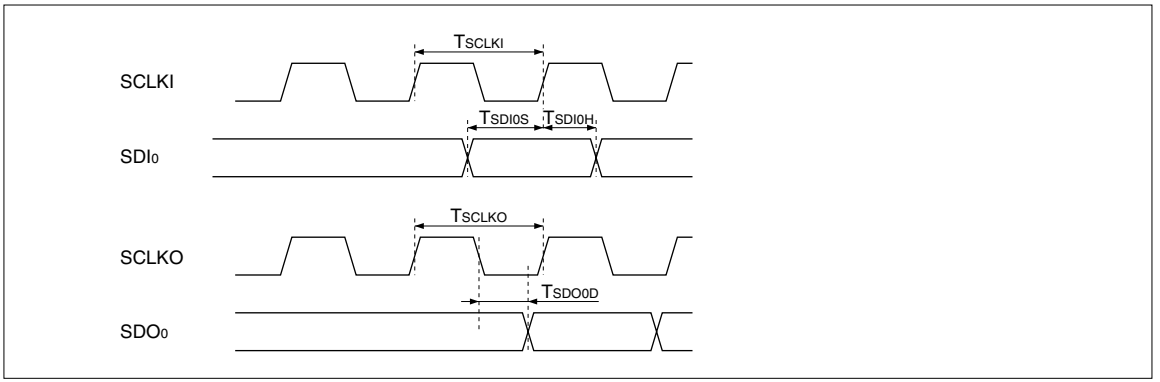


Fig. 17 USART Communication Cycle

(DV_{DD} = 3.3 V, DV_{DD2} = 2.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS			UNIT	NOTE
		MIN.	TYP.	MAX.		
SCLKI clock input cycle	T_{SCLKI}		T_{BRCK}		ns	2
SDI0 input setup time	T_{SDI0S}	1/4 T_{BRCK}			ns	2
SDI0 input hold time	T_{SDI0H}	1/4 T_{BRCK}			ns	2
SCLKO clock output cycle	T_{SCLKO}		T_{BRCK}		ns	1, 2
SDO0 output delay	T_{SDO0D}	–1/4 T_{BRCK}		1/4 T_{BRCK}	ns	1, 2

NOTES :

1. Output load capacity C_L = 15 pF
2. T_{BRCK} means the baud rate clock frequency.
   If COMI (24 MHz) is used and baud rate generator control register BKGC is set to 0x138 (9 600 bps), T_{BRCK} is given as follows : $T_{BRCK} = [48\ MHz/(312*16)]^{-1} = 104\ \mu s$

GIO PORT PWM OUTPUT TIMING

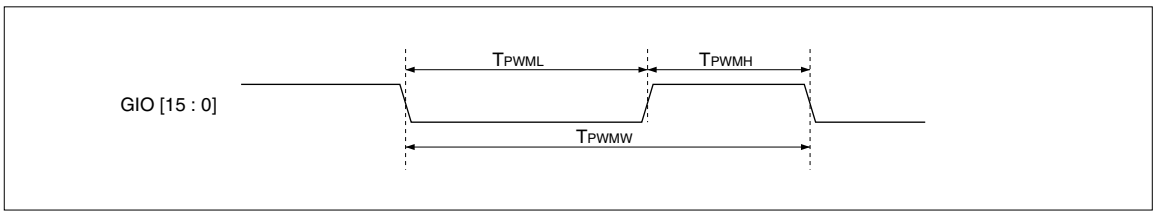


Fig. 18 GIO I/O Timing

PARAMETER	SYMBOL	CONDITIONS	UNIT	NOTE
Output pulse width	T_{PWMW}	256	T_{BCLK}	1, 2
"Low" output pulse width	T_{PWML}	0 to 256	T_{BCLK}	1, 2
"High" output pulse width	T_{PWMH}	$T_{PWMW} - T_{PWML}$	T_{BCLK}	1, 2

NOTES :

1. Output load capacity C_L = 15 pF
2. T_{BCLK} is twice the internal bus clock period.

CCD INTERFACE TIMING

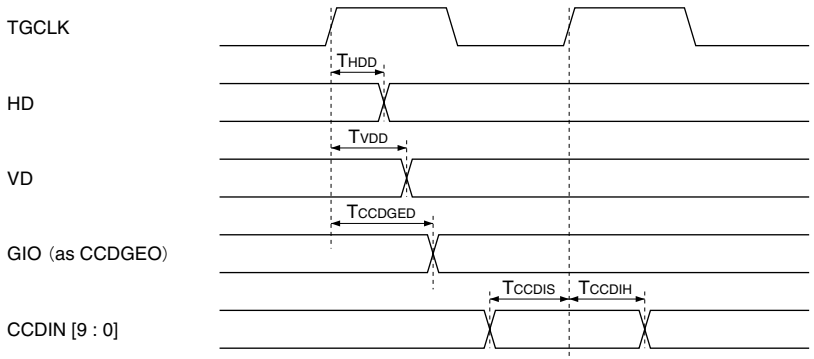


Fig. 19 CCD Data Input Cycle

(DV_{DD} = 3.3 V, DV_{DD2} = 2.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS			UNIT	NOTE
		MIN.	TYP.	MAX.		
HD output delay	T_{HDD}			15	ns	1
VD output delay	T_{VDD}			15	ns	1
CCDGEO output delay	T_{CCDGED}			15	ns	1
CCDIN input setup time	T_{CCDIS}	10			ns	
CCDIN input hold time	T_{CCDIH}	10			ns	

NOTE :

1. Output load capacity C_L = 15 pF

AUDIOIF TIMING

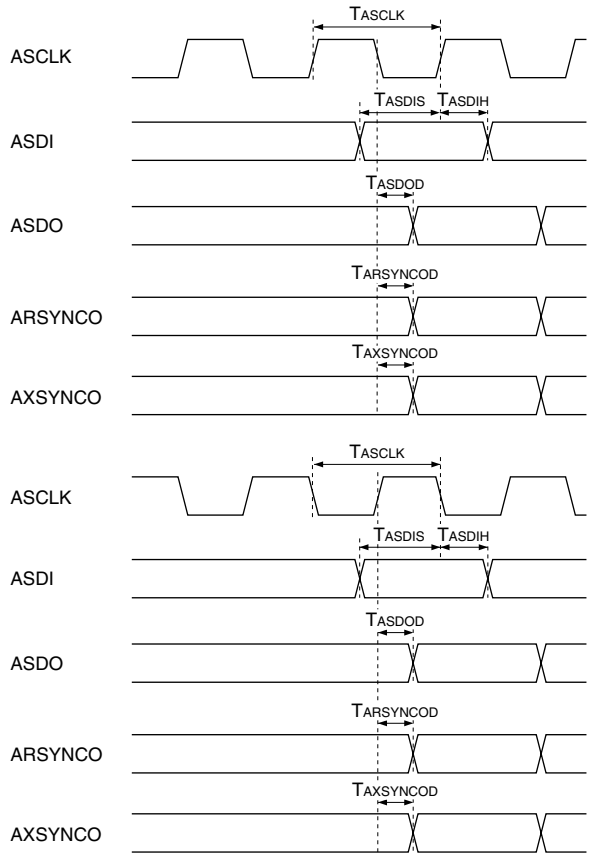


Fig. 20 AUDIOIF Communication Cycle

(DV_{DD} = 3.3 V, DV_{DD2} = 2.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS			UNIT	NOTE
		MIN.	TYP.	MAX.		
Input setup period of ASDI	T_{ASDIS}	1/4 T_{ASCK}			ns	2
Input hold period of ASDI	T_{ASDIH}	1/4 T_{ASCK}			ns	2
Clock output cycle of ASCLK	T_{ASCLK}		T_{ASCK}		ns	1, 2
Output delay period of ASDO	T_{ASDOD}			20	ns	1
Output delay period of ARSYNCO	$T_{ARSYNCOD}$			20	ns	1
Output delay period of AXSYNCO	$T_{AXSYNCOD}$			20	ns	1

NOTES :

1. Output load capacity C_L = 15 pF
2. T_{ASCK} means the clock period of bit-shift-clock.
   If the sampling clock frequency is 32 kHz, TCLK input is 16.384 MHz (512 fs) and bit-shift-clock register (BSCG) is set to 0x0010 (bit-shift-clock is 1.024 MHz or 32 fs), T_{ASCK} is given as follows :
   $T_{ASCK} = (16.384\ MHz/16)^{-1} = 976.5625$ ns

PACKAGE OUTLINES

240 CSP (T-TFBGA240-1414)

(Unit : mm)