

- PERFORMANCE (1850 MHz)
  - ◆ 27 dBm Output Power ( $P_{1dB}$ )
  - ◆ 18 dB Small-Signal Gain (SSG)
  - ◆ 1.2 dB Noise Figure
  - ◆ 42 dBm Output IP3
  - ◆ 45% Power-Added Efficiency
  - ◆ Evaluation Boards Available
  - ◆ Featuring Lead Free Finish Package



### DESCRIPTION AND APPLICATIONS

The FPD1500DFN is a packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT). It utilizes a  $0.25\ \mu\text{m} \times 1500\ \mu\text{m}$  Schottky barrier Gate, defined by high-resolution stepper-based photolithography. The recessed and offset Gate structure minimizes parasitics to optimize performance, with an epitaxial structure designed for improved linearity over a range of bias conditions and input power levels. The FPD1500DFN is available in die form and in other packages.

Typical applications include drivers or output stages in PCS/Cellular base station high-intercept-point LNAs, WLL and WLAN systems, and other types of wireless infrastructure systems.

### ELECTRICAL SPECIFICATIONS AT 22°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>RF SPECIFICATIONS MEASURED AT <math>f = 1850\ \text{MHz}</math> USING CW SIGNAL</b>						
Power at 1dB Gain Compression	$P_{1dB}$	$V_{DS} = 5\ \text{V}; I_{DS} = 50\% I_{DSS}$		27		dBm
Small-Signal Gain	SSG	$V_{DS} = 5\ \text{V}; I_{DS} = 50\% I_{DSS}$		18		dB
Power-Added Efficiency	PAE	$V_{DS} = 5\ \text{V}; I_{DS} = 50\% I_{DSS}; P_{OUT} = P_{1dB}$		45		%
Noise Figure	NF	$V_{DS} = 5\ \text{V}; I_{DS} = 50\% I_{DSS}$		1.2		dB
Output Third-Order Intercept Point (from 15 to 5 dB below $P_{1dB}$ )	IP3	$V_{DS} = 5\ \text{V}; I_{DS} = 50\% I_{DSS}$ Matched for optimal power Matched for best IP3		40 42		dBm
Saturated Drain-Source Current	$I_{DSS}$	$V_{DS} = 1.3\ \text{V}; V_{GS} = 0\ \text{V}$	375	465	550	mA
Maximum Drain-Source Current	$I_{MAX}$	$V_{DS} = 1.3\ \text{V}; V_{GS} \cong +1\ \text{V}$		750		mA
Transconductance	$G_M$	$V_{DS} = 1.3\ \text{V}; V_{GS} = 0\ \text{V}$		400		mS
Gate-Source Leakage Current	$I_{GSO}$	$V_{GS} = -5\ \text{V}$		1	15	$\mu\text{A}$
Pinch-Off Voltage	$ V_P $	$V_{DS} = 1.3\ \text{V}; I_{DS} = 1.5\ \text{mA}$	0.7	0.9	1.3	V
Gate-Source Breakdown Voltage	$ V_{BDGS} $	$I_{GS} = 1.5\ \text{mA}$	12	18		V
Gate-Drain Breakdown Voltage	$ V_{BDGD} $	$I_{GD} = 1.5\ \text{mA}$	12	18		V

### • ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	$V_{DS}$	$-3V < V_{GS} < +0V$		8	V
Gate-Source Voltage	$V_{GS}$	$0V < V_{DS} < +8V$		-3	V
Drain-Source Current	$I_{DS}$	For $V_{DS} > 2V$		$I_{DSS}$	mA
Gate Current	$I_G$	Forward or reverse current		15	mA
RF Input Power <sup>2</sup>	$P_{IN}$	Under any acceptable bias state		350	mW
Channel Operating Temperature	$T_{CH}$	Under any acceptable bias state		175	°C
Storage Temperature	$T_{STG}$	Non-Operating Storage	-40	150	°C
Total Power Dissipation	$P_{TOT}$	See De-Rating Note below		2.2	W
Gain Compression	Comp.	Under any bias conditions		5	dB
Simultaneous Combination of Limits <sup>3</sup>		2 or more Max. Limits		80	%

<sup>1</sup> $T_{Ambient} = 22^{\circ}C$  unless otherwise noted      <sup>2</sup>Max. RF Input Limit must be further limited if input VSWR > 2.5:1

<sup>3</sup>Users should avoid exceeding 80% of 2 or more Limits simultaneously

#### Notes:

- Operating conditions that exceed the Absolute Maximum Ratings will result in permanent damage to the device.
- Total Power Dissipation defined as:  $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$ , where:  
 $P_{DC}$ : DC Bias Power  
 $P_{IN}$ : RF Input Power  
 $P_{OUT}$ : RF Output Power

- Total Power Dissipation to be de-rated as follows above  $22^{\circ}C$ :

$$P_{TOT} = 2.2W - (0.0167W/^{\circ}C) \times T_{PACK}$$

where  $T_{PACK}$  = source lead temperature above  $22^{\circ}C$

(coefficient of de-rating formula is the Thermal Conductivity)

Example: For a  $65^{\circ}C$  source lead temperature:  $P_{TOT} = 2.2W - (0.0167 \times (65 - 22)) = 1.48W$

- **The use of a filled via-hole directly beneath the exposed heatsink tab on the bottom of the package is strongly recommended to provide for adequate thermal management. Ideally the bottom of the circuit board is affixed to a heatsink or thermal radiator.**

### • HANDLING PRECAUTIONS

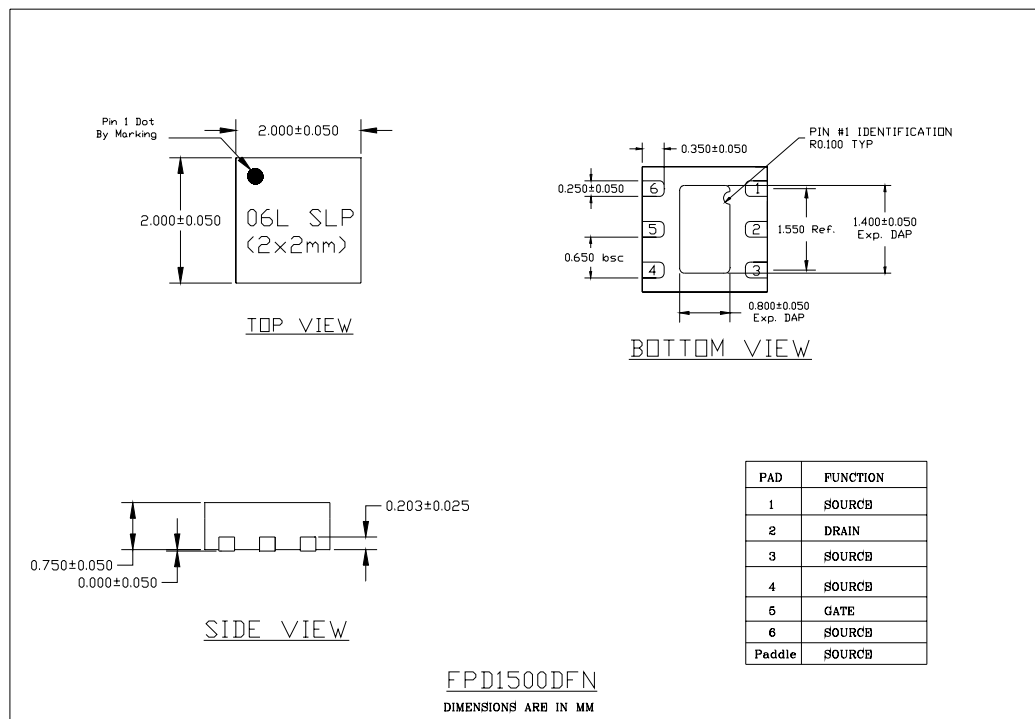
To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A per ESD-STM5.1-1998, Human Body Model. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

### • APPLICATIONS NOTES & DESIGN DATA

Applications Notes are available from your local Filtronic Sales Representative or directly from the factory. Complete design data, including S-parameters, noise data, and large-signal models are available on the Filtronic web site. Evaluation Boards available upon request.

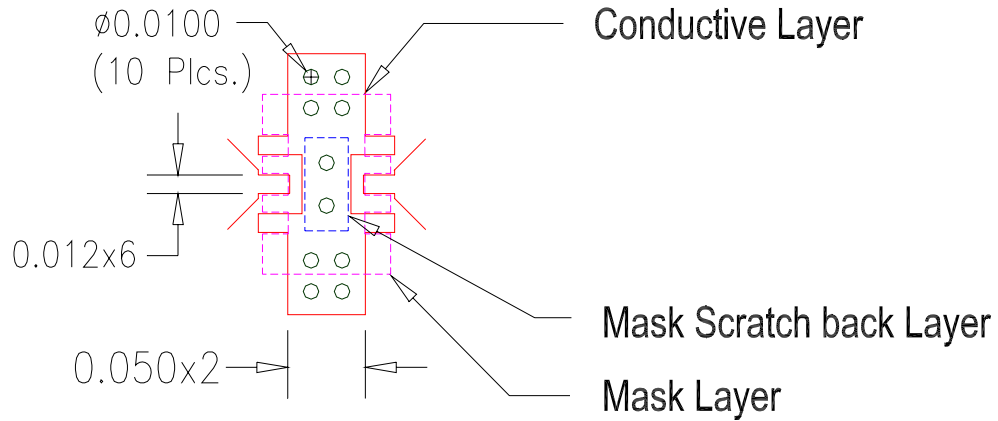
**BIASING GUIDELINES**

- Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias, otherwise the pHEMT may be induced to self-oscillate. Contact your Sales Representative for additional information.
- Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices such as the FPD1500DFN.
- For standard Class A operation, a 50% of  $I_{DSS}$  bias point is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. Note that pHEMTs, since they are “quasi- E/D mode” devices, exhibit Class AB traits when operated at 50% of  $I_{DSS}$ . To achieve a larger separation between  $P_{1dB}$  and  $IP3$ , an operating point in the 25% to 33% of  $I_{DSS}$  range is suggested. Such Class AB operation will not degrade the  $IP3$  performance.

**PACKAGE OUTLINE (dimensions in mm)**


All information and specifications subject to change without notice.

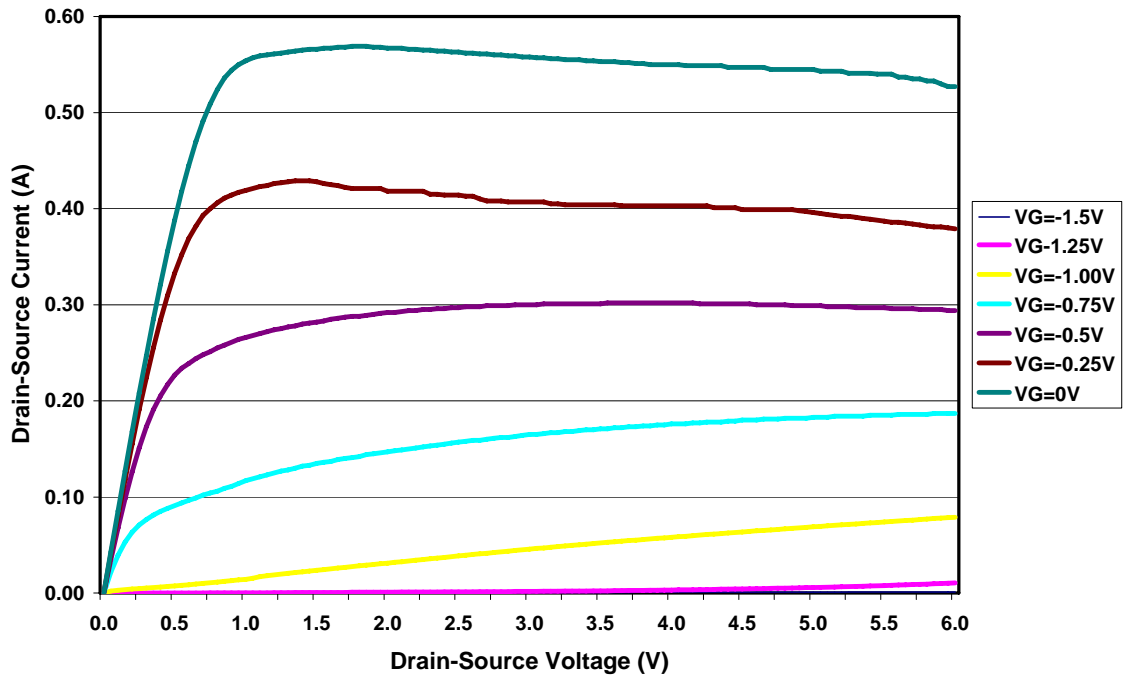
- PCB FOOT PRINT



Dimensions are in Inches

- TYPICAL I-V CHARACTERISTICS

DC IV Curves FPD1500SOT89



Note: The recommended method for measuring  $I_{DSS}$ , or any particular  $I_{DS}$ , is to set the Drain-Source voltage ( $V_{DS}$ ) at 1.3V. This measurement point avoids the onset of spurious self-oscillation which would normally distort the current measurement (this effect has been filtered from the I-V curves presented above). Setting the  $V_{DS} > 1.3V$  will generally cause errors in the current measurements, even in stabilized circuits.

Recommendation: Traditionally a device's  $I_{DSS}$  rating ( $I_{DS}$  at  $V_{GS} = 0V$ ) was used as a predictor of RF power, and for MESFETs there is a correlation between  $I_{DSS}$  and  $P_{1dB}$  (power at 1dB gain compression). For pHEMTs it can be shown that there is *no* meaningful statistical correlation between  $I_{DSS}$  and  $P_{1dB}$ ; specifically a linear regression analysis shows  $r^2 < 0.7$ , and the regression fails the F-statistic test.  $I_{DSS}$  is sometimes useful as a guide to circuit tuning, since the  $S_{22}$  does vary with the quiescent operating point  $I_{DS}$ .