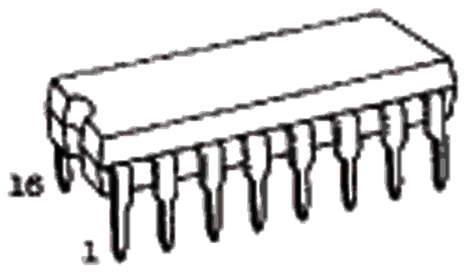
TC4043BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4043BP QUAD 3-STATE R/S LATCH (Quad NOR R/S Latch)

TC4043BP is the latches composed by four independent R/S flip-flop circuits. TC4043BP fabricated with NOR gates is suitable for data processing of four bits configuration. Four output lines can have high impedance regardless of the contents of latches by means of common ENABLE input to make connection to the bus lines easy.

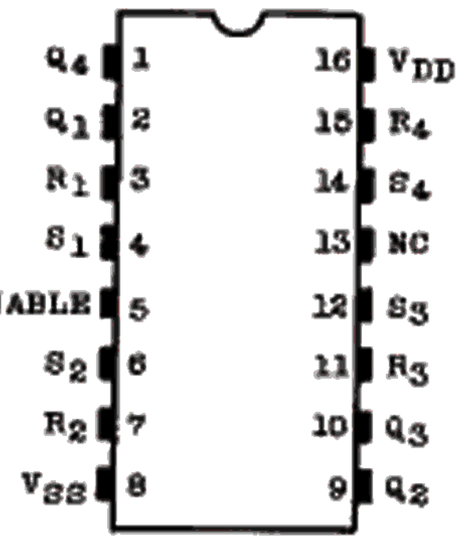


DIP16 (3D16A-P)

ABSOLUTE MAXIMUM RATINGS

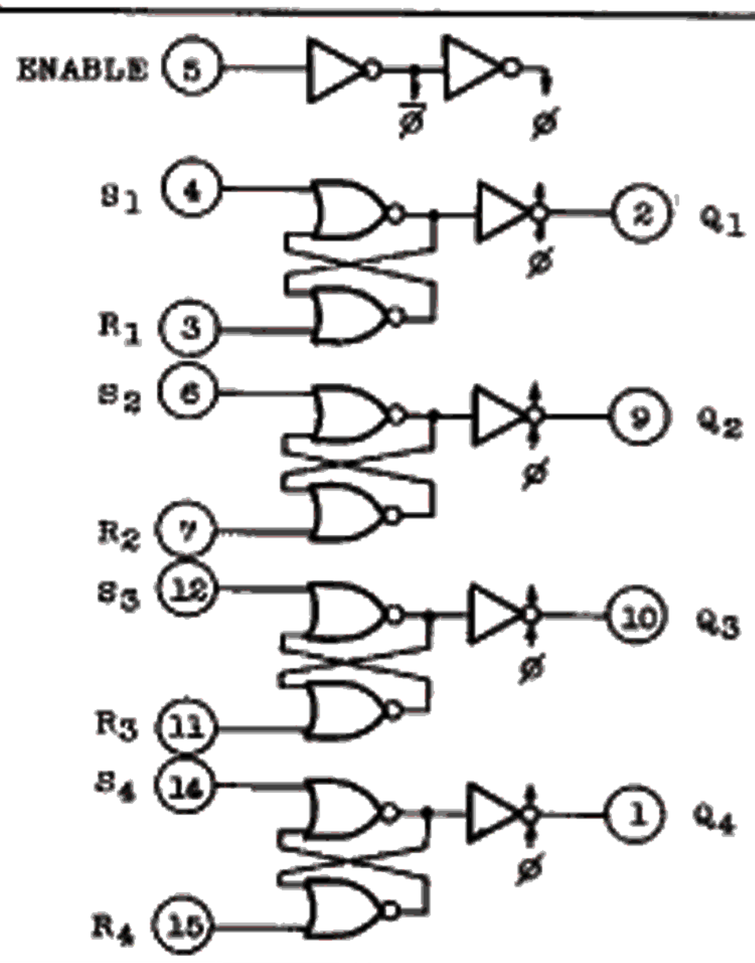
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	Tstg	-65 ~ 150	°C
Lead Temp./Time	Tsol	260°C · 10 sec	

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



TRUTH TABLE

S	R	E	Q
*	*	L	HZ
L	L	H	No Change
L	H	H	L
H	L	H	H
H	H	H	H

* : Don't Care

HZ : High Impedance

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
				10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
				10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Output Low Current		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
3-State Output Leakage Current	"H" Level	I_{DH}	V_{OH}=18V	18	-	0.4	-	10^{-4}	0.4	-	12	μA
	"L" Level	I_{DL}	V_{OL}=0V	18	-	-0.4	-	-10^{-4}	-0.4	-	-12	
Quiescent Device Current		I_{DD}	V_{IN}=V_{SS}, V_{DD} *	5	-	1	-	0.002	1	-	30	μA
				10	-	2	-	0.004	2	-	60	
				15	-	4	-	0.008	4	-	120	

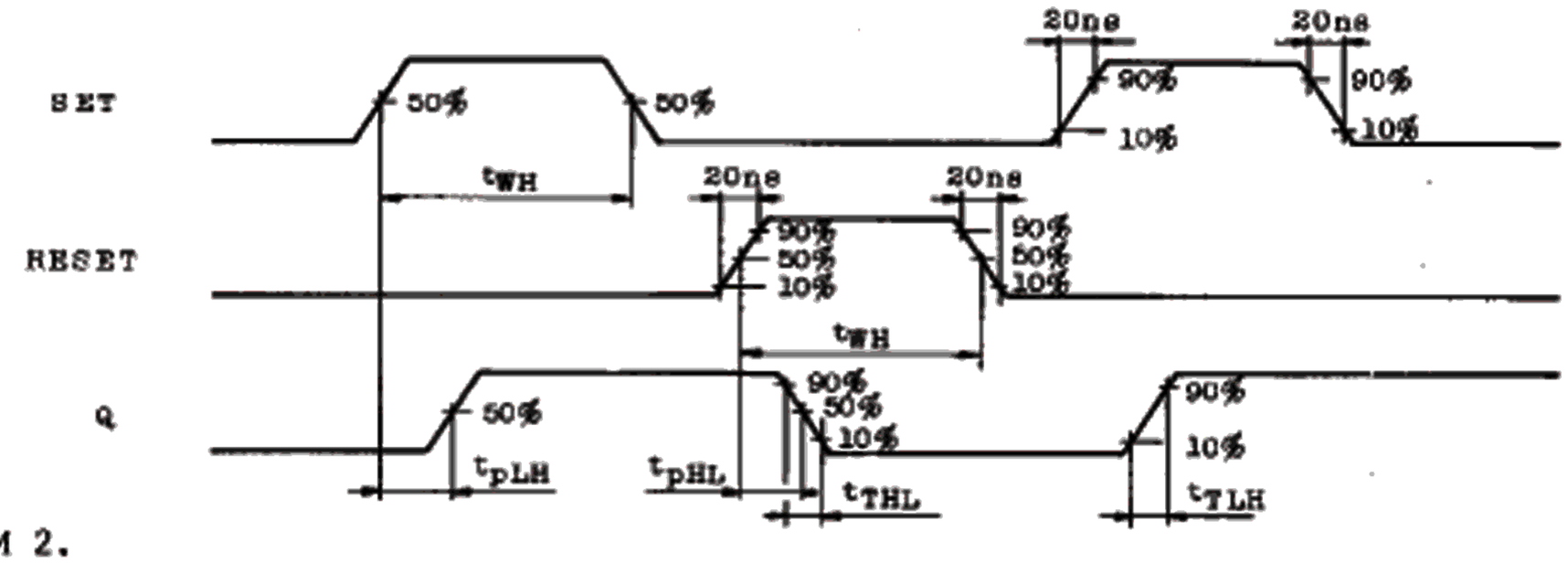
* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (SET, RESET - Q)	t_{pLH} t_{pHL}		5	-	150	300	ns
			10	-	60	140	
			15	-	40	100	
3-State Propagation Delay Time (ENABLE - Q)	t_{pHZ} t_{pZH}	R_L=1kΩ	5	-	60	230	ns
			10	-	25	110	
			15	-	20	80	
3-State Propagation Delay Time (ENABLE - Q)	t_{pLZ} t_{pZL}	R_L=1kΩ	5	-	80	180	
			10	-	35	100	
			15	-	25	70	
Min. Pulse Width (SET, RESET)	t_{WH}		5	-	30	160	ns
			10	-	15	80	
			15	-	10	40	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1.



WAVEFORM 2.