HV400MJ/883

August 1997

High Current MOSFET Driver

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Fast Fall Times . . . . . .16ns at 10,000pF**
- **No Supply Current in Quiescent State**
- **Peak Source Current 6A**
- **Peak Sink Current 30A**
- **High Frequency Operation 300kHz**

Applications

- **Switch Mode Power Supplies**
- **DC/DC Converters**
- **Motor Controllers**
- **Uninterruptable Power Supplies**

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HV400MJ/883	-55 to 125	8 Ld SBDIP	D8.3

Description

The HV400MJ/883 is a single monolithic, non-inverting high current driver designed to drive large capacitive loads at high slew rates. The device is optimized for driving single or parallel connected N-Channel power MOSFETs with total gate charge from 5nC to >1000nC. It features two output stages pinned out separately allowing independent control of the MOSFET gate rise and fall times. The current sourcing output stage is an NPN capable of 6A. An SCR provides over 30A of current sinking. The HV400MJ/883 achieves rise and fall times of 54ns and 16ns respectively driving a 10,000pF load.

Special features are included in this part to provide a simple, high speed gate drive circuit for power MOSFETs. The HV400MJ/883 requires no quiescent supply current, however, the input current is approximately 15mA while in the high state. With the internal current steering diodes (Pin 7) and an external capacitor, both the timing and MOSFET gate power come from the same pulse transformer; no special external supply is required for high side switches. No high voltage diode is required to charge the bootstrap capacitor.

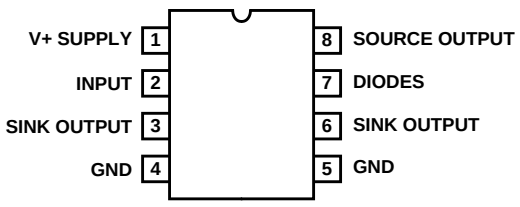
The HV400MJ/883 in combination with the MOSFET and pulse transformer makes an isolated power switch building block for applications such as high side switches, secondary side regulation and synchronous rectification. The HV400MJ/883 is also suitable for driving IGBTs, MCTs, BJTs and small GTOs.

The HV400MJ/883 is a type of buffer; it does not have input logic level switching threshold voltages. This single stage design achieves propagation delays of 20ns. The output NPN begins to source current when the voltage on Pin 2 is approximately 2V more positive than the voltage at Pin 8.

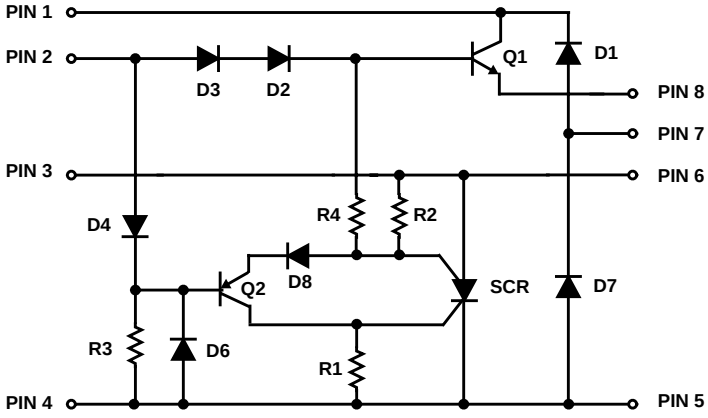
The output SCR switches on when the input Pin 2 is 1V more negative than the voltage at Pins 3/6. Due to the use of the SCR for current sinking, once the output switches low, the input must not go high again until all the internal SCR charge has dissipated, 0.5µs - 1.5µs later.

Pinout

HV400MJ/883 (SBDIP)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

File Number **3584.2**

Absolute Maximum Ratings

Voltage Between Pin 1 and Pins 4/5 . . . . . 35V
Input Voltage Pin 7 (Max) . . . . . .Pin 1 + 1.5V
Input Voltage Pin 7 (Min) . . . . . Pin 4/5 -1.5V
Input Voltage Pin 2 to Pin 4/5 . . . . . ±35V
Input Voltage Pin 2 to Pin 6 . . . . . .-35V
Maximum Clamp Current (Pin 7) . . . . . .±300mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
SBDIP Package	91	25

Maximum Junction Temperature . . . . . 200^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C < T_A < 150^{o}C

Operating Conditions

Temperature Range . . . . . -55^{o}C to 125^{o}C
Supply Voltage . . . . . +10V to +35V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = +15V, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE (^{o}C)	MIN	MAX	UNITS
Input High Differential Voltage (Pin 2 - Pin 8)	V_{IH}	V_{OUT} = 0V, I_{OUT} HI = 10mA	1	25	0.6	2.8	V
			2	125	0.1	2.3	V
			3	-55	1.0	3.2	V
Input Low Differential Voltage (Pin 2 - Pin 3/6)	V_{IL}	V_{OUT} = 12V, I_{OUT} LO = -3mA	1	25	-1.1	-0.8	V
			2	125	-0.95	-0.6	V
			3	-55	-1.2	-0.9	V
Input High Current	I_{IH}	$V_{PIN\ 1,\ 2}$ = 30V, I_{SOURCE} = 0	1	25	15.0	20.0	mA
			2	125	13.0	18.0	mA
			3	-55	18.0	25.0	mA
Input Low Current	I_{IL}	$V_{PIN\ 2}$ = -30V	1	25	-80	1.0	µA
			2, 3	125, -55	-80	1.0	µA
High Output Voltage	V_{OH}	V_{IN} = +V, I_{OUT} = 150mA	1	25	12.1	13.4	V
			2	125	12.2	13.5	V
			3	-55	11.0	13.0	V
Output Low Leakage	I_{OL}	V_{OUT} = 0V, V_{IN} = 0V	1	25	-1.0	50	µA
			2, 3	125, -55	-1.0	60	µA
Low Output Voltage	V_{OL}	V_{IN} = 0V, I_{OUT} = -150mA	1	25	0.8	1.0	V
			2	125	0.65	0.85	V
			3	-55	0.9	1.1	V
Output High Leakage	I_{OH}	V_{IN} = 15V	1	25	-1.0	2.0	µA
			2	125	-1.0	100	µA
			3	-55	-1.0	2.0	µA
Forward Voltage	V_F	I_D = 100mA	1	25	0.8	1.4	V
			2	125	0.8	1.25	V
			3	-55	0.8	1.6	V
Reverse Leakage Current	I_R	V_R = 30V	1	25	-1.0	1.0	µA
			2, 3	125, -55	-1.0	1.0	µA

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

This Table Intentionally Left Blank. See AC Parameter on Table 3.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, Unless Otherwise Specified (Note 2)

PARAMETER	SYMBOL	CONDITIONS	TEMPERATURE (^{o}C)	MIN	MAX	UNITS
Input High Current fPeak	I_{IHP}	I_{SOURCE} = 6A, 1µs Pulse, V_{IN} = 9V, V_{OUT} = 0V	25	500	900	mA
Peak Output Current	I_{OP8}	V_{IN} = 9V, 1µs Pulse, V_{OUT} = 0	25	4	8	A
Peak Output Current	I_{OP6}	V_{IN} = 9V, 1µs Pulse, V_{OUT} = 0	25	25	35	A
Diode (Pin 7) Stored Charge	Q_{RR}	I_D = 100mA	25	6	7	nC
Rise Time	t_r	See Switching Diagram and Test Circuit	25	37	62	ns
Fall Time	t_f	See Switching Diagram and Test Circuit	25	14	21	ns
Delay Time (Lo to Hi)	t_{DR}	See Switching Diagram and Test Circuit	25	6	13	ns
Delay Time (Hi to Lo)	t_{DF}	See Switching Diagram and Test Circuit	25	7	16	ns
Minimum Off Time	t_{OR}	See Switching Diagram and Test Circuit	25	400	1140	ns

NOTE:

2. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 3), 2
Group A Test Requirements	1, 2
Groups C and D Endpoints	1

NOTE:

3. PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Test Descriptions

SYMBOL	DESCRIPTION
DC INPUT PARAMETERS	
V_{IH}	The differential voltage between the input (pin 2) to the output (pin 8) required to source 10mA
V_{IL}	The differential voltage between the input (pin 2) to the output (pins 3, 6) required to sink 3mA
I_{IH}	The current required to maintain the input (pin 2) high with I_{OUT} = 0A
I_{IHP}	The input (pin 2) current for a given pulsed output current
I_{IL}	The current require to maintain the input (pin 2) low
DC OUTPUT PARAMETERS	
V_{OH}	The output (pin 8) voltage with input (pin 2) = V+
I_{OP8}	The pulsed peak source current form output (pin 8)
I_{OL}	The output (pin 8) leakage current with the input (pin 2) = Ground
V_{OL}	The output (pins 3, 6) voltage with the input (pin 2) = Ground
I_{OP6}	The pulsed peak sink current into output (pins 3, 6)
I_{OH}	The output (pins 3, 6) leakage current with the input (pin 2) = V+
V_F	The forward voltage of diode D1 or D7
I_R	The reverse leakage current of diode D1 or D7
Q_{RR}	The time integral of the reverse current at turn off
AC PARAMETERS (See Switching Time Specifications)	
T_R	The low to high transition of the output
T_F	The high to low transition of the output
T_{DR}	The output propagation delay from the input (pin 2) rising edge
T_{DF}	The output propagation delay from the input (pin 2) falling edge
T_{OR}	The minimum time required after an output high to low transition before the next input low to high transition

Switching Diagram and Test Circuit

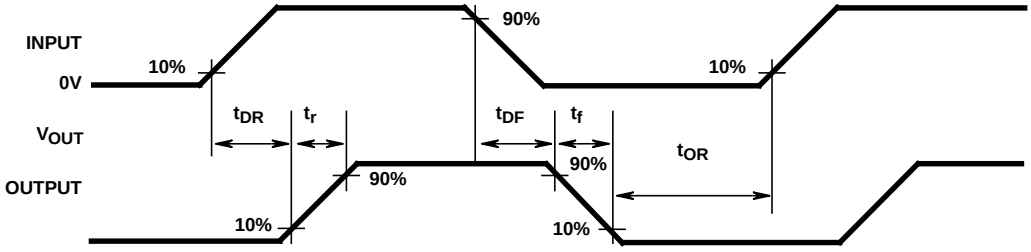


FIGURE 1.

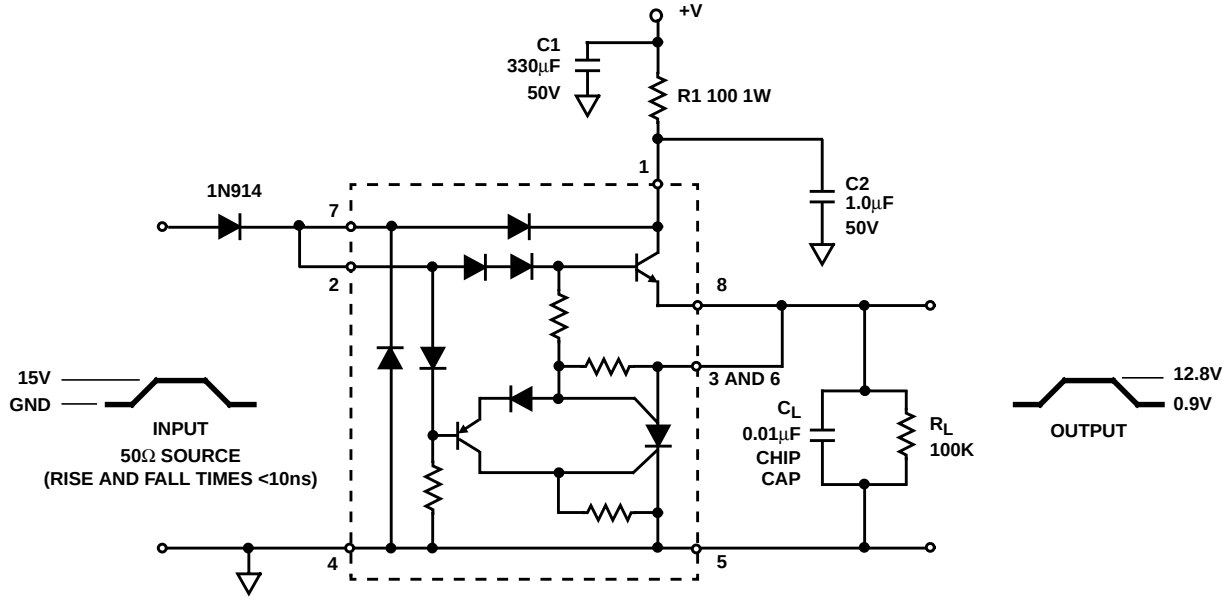
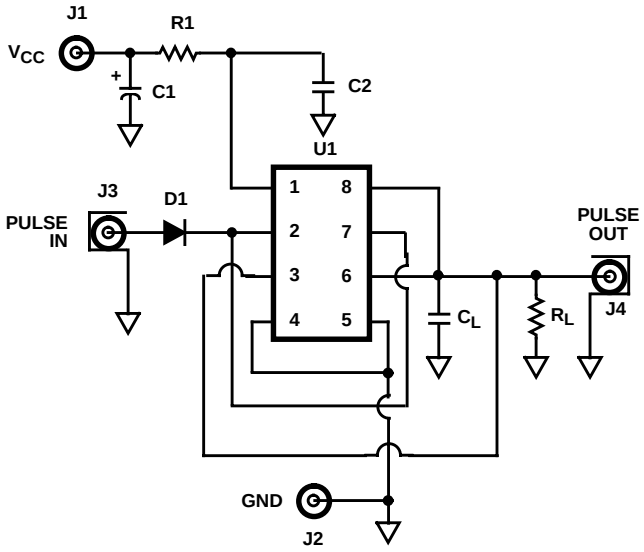
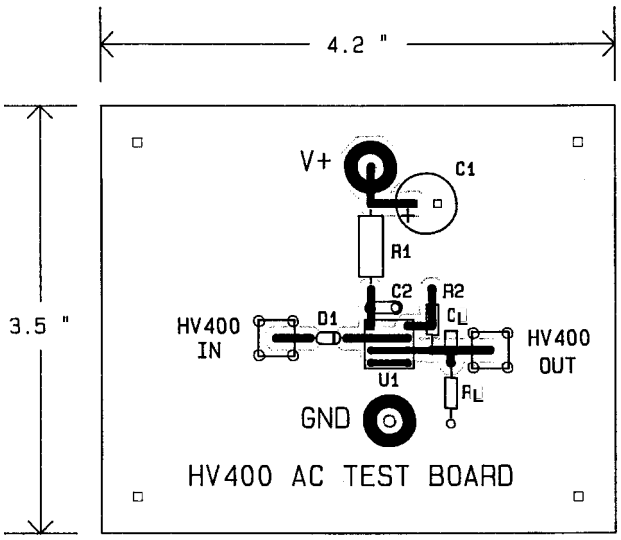


FIGURE 2.

HV400MJ/883 Switching Test Circuit





Parts List

R1 100Ω, 1W Carbon Resistor
R2 Wire
R_L 100kΩ, 1/8W Carbon Resistor
C1 330µF, 50V Capacitor
C2 1µF, 50V Capacitor
C_L 0.01µF, 50V Chip Capacitor
D1 1N914 Diode
J1, J2 PC Mount Banana Jack Johnson 108-0740-001
J3, J4 PC Mount SMA Connector Johnson EFJ142
U1 Intersil HV400MJ/883 I.C.

Typical Design Information

The information contained in this section has been developed through characterization by Intersil Corporation and is for use as application and design information only. No guarantee is implied.

Circuit Operation

The HV400MJ/883s operation is easily explained by referring to the schematic. The control signal is applied to Pin 2. If the control signal is about 2V above Pin 8, the output NPN Q1 turns on charging the MOSFET gate from a capacitor connected to Pin 1. Resistor R4 helps keep the SCR off by applying a reverse bias to the SCR anode gate.

When the control input drops about 1V below Pin 3/6, PNP Q2 turns on which triggers the SCR by driving both the anode and cathode gates. The SCR discharges the MOSFET gate and when its current becomes less than 10mA, it turns off. Transistor Q2 conducts any gate leakage currents, through resistors R1 and R2, once the SCR turns off. Figure 7 shows the output characteristics before the SCR turns on and after it turns off. When the SCR turns on, resistor R4 provides a path to remove Q1 base charge. Resistor R3 provides the base current for Q2 to reduce the turn off delay time. Resistors R1 and R2 reduce the SCR recovery time.

The two diodes connected to the diode input Pin 7 provide some operation flexibility. With Pins 2 and 7 connected together, diode D1 provides a path to recharge the storage capacitor once the MOSFET gate is pulled high and, along with diodes D2 and D3, keeps Q1 from going into hard saturation which would increase delay times. Diode D7 would clamp the input near ground and provide a current path if an input DC blocking capacitor is used.

Alternatively, Pin 7 can be connected to Pin 6 so that the SCR and NPN Q1 don't have to pass reverse current if the output "rings" above the supply or below ground. When high performance diodes are required, Pin 7 can be left disconnected and external diodes substituted.

The diodes in series with Pin 2 decoupled the input from the output during negative going transitions. The absence of input current turns off Q1 and allows Q2 to trigger the SCR. Diode D8 turns off Q2 once the SCR turns on pulling the output low, otherwise Q2 would saturate and slow down circuit operation. In addition, the diodes D2, D3 and D8 improve noise immunity by adding about 2.5V of input hysteresis.

The HV400MJ/883 is capable of large output currents but only for brief durations due to power dissipation.

Circuit Board Layout

PC board layout is very important. Pins 3 and 6 should be connected together as should Pins 4 and 5. Otherwise the internal interconnect impedance is doubled and only half of the bond wires are used which would degrade the reliability.

The bootstrap capacitor should hold at least 10x the charge of the MOSFET and should be connected between Pins 1 and 4/5 with minimum pin lengths and spacings. Likewise, the HV400MJ/883 should be as close to the MOSFET as possible. Any long PC traces (parasitic inductances) between the MOSFET gate and Pins 8 or 3/6 or between the source and Pins 4/5 should be avoided. Inductance between the HV400MJ/883 and the MOSFET limit the MOSFET switching time. If they are too large, the HV400MJ/883 may operate erratically as discussed below.

Cross Conduction Faults

It is possible to have both Q1 and the SCR on at the same time resulting in very large cross conduction currents. The SCR has larger current capacity so the output goes low and the storage capacitor is discharged. The conditions that cause cross conduction and precautions are discussed below.

Minimum Off Time

The SCR requires a recovery time before voltage can be reapplied without it switching back on. Figure 13 shows how this SCR recovery time, called “minimum off time” (t_{OR}), is a function of the load capacitance. If the input voltage goes high before this recovery time is complete, the SCR will switch back on.

Note that reverse current flowing through the SCR, for example due to load inductance ringing, extends the minimum off time. Since the minimum off time is really dependent upon how much stored charge remains in the SCR when the anode (Pin 3/6) is taken positive, it may vary for different applications. Figure 13 indirectly shows that the minimum off time increases with larger currents. It also increases at elevated temperatures as shown in Figure 14. Excessive ringing increases the minimum off time since the stored charge doesn’t begin to dissipate until the current drops below 10mA for the last time. Rising anode voltage acts on the internal SCR capacitance to generate its own triggering current. The excess stored charge increases this capacitance. Faster rise times and/or higher voltages also increase the amount of internal trigger current from the internal capacitance so applications with larger dV/dt require longer minimum off times.

The minimum off time must be considered for all occurrences of SCR current. For example, in a half bridge switch mode power supply, there are two MOSFETs connected to the transformer primary. Assume that the high side MOSFET switch is off. When the low side MOSFET switch is turned on, the HV400MJ/883 driving the high side MOSFET will have to sink gate current from C_{GD} and will have to source gate current when the low side MOSFET switches back off. Both of these current pulses will try to flow through Pin 3/6 since the Pin 8 output is turned off. Sourcing current from Pins 3/6 through the SCR is possible, the Pin 3/6 voltage becoming negative with respect to Pins 4/5 (See Figure 8). But a better practice would be to connect a Schottky diode between Pins 4/5 (anode) and 3/6 (cathode) so reverse current does not flow through the SCR.

False SCR Triggering

The SCR may be triggered inadvertently. The output may overshoot the input due to inductive loading or over driving the output NPN (allowing it to saturate). Whenever Pin 6 is more positive than Pin 2 by 1V, the SCR is triggered on.

Also, if the output rises too rapidly, greater than 0.5V/ns, the SCR may self trigger. Both issues are resolved by minimizing the load inductance and inserting sufficient resistance, usually 0.1Ω to 10Ω, between Pin 8 and the load.

A very fast negative going input voltage can result in minimum off times of about 2.5µs. If the output can not keep up with the falling input, the stored charge of diode D4 is transferred into the base of Q2. This excess charge in Q2 must have time to dissipate. Otherwise, when Pin 3/6 goes positive, Q2 will turn on and trigger the SCR. An external diode in series with Pin 2, as shown in Figure 1, will prevent D4 from discharging into the base of Q2 but that will also reduce the output voltage by the forward voltage of that diode.

Internal Diodes

The internal diodes connected to Pin 7 are provided for convenience but may not be suitable for large currents. Since they are part of the integrated circuit, they are physically small, operate at high current densities, and have long recovery times. Figure 15 shows that their forward characteristics degrade above 100mA. In addition, Figure 16 shows their reverse recovery charge as a function of forward current. The product of this charge, the applied reverse voltage and the frequency is the additional power dissipation due to the diodes. For stored charge calculations, use the peak forward current within 100ns of the application of reverse bias. In addition to the extra power dissipation, the capacitance of these diodes may extend the switching delay times.

Power Dissipation Calculations

The power required to drive the MOSFET is the product of its total gate charge times the gate supply voltage (maximum voltage on HV400MJ/883 Pin 1, 2 or 7) times the frequency. Assuming that the MOSFET gate resistance is negligible, this power is dissipated within the HV400MJ/883. If resistors are placed between the HV400MJ/883 and the MOSFET, then some of the power is dissipated in the resistors, the percentage depending upon the ratio of resistors to HV400MJ/883 output impedance.

There are two other sources of power dissipation to consider. First there is the power in R3 which is the product of the input Pin 2 current and voltage (with no output current) times the duty cycle. Second is the product of the Pin 7 diode stored charge, which is dependent upon the forward current, times the applied diode reverse voltage times the frequency. This information is available from Figure 3 and Figure 16 in this data sheet.

Applications Circuits

The HV400MJ/883 was designed to interface a pulse transformer to a power MOSFET. There must be some means to balance the transformer volt-second product over a cycle. The unipolar drive shown in Figure 3 lets the core magnetization inductance reverse the primary and secondary voltages. The zener diode on the primary side limits this voltage and must be capable of dissipating the energy stored in the transformer. The load may be connected to either the power MOSFET drain or source.

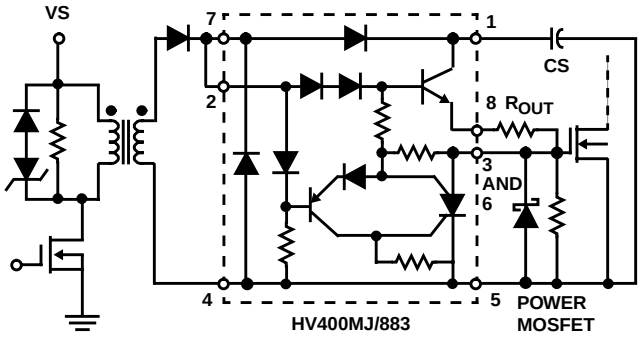


FIGURE 3. UNIPOLAR DRIVE

A diode is added in series with Pins 2 and 7 to allow the transformer secondary to go negative. The charge storage of the Pin 7 diode may cause the turn off delay time to be too long. Alternatively, Pin 7 could be left disconnected and a second external diode connected between the transformer (anode) and Pin 1 (cathode). In some applications the diode in series with Pin 2 may be unnecessary but the -35V input to output or ground maximum rating should be observed.

Sometimes the volt-second balance is achieved by a push-pull drive on the pulse transformer primary. This is especially useful if there are two secondary windings driving two HV400MJ/883s out of phase such as in a half-bridge configuration.

Other times it is more convenient to achieve volt-second balance by using capacitors to block DC in the primary and secondary windings as shown in Figure 4. The Pin 7 diodes provide a path for discharging the secondary side DC blocking capacitor. Both capacitors, C_{IN} and C_S, should be at least 10 times the equivalent MOSFET gate capacitance.

The HV400MJ/883 can be used as a current booster for low side switches by connecting directly to the PWM output. The circuit would be similar to the switching time test circuit.

It is worth restating that some consideration (and experimentation) should be given to the choice of external components, i.e., resistors, capacitors and diodes, to optimize performance in a given application.

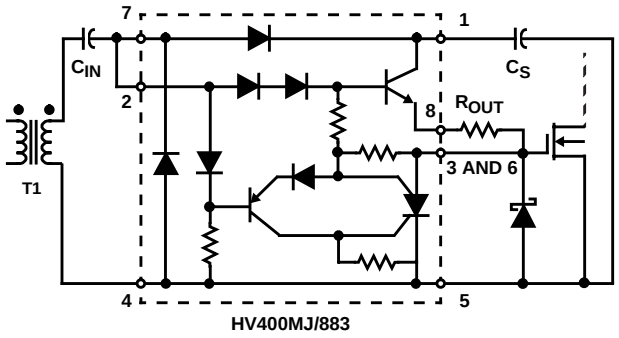
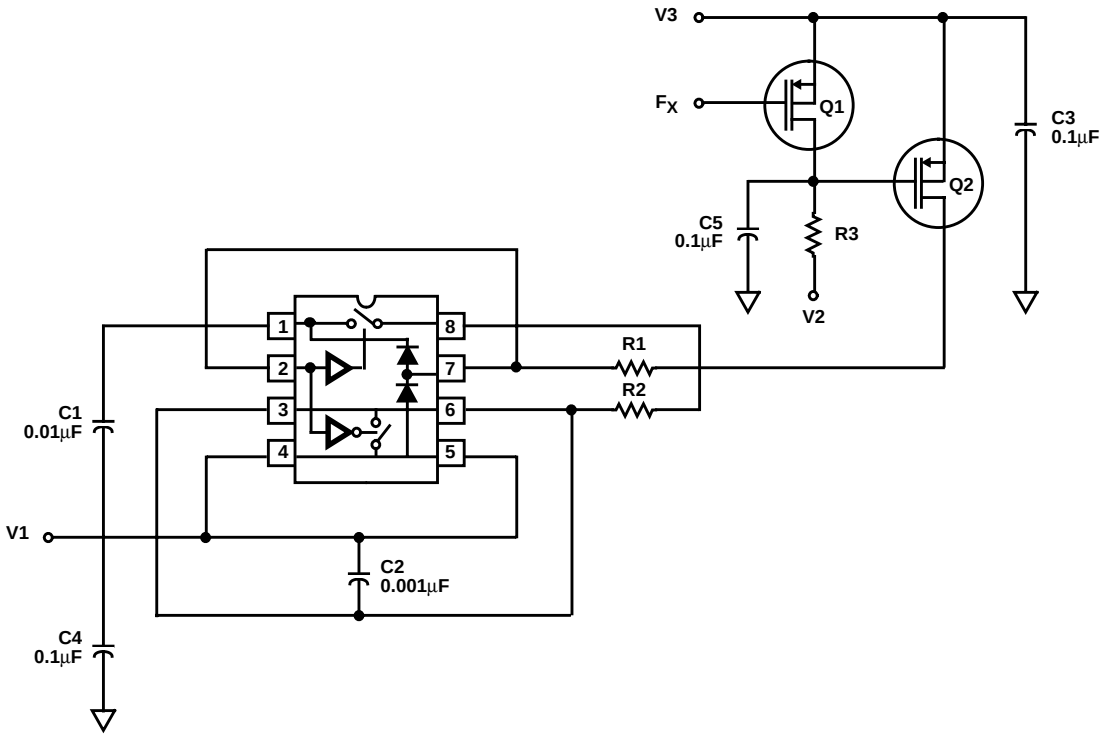


FIGURE 4. BIPOLAR DRIVE WITH DC BLOCKING CAPACITOR

Burn-In Circuit (Dynamic)



NOTES:

4. R1 = 100Ω, 5%, 1/4W.
5. R2 = 5Ω, 5%, 2W.
6. R3 = 100Ω, 5%, 2W.
7. C1 = 0.01µF, 10%, 30V.
8. C2 = 0.001µF, 10%, 30V.
9. C3, C4, C5 = 0.1µF, 20%, 50V.
10. V1 = -15.5V, ± 0.5V.
11. V2 = -5.5V, ± 0.5V.
12. V3 = +5.5V, ± 0.5V.
13. Q1, Q2 = SK9505 or Equivalent. (One Pair Per Board Column)
14. F_X = 12.5kHz, 50% Duty Cycle.
    V_{IL} = 0.8V (Max)
    V_{IH} = +4V (Min)

Die Characteristics

DIE DIMENSIONS:

1700 x 1820 x 483µm

METALLIZATION:

Type: 1% Cu, 99% Al
Thickness: 16kÅ ± 2kÅ

SUBSTRATE POTENTIAL (POWERED UP):

Unbiased

WORST CASE CURRENT DENSITY:

8.2×10^4 A/cm^2 during 1µs pulse with -35A output current, through 8µm wide line 14kA thick.

GLASSIVATION:

Type: Silox
Thickness: 12kÅ ± 2kÅ
Type: Nitride
Thickness: 3.5kÅ ± 2.5kÅ

TRANSISTOR COUNT:

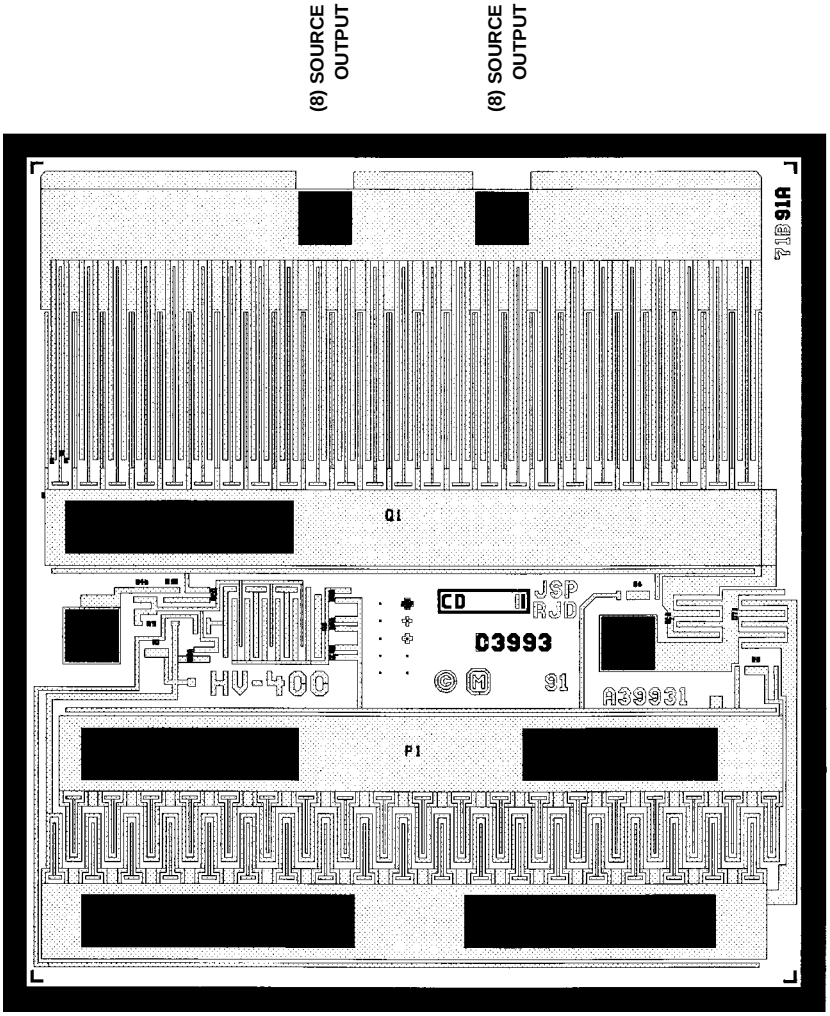
3

PROCESS:

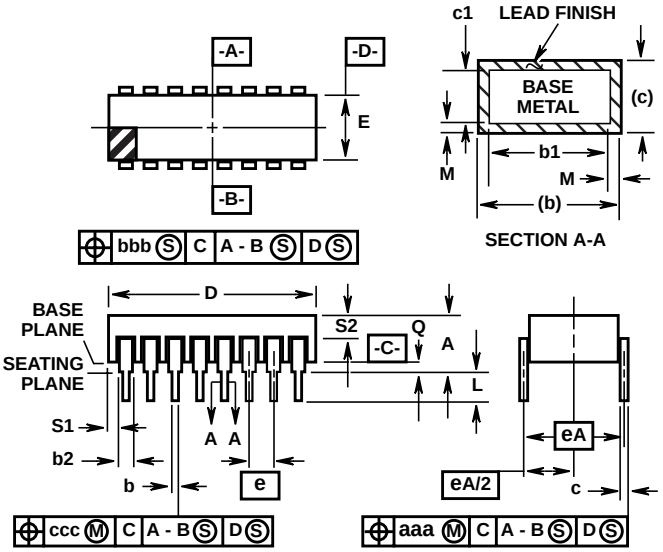
HFSB Linear Dielectric Isolation

Metallization Mask Layout

HV400MJ/883



Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D8.3 MIL-STD-1835 CDIP2-T8 (D-4, CONFIGURATION C)
8 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	8		8		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

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