

NC7WZ125

TinyLogic® UHS Dual Buffer with 3-STATE Outputs

General Description

The NC7WZ125 is a Dual Non-Inverting Buffer with independent active LOW enables for the 3-STATE outputs. The Ultra High Speed device is fabricated with advanced CMOS technology to achieve superior switching performance with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} operating range. The inputs and outputs are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 5.5V independent of V_{CC} operating range. Outputs tolerate voltages above V_{CC} when in the 3-STATE condition.

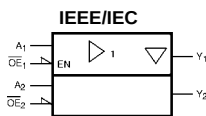
Features

- Space saving US8 surface mount package
- MicroPak™ leadless package
- Ultra High Speed; t_{PD} 2.6 ns typ into 50 pF at 5V V_{CC}
- High Output Drive; ± 24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range; 1.65V to 5.5V
- Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/outputs
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Outputs are overvoltage tolerant in 3-STATE mode
- Patented noise/EMI reduction circuitry implemented

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7WZ125K8X	MAB08A	WZ25	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
NC7WZ125L8X	MAC08A	P3	8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

Logic Symbol



Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Enable Inputs for 3-STATE Outputs
A_n	Input
Y_n	3-STATE Outputs

Function Table

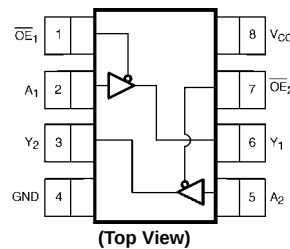
Inputs		Output
$\overline{OE}$	A_n	Y_n
L	L	L
L	H	H
H	L	Z
H	H	Z

H = HIGH Logic Level L = LOW Logic Level Z = 3-STATE

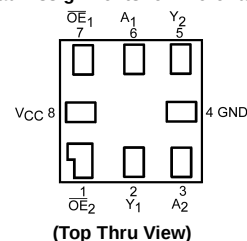
TinyLogic® is a registered trademark of Fairchild Semiconductor Corporation.

MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

Connection Diagrams



Pad Assignments for MicroPak



Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	–0.5V to +7V
DC Input Voltage (V_{IN}) (Note 2)	–0.5V to +7V
DC Output Voltage (V_{OUT})	–0.5V to +7V
DC Input Diode Current (I_{IK}) @ $V_{IN} < 0V$	–50 mA
DC Output Diode Current (I_{OK}) @ $V_{OUT} < 0V$	–50 mA
DC Output Source/Sink Current (I_{OUT})	± 50 mA
DC V_{CC} /Ground Current (I_{CC}/I_{GND})	± 100 mA
Storage Temperature Range (T_{STG})	–65°C to +150°C
Junction Lead Temperature under Bias (T_J)	+150°C
Junction Lead Temperature (T_L) (Soldering, 10 seconds)	+260°C
Power Dissipation (P_D) @ +85°C	250 mW

Recommended Operating Conditions (Note 3)

Supply Voltage Operating (V_{CC})	1.65V to 5.5V
Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	
Active State	0V to V_{CC}
3-STATE	0V to 5.5V
Operating Temperature (T_A)	–40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} @ 1.8V, 0.15V, 2.5V ± 0.2V	0 ns/V to 20 ns/V
V_{CC} @ 3.3V ± 0.3V	0 ns/V to 10 ns/V
V_{CC} @ 5.0V ± 0.5V	0 ns/V to 5 ns/V
Thermal Resistance (θ_{JA})	250°C/W

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input Voltage	1.65 to 1.95 2.3 to 5.5	0.75 V_{CC} 0.7 V_{CC}			0.75 V_{CC} 0.7 V_{CC}		V		
V_{IL}	LOW Level Input Voltage	1.65 to 1.95 2.3 to 5.5			0.25 V_{CC} 0.3 V_{CC}		0.25 V_{CC} 0.3 V_{CC}	V		
V_{OH}	HIGH Level Output Voltage	1.65	1.55	1.65		1.55		V	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100 \mu\text{A}$
		2.3	2.2	2.3		2.2				
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		1.65	1.29	1.52		1.29		V	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -4 \text{ mA}$
		2.3	1.9	2.15		1.9				$I_{OH} = -8 \text{ mA}$
		3.0	2.4	2.80		2.4				$I_{OH} = -16 \text{ mA}$
		3.0	2.3	3.68		2.3				$I_{OH} = -24 \text{ mA}$
V_{OL}	LOW Level Output Voltage	4.5	3.8	4.20		3.8		V	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -32 \text{ mA}$
		1.65		0.0	0.10		0.10			$I_{OL} = 100 \mu\text{A}$
		2.3		0.0	0.10		0.10			
		3.0		0.0	0.10		0.10			
		4.5		0.0	0.10		0.10			
		1.65		0.08	0.24		0.24	V		$I_{OL} = 4 \text{ mA}$
		2.3		0.10	0.3		0.3			$I_{OL} = 8 \text{ mA}$
		3.0		0.15	0.4		0.4			$I_{OL} = 16 \text{ mA}$
		3.0		0.22	0.55		0.55			$I_{OL} = 24 \text{ mA}$
		4.5		0.22	0.55		0.55			$I_{OL} = 32 \text{ mA}$
I_{IN}	Input Leakage Current	0 to 5.5			±0.1		±1	μA	$V_{IN} = 5.5V, \text{GND}$	
I_{OZ}	3-STATE Output Leakage	1.65 to 5.5			±0.5		±5	μA	$V_{IN} = V_{IH}$ or V_{IL} $0 \leq V_{OUT} \leq 5.5V$	
I_{OFF}	Power Off Leakage Current	0.0			1		10	μA	V_{IN} or $V_{OUT} = 5.5V$	
I_{CC}	Quiescent Supply Current	1.65 to 5.5			1		10	μA	$V_{IN} = 5.5V, \text{GND}$	

Noise Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C		Units	Conditions
			Typ	Max		
V _{OLP} (Note 4)	Quiet Output Maximum Dynamic V _{OL}	5.0		1.0	V	C _L = 50 pF
V _{OLV} (Note 4)	Quiet Output Minimum Dynamic V _{OL}	5.0		1.0	V	C _L = 50 pF
V _{OHV} (Note 4)	Quiet Output Minimum Dynamic V _{OH}	5.0		4.0	V	C _L = 50 pF
V _{IHD} (Note 4)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	C _L = 50 pF
V _{ILD} (Note 4)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	C _L = 50 pF

Note 4: Parameter guaranteed by design.

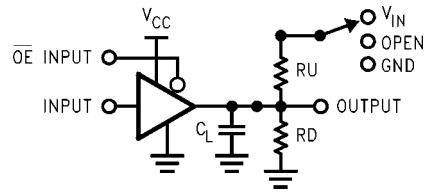
AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t _{PLH} , t _{PHL}	Propagation Delay A _N to Y _N	1.8 ± 0.15 2.5 ± 0.2 3.3 ± 0.3 5.0 ± 0.5	2.0 1.0 0.8 0.5		12.0 7.5 5.2 4.5	2.0 1.0 0.8 0.5	13.0 8.0 5.5 4.8	ns	C _L = 15 pF R _D = 1 MΩ S1= Open	Figures 1, 3
t _{PLH} , t _{PHL}	Propagation Delay A _N to Y _N	3.3 ± 0.3 5.0 ± 0.5	1.2 0.8		5.7 5.0	1.2 0.8	6.0 5.3	ns	C _L = 50 pF R _D = 500Ω S1= Open	Figures 1, 3
t _{OSLH} , t _{OSHL}	Output to Output Skew (Note 5)	3.3 ± 0.3 5.0 ± 0.5			1.0 0.8		1.0 0.8	ns	C _L = 50 pF R _D = 500Ω S1= Open	Figures 1, 3
t _{PZL} , t _{PZH}	Output Enable Time	1.8 ± 0.15 2.5 ± 0.2 3.3 ± 0.3 5.5 ± 0.5	3.0 1.8 1.2 0.8		14.0 8.5 6.2 5.5	3.0 1.8 1.2 0.8	15.0 9.0 6.5 5.8	ns	C _L = 50 pF R _D , R _U = 500 Ω S1 = GND for t _{PZH} S1 = V _I for t _{PZL} V _I = 2 x V _{CC}	Figures 1, 3
t _{PLZ} , t _{PHZ}	Output Disable Time	1.8 ± 0.15 2.5 ± 0.2 3.3 ± 0.3 5.0 ± 0.5	2.5 1.5 0.8 0.3		12.0 8.0 5.7 4.7	2.5 1.5 0.8 0.3	13.0 8.5 6.0 5.0	ns	C _L = 50 pF R _D , R _U = 500 Ω S1 = GND for t _{PZH} S1 = V _I for t _{PZL} V _I = 2 x V _{CC}	Figures 1, 3
C _{IN}	Input Capacitance	0		2.5				pF		
C _{OUT}	Output Capacitance	5.0		4				pF		
C _{PD}	Power Dissipation Capacitance	3.3 5.0		10 12				pF	(Note 6)	Figure 2

Note 5: Parameter guaranteed by design. t_{OSLH} = |t_{PLHmax} - t_{PLHmin}|; t_{OSHL} = |t_{PHLmax} - t_{PHLmin}|.

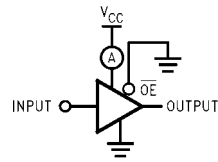
Note 6: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression:
I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CCstatic}).

AC Loading and Waveforms



C_L includes load and stray capacitance
 Input PRR = 1.0 MHz; $t_w = 500$ ns

FIGURE 1. AC Test Circuit



Input = AC Waveform; $t_r = t_f = 1.8$ ns;
 PRR = 10 MHz; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

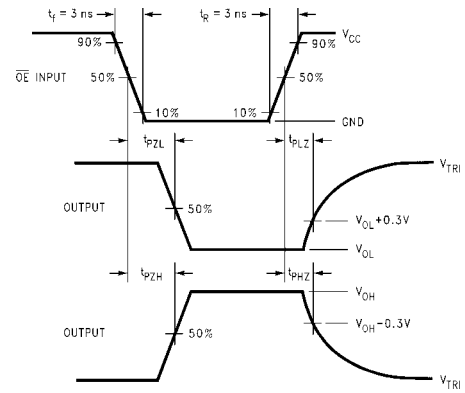
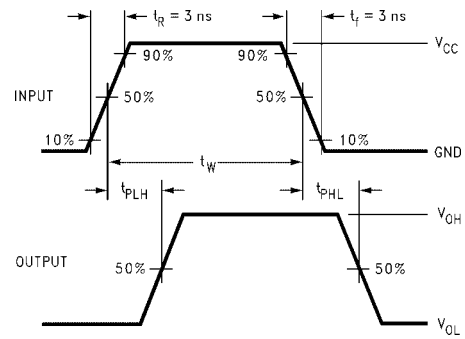
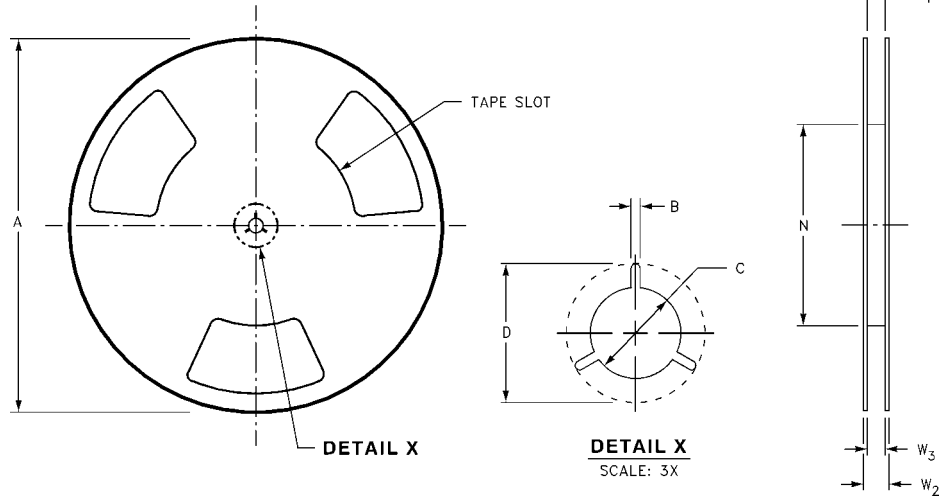


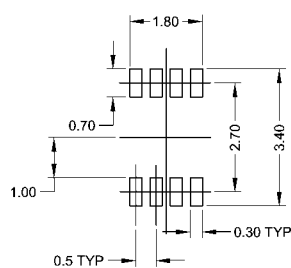
FIGURE 3. AC Waveforms

Tape and Reel Specification (Continued)

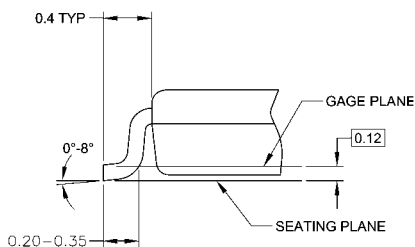
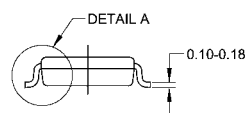
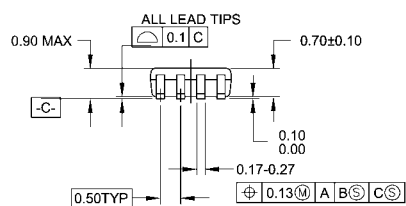
REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)



LAND PATTERN RECOMMENDATION



DETAIL A

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-187
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH,
AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

**8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide
Package Number MAB08A**

