



Dual P-Channel 12-V (D-S) MOSFET

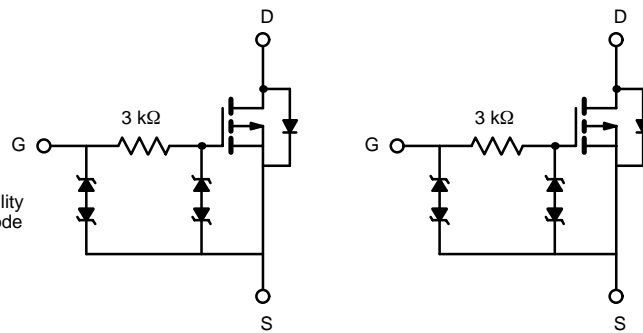
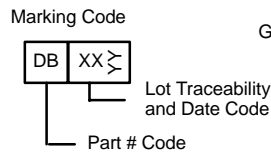
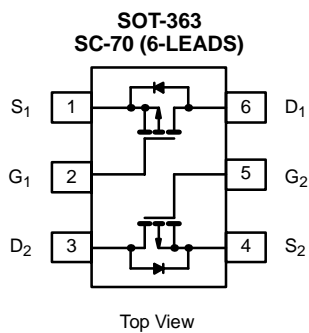
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-12	0.370 @ $V_{GS} = -4.5$ V	-1.15
	0.575 @ $V_{GS} = -2.5$ V	-0.92
	0.800 @ $V_{GS} = -1.8$ V	-0.78

FEATURES

- TrenchFET® Power MOSFETS: 1.8-V Rated
- ESD Protected: 3000 V
- Thermally Enhanced SC-70 Package

APPLICATIONS

- Load Switching
- PA Switch
- Level Switch



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	5 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	-12		V	
Gate-Source Voltage	V_{GS}	± 12			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	-1.15	-1.00	A
		$T_A = 85^\circ\text{C}$	-0.83	-0.73	
Pulsed Drain Current	I_{DM}	-3			
Continuous Diode Current (Diode Conduction) ^a	I_S	-0.61	-0.47		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	0.73	0.57	W
		$T_A = 85^\circ\text{C}$	0.38	0.30	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 5$ sec	130	170	$^\circ\text{C/W}$
		Steady State	170	220	
Maximum Junction-to-Foot (Drain)	R_{thJF}	80	100		

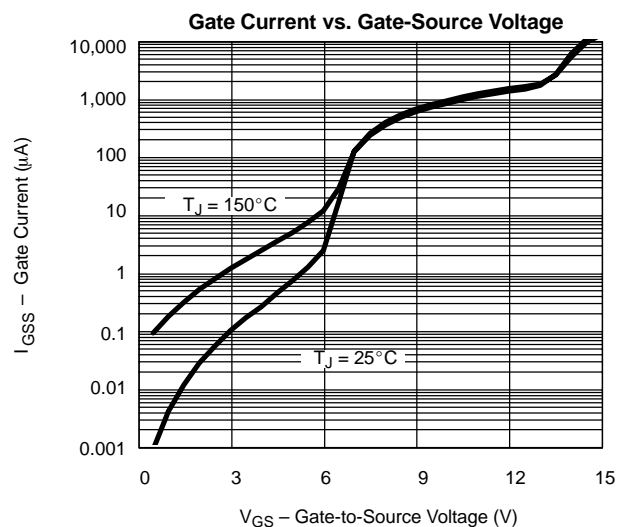
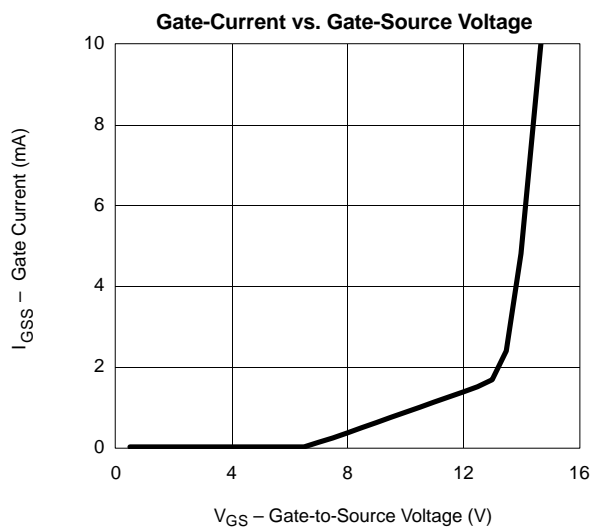
Notes
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -100\ \mu\text{A}$	-0.45			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 4.5\ \text{V}$			± 1.5	μA
		$V_{DS} = 0\ \text{V}, V_{GS} = \pm 12\ \text{V}$			± 10	mA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -9.6\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -9.6\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 85^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\ \text{V}, V_{GS} = -4.5\ \text{V}$	-2			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -4.5\ \text{V}, I_D = -1.0\ \text{A}$		0.300	0.370	Ω
		$V_{GS} = -2.5\ \text{V}, I_D = -0.81\ \text{A}$		0.470	0.575	
		$V_{GS} = -1.8\ \text{V}, I_D = -0.2\ \text{A}$		0.660	0.800	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\ \text{V}, I_D = -1.0\ \text{A}$		1.7		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -0.47\ \text{A}, V_{GS} = 0\ \text{V}$		-0.85	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -6\ \text{V}, V_{GS} = -4.5\ \text{V}, I_D = -1.0\ \text{A}$		1.3	2.0	nC
Gate-Source Charge	Q_{gs}			0.31		
Gate-Drain Charge	Q_{gd}			0.31		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\ \text{V}, R_L = 12\ \Omega$ $I_D \cong -0.5\ \text{A}, V_{GEN} = -4.5\ \text{V}, R_G = 6\ \Omega$		0.17	0.26	μs
Rise Time	t_r			0.47	0.71	
Turn-Off Delay Time	$t_{d(off)}$			0.96	1.4	
Fall Time	t_f			1.0	1.5	

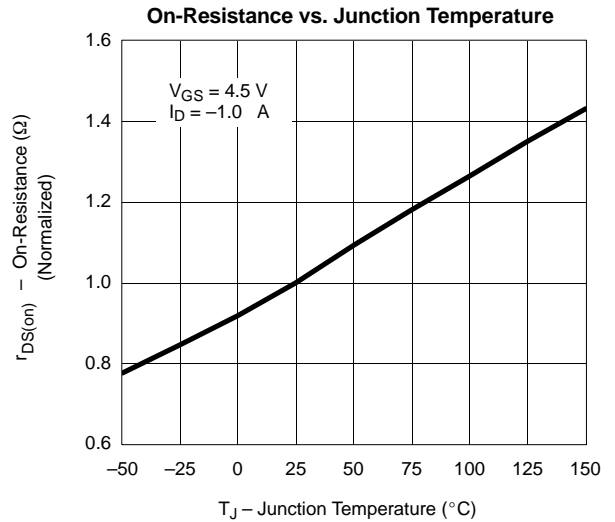
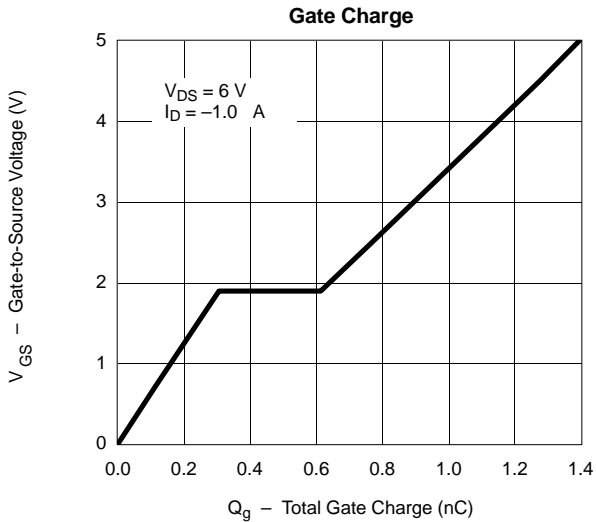
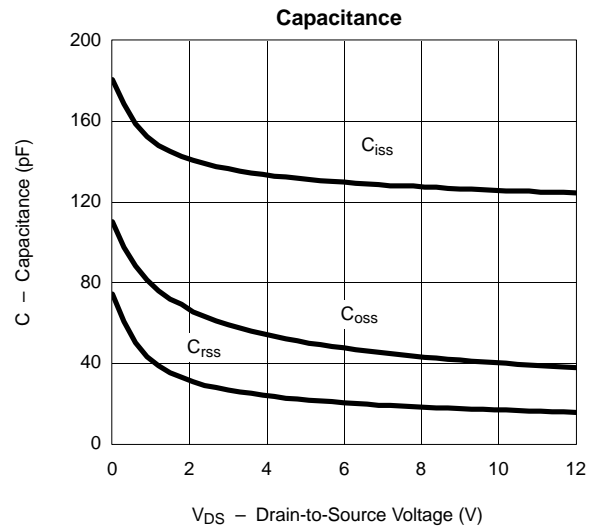
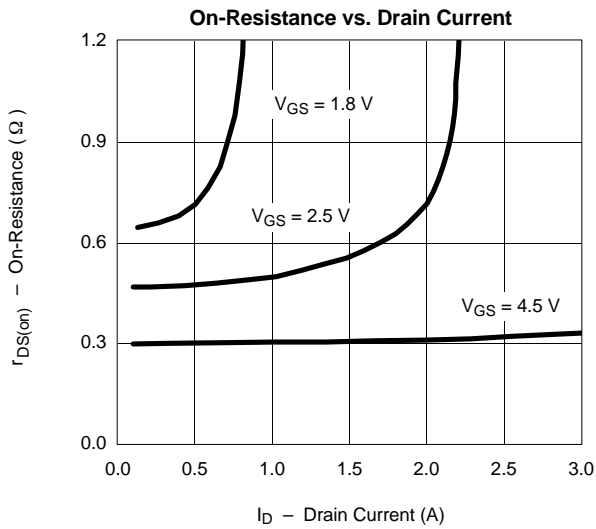
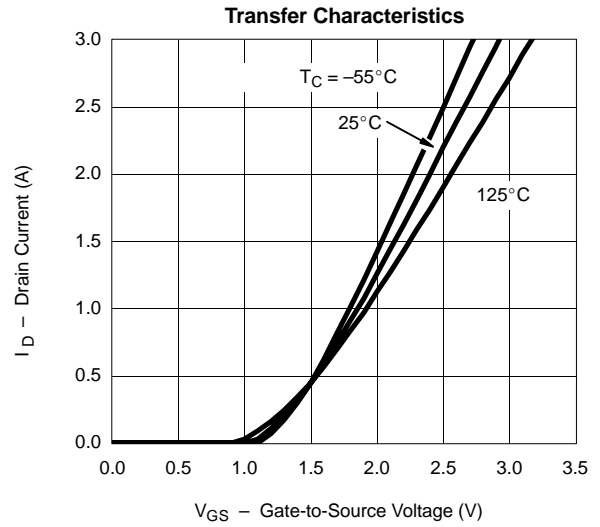
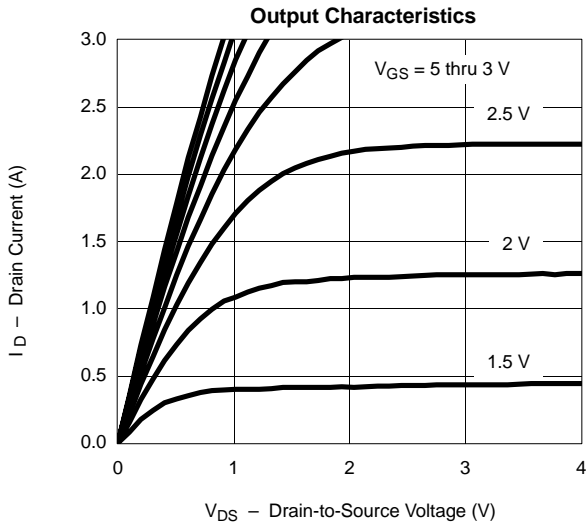
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

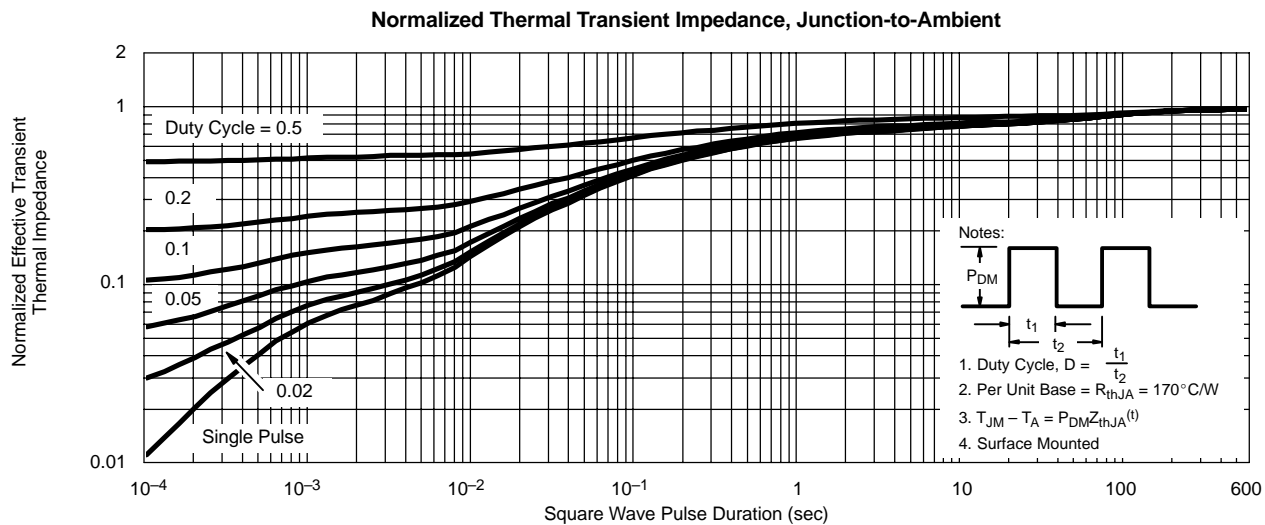
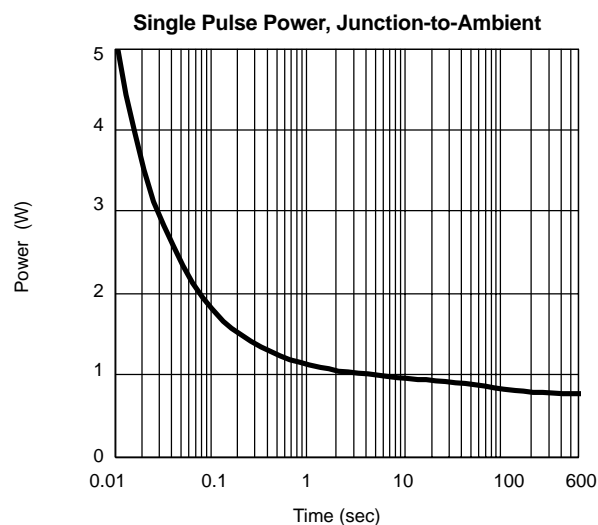
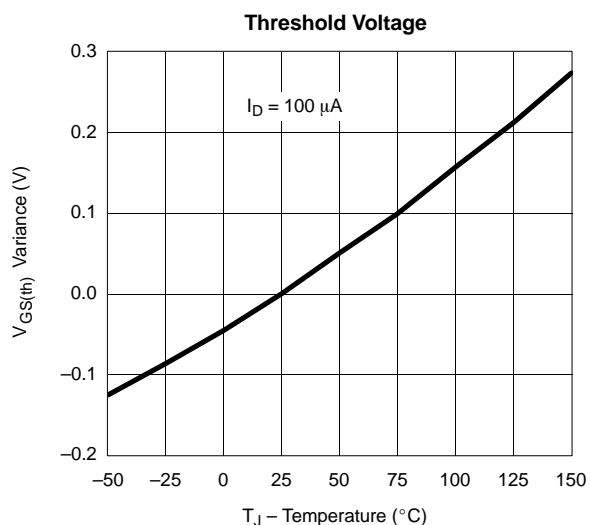
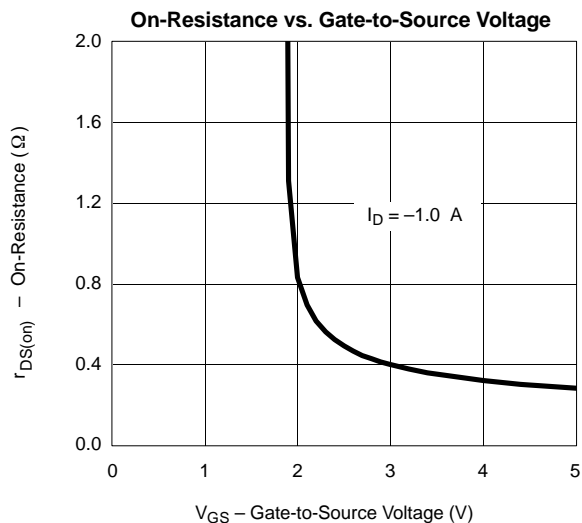
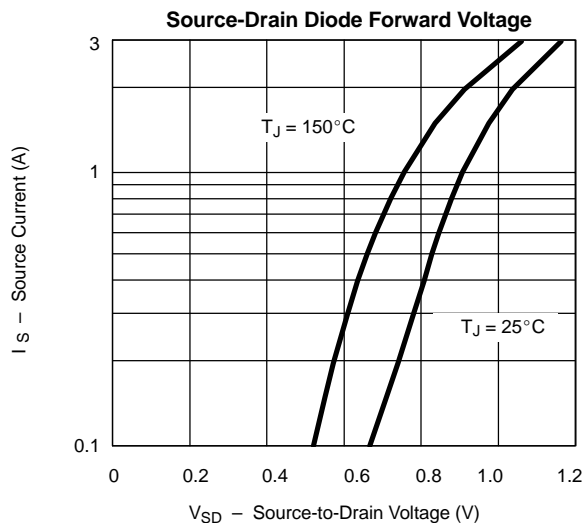
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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