TC9125BP

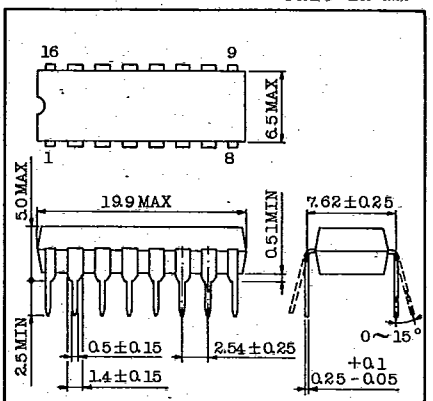
T-50-17

TC9125BP FM/AM (LW, MW, SW)/TV SYNTHESIZER PLL

TC9125BP is CMOS LSI developed for the digital tuning system and has the following features.

- The system design with high flexibility allows the applications of frequency synthesizers covering all the frequency ranges of FM/LW/SW/MW and TV.
- High speed programmable counter has been realized by TOSHIBA's unique circuitry and process, and 1/8 frequency divider can be used as the prescaller for receiving FM signals obtaining high S/N ratio.
- When combined with prescaller TD6102P, IF of FM receiving can be fine-tuned by 25kHz shifting with the center frequency of 10.7MHz. The channel step of 50 kHz for Europe can also be handled.

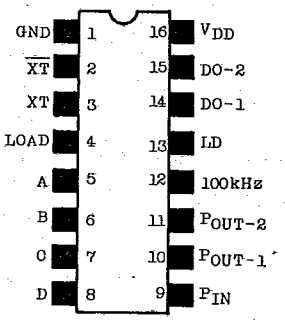
Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.16 leads.

JEDEC	—
TOSHIBA	3D16A-P

PIN CONNECTION



MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	-0.3 ∿ 10.0	V
Input Voltage	V_{IN}	-0.3 ∿ V_{DD}+0.3	V
Voltage Applied to Output Terminal	V_{OUT}	-0.3 ∿ V_{DD}+0.3	V
Power Dissipation	P_D	600	mW
Operating Temperature	Topr	-30 ∿ 70	°C
Storage Temperature	Tstg	-55 ∿ 125	°C

TC9125BP

T-50-17

- Having two phase comparator outputs, two kinds of low pass filters can be used without switching.
- TC9125BP has the input circuits most suitable for using a micro computer as its controller and the programming can be achieved through only five terminals, A through D and LOAD.
- The threshold voltage of the input terminals for program has been set low enough to eliminate limitation of power supply voltage when connected to a micro computer.
- Compact having 16 pin DIP arrangement.

FUNCTIONAL DESCRIPTION OF TERMINALS

PIN NO.	SYMBOL	NAME OF TERMINAL	DESCRIPTION OF FUNCTION AND OPERATION	REMARKS
1	GND	Ground Terminal		
2 3	$\overline{X_T}$ X_T	Crystal Oscillator Terminal	Terminal to connect 9.0 MHz crystal	Equipped with feedback resistor.
4	LOAD	Load Input Terminal	Input terminal for Read Command for the data on A through D. When this terminal is at "1" level, the data is read in and when it is at "0" level, the previous data is retained regardless of other inputs.	
5 6 7 8	A B C D	Program Data Input Terminals.	Input terminals for the reference frequency selection data and the frequency division ratio data for programmable counter.	

TC9125BP

T-50-17

PIN NO.	SYMBOL	NAME OF TERMINAL	DESCRIPTION OF FUNCTION AND OPERATION	REMARKS
9	P_{IN}	Programmable Counter Input Terminal	Input terminal of programmable counter.	Equipped with input amplifier
10 11	P_{OUT}-1 P_{OUT}-2	Programmable Counter Output Terminal	Frequency division output terminal of programmable counter. Connected to pre-scaller TD6102P for fine adjustment of IF frequency of FM and 50 kHz shifting in Europe. Signals from Pout-1 and Pout-2 are output at the points of different phase.	
12	100kHz	100kHz Clock Output Terminal	Output terminal of 100 kHz signal which can be utilized as the clock of micro computer.	
13	LD	Lockout Detection Terminal	Holds "H" level during lockout.	
14 15	DO-1 DO-2	Phase Comparator Output Terminals	Connected to low pass filters.	
16	V_{DD}	Supply Voltage Terminal		

TC9125BP

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta=25°C, V_{DD}=7.0V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
* Operating Supply Voltage Range	V_{DD}(1)		P_{IN}=11MHz, V_{IN}=1.7Vp-p	5.5	-	9.0	V
	V_{DD}(2)		P_{IN}=16MHz, V_{IN}=1.7Vp-p	7.0	-	9.0	V
* Operating Supply Current	I_{DD}(1)		V_{DD}=6.0V, P_{IN}=10MHz 9.0MHzX-Tal is connected to $X_T - \overline{X_T}$	-	6.0	12.0	mA
	I_{DD}(2)		V_{DD}=8.0V, P_{IN}=15MHz 9.0MHzX-tal is connected to $X_T - \overline{X_T}$	-	11.0	18.0	mA
(Programmable Counter)	(P_{IN})						
* Maximum Operating Frequency	f_{MAX}(1)		V_{DD}=5.5V, V_{IN}=1.7Vp-p	11	-	-	MHz
	f_{MAX}(2)		V_{DD}=7.0V, V_{IN}=1.7Vp-p	16	-	-	MHz
* Minimum Operating Frequency	f_{MIN}		V_{DD}=5.5∿9.0V, V_{IN}=1.7Vp-p	-	-	200	kHz
* Operating Input Amplitude	V_{IN}		V_{DD}=7.0V, P_{IN}=16MHz	1.7	-	6.0	Vp-p
(Reference Frequency Divider)	(X_T-$\overline{X_T}$)		V_{DD}=5.5V				
* Maximum Operating Frequency	f_{MAX}		9.0MHzX-Tal is connected to X_T-$\overline{X_T}$	9	-	-	MHz
(Program Input Terminal)	(A∿D, $(_{LOAD}$)						
* Threshold Voltage Range	Vth (1)		V_{DD}=6.0V	0.5	-	3.1	V
	Vth (2)		V_{DD}=8.0V	0.7	-	3.5	V

TC9125BP

T-50-17

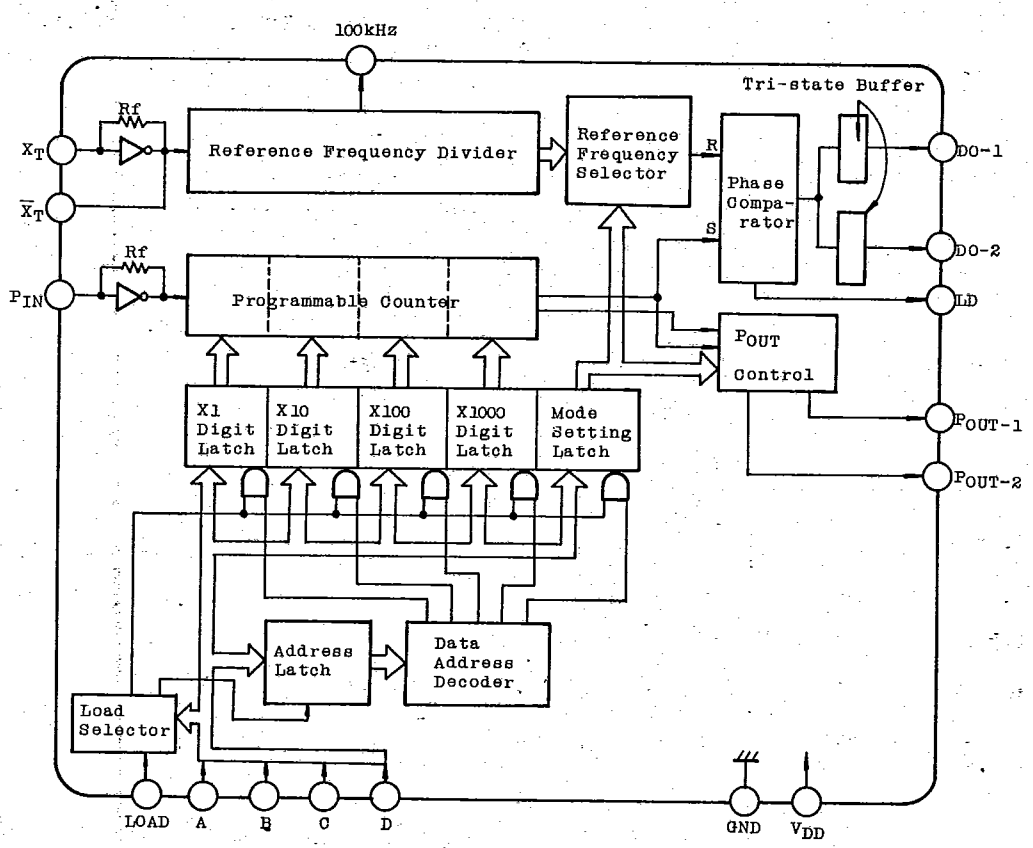
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Leakage Current	"H" Level	I_{IH}		V_{IH}=9.0V	-	-	10	μA
	"L" Level	I_{IL}		V_{IL}=0V	-	-	-10	μA
("H" Level Output Current)		(I_{OH})						
P_{OUT}-1,2 Output		$I_{OH}P_{OUT}$						
100kHz Output		I_{OH}100kHz		V_{OH}=6.0V	-0.3	-	-	mA
LD Output		I_{OH} DO						
DO - 1,2 Output		I_{OH} DO						
("L" Level Output Current)		(I_{OL})						
P_{OUT}-1,2 Output		$I_{OL}P_{OUT}$						
100kHz Output		I_{OL}100kHz						
LD Output		I_{OL} LD		V_{OL}=1.0V	0.3	-	-	mA
DO - 1,2 Output		I_{OL} DO						
(DO Tri-state Leakage Current)								
Leakage Current	"H" Level	I_{TLHDO}		V_{DD}=9.0V	-	-	100	nA
	"L" Level	I_{TLLDO}			-	-	-100	nA
Feedback resistors at X_T-$\overline{X_T}$ and P_{IN}		Rf		-	100	250	500	kΩ

Note: Temperature range of Ta=-30 ∿ 70°C for all the items marked with *.

TC9125BP

T-50-17

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION OF EACH BLOCK

1. REFERENCE FREQUENCY DIVIDER

1) The reference frequency divider consists of the crystal oscillator amplifier having externally connected 9.0 MHz crystal and the frequency divider which divides the oscillator output to generate the reference frequency.

TC9125BP

T-50-17

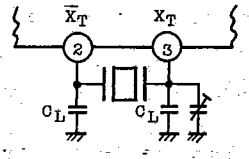
TC9125BP is provided with the following six kinds of reference frequencies to enable to be applicable for FM/LW/MW/SW and TV.

Table 1

Mode	LW	SW	AM_2	AM_1	FM	TV
Frequency Division Factor	9000	1800	1000	900	720	576
Reference Frequency [kHz]	1.0	5.0	9.0	10.0	12.5	15.625

2) One of reference frequencies is selected by the signal from the data latch for mode setting and fed to the reference input of the phase comparator.

3) The amplifier for crystal oscillator is equipped with the bias resistor making the external circuit very simple as shown in Fig. 1.



Crystal : 9.00MHz HC-18/u Type

C_L : 33pF

Fig. 1

4) The output terminal for 100 kHz is separately provided in the reference frequency divider and this signal can be utilized as the clock of micro processor which is the controller of TC9125BP.

100 kHz signal usually appears at 100 kHz output but 125 kHz signal will be seen only during TV mode.

TC9125BP

2. PROGRAMMABLE COUNTER

1) The programmable counter is the frequency divider which can control the frequency division factor according to the program data given externally and has the arrangement of four BCD digits (16 bits).

2) Since the programmable counter of TC9125BP is especially high speed, 1/8 frequency divider can be used for the prescaller of FM receiving.

3) The frequency division range of TC9125BP is

Frequency Division Factor N = 80 ∿ 9999

and the frequency division factor is same as the program data given by the controller.

Therefore, there is the difference which corresponds to the intermediate frequency in PLL of receiver between the receiving frequency and the oscillating frequency of VCO (local oscillator)to normally control the local oscillator, and the frequency division offset which corresponds to IF frequency is controlled by the controller side for TC9125BP.

4) The frequency division output of the programmable counter is fed to the signal input (S) of the phase comparator and compared with the output frequency of the reference frequency divider.

5) And this frequency divider output is fed to the P_{OUT} control circuit where the signal is output to programmable counter output terminals P_{OUT}-1 and P_{OUT}-2. By utilizing these two terminals, dedicated prescaller TD6102P is controlled to provide the capabilities of IF fine tuning for FM receiving and 50 kHz channel step for European areas.

Detail of this operation is described later.

6) As frequency input terminal P_{IN} of the programmable counter is equipped with a self biased amplifier, the input signal is given through capacitor coupling and small amplitude is enough for proper operation.

3. PHASE COMPARATOR

The phase comparator is the circuit block which compares the phases of reference frequency divider output and programmable counter output and controls VCO through the low pass filter to coincide the frequencies and the phases of these two signals.

1) Outputs of DO-1 and DO-2 Terminals (CMOS Tri-state Outputs)

a) When the phase of programmable counter frequency divider output lags behind that of reference frequency, DO-1 and DO-2 outputs become "L" level by turning on N-channel FET's for the period equivalent to the phase difference.

b) On the contrary, when it leads, DO-1 and DO-2 outputs become "H" level by turning on P-channel FET's for the period equivalent to the phase difference.

c) For the period when none of the aboves are seen, DO-1 and DO-2 outputs have high impedance by turning off both N-channel and P-channel FET's.

2) As TC9125BP is equipped with two tri-state outputs DO-1 and DO-2, two sets of low pass filters can be used without switching and the constants of low pass filters can be set to the optimum values for the multi-band applications.

3) Output of LD Terminal

a) LD terminal is provided to detect the unlock operational state of PLL loop.

TC9125BP

b) LD output becomes "H" level for the phase error time period during lock out. (Refer to Fig. 2)

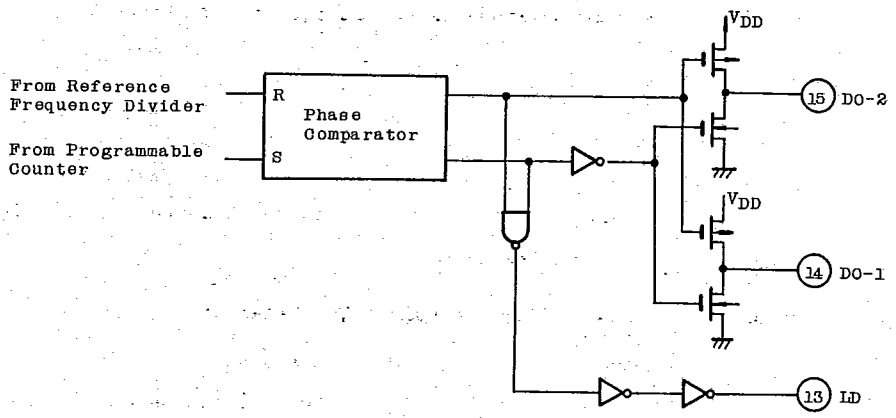


FIG. 2 CIRCUIT OF PHASE COMPARATOR BLOCK

4. P_{OUT} CONTROL CIRCUIT

1) TC9125BP is equipped two programmable counter outputs P_{OUT}-1 and P_{OUT}-2 and the output conditions of these two are controlled in the P_{OUT} control circuit by the signal from the reference frequency data latches.

2) The signals of P_{OUT}-1 and P_{OUT}-2 are output with different phases each other as shown in Fig. 3.

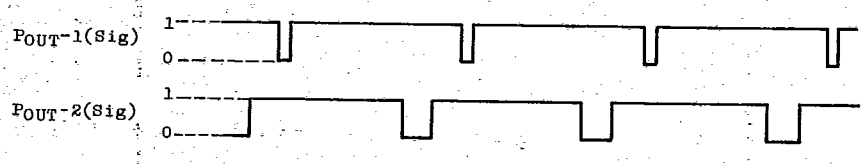


FIG. 3 OUTPUTS OF P_{OUT}-1 AND P_{OUT}-2

5. DATA LATCHES

1) Because the mode setting data for reference frequency selection and P_{OUT} control and the data to set the programmable counter frequency division factor are input from four input terminals A through D in 4 bit serial for TC9125BP, 4bits × 5 latch circuits are provided in LSI where the program data is stored being converted to parallel.

2) As the circuit threshold voltage of program input terminals A through D and LOAD has been set low eliminating limitation of power supply voltage for connecting micro computer as its controller, it can be directly connected without any interface circuits.

3) The configuration of data latches is as shown in Fig. 4.

When the binary input signal from A through D is from 11 (hexadecimal B) to 15 (hexadecimal F), LOAD signal is sent to the address latches through the load selection circuit and the data is stored in the address latches. Then a data latch corresponding to the input data is designated by the address decoder.

And when the input from A through D is 0 ∿ 9, LOAD signal is sent to the data latches and the input data is stored in the data latchs designated by the address decoder.

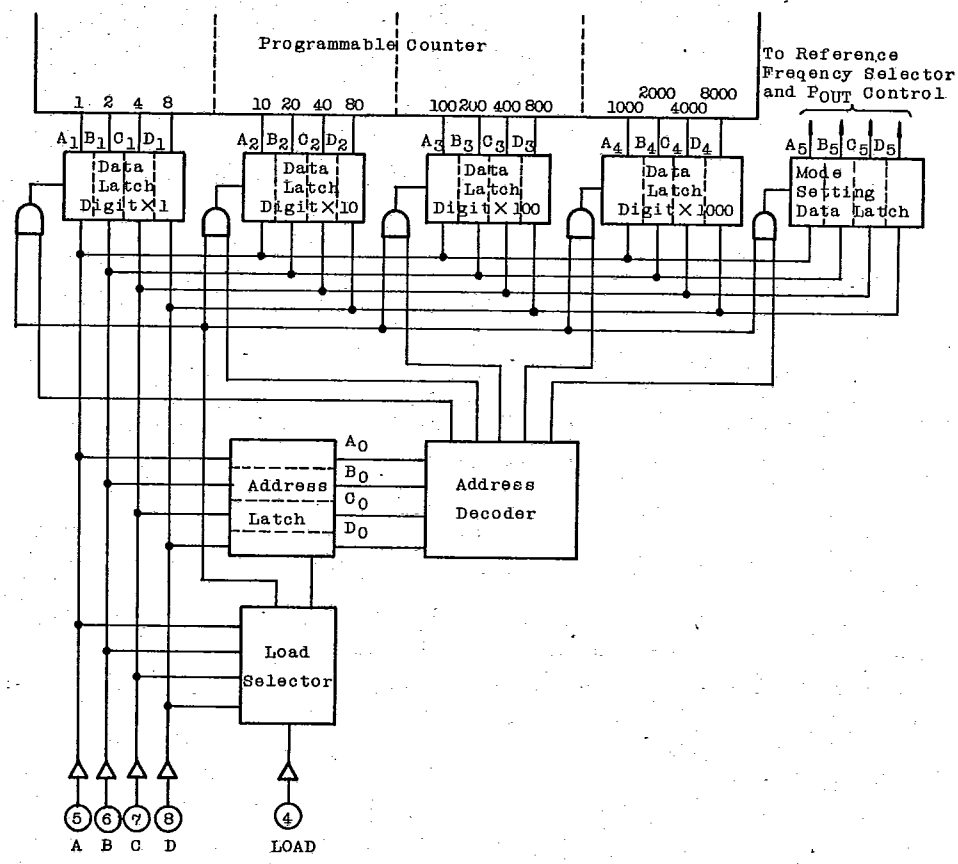


Fig. 4 CONFIGURATION OF DATA LATCH

RECEIVING BAND OF TC9125BP

TC9125BP has the system structure with high flexibility enabling to handle all the bands of FM/LW/MW/SW and TV.

TC9125BP

T-50-17

In FM band, receiving with 50 kHz channel space has become possible for European areas by means of coupled control with dedicated prescaller TD6102P in addition to domestic FM and international FM.

1. The following six kinds of reference frequencies are provided as shown in Table 1.

   1 kHz, 5 kHz, 9 kHz, 10kHz, 12.5 kHz, 15.625 kHz

   The programmable counter does not have the frequency division factor offset. Table 1 shows each receiving band corresponding to reference frequency, but what reference frequency is used for what band can be freely selected according to the design specification of micro computer which is to be the controller. In this case, the frequency division factor offset corresponding to IF frequency is set accordingly by the controller side.

2. If reference frequency of FM band is set to 12.5 kHz, 1/8 prescaller can be used to realize high S/N ratio. The prescaller for TV band is 1/64.

PROGRAMMING OF TC9125BP

1. TC9125BP has the optimum input circuits for using a micro computer as its controller and the programming can be achieved through five terminals, A through D and LOAD.

   As the program data which instruct the operations of TC9125BP, there are the mode setting data to select the reference frequency and to control the P_{OUT} output and the data to set the programmable counter frequency division factor. These data are input in 4 bit serial from four terminals A through D and converted to parallel in LSI being set in 4 bits × 5 latches.

TC9125BP

2. In order to determine in what latch the data is set, the data which designates the address of latch is input first, then the data to be set in the latch is input. Whether the input data is frequency division factor data, mode setting data or address data is automatically selected in LSI according to the contents of A through D.

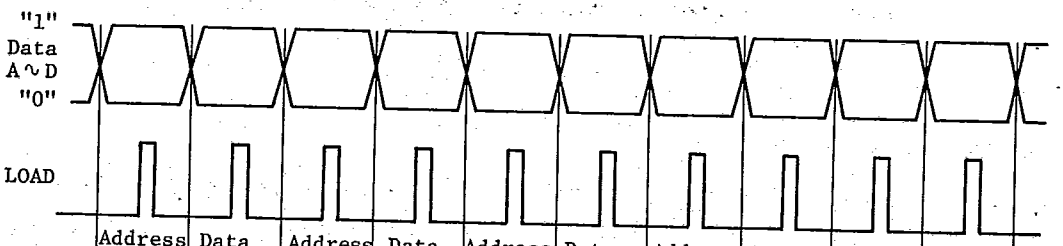
The address of each latch is as shown in Table 2.

Table 2 Latch Address

Latch	Digit × 1	Digit × 10	Digit × 100	Digit × 1000	Mode Setting
Address	F = 11	F = 12	F = 13	F = 14	F = 15

Where, $F = 1 \cdot A + 2 \cdot B + 4 \cdot C + 8 \cdot D$, A, B, C, D = "1" or "0"

3. Timing of Program Input



Data Input	Address designation of unit's	Data set of unit's	Address designation of ten's	Data set of ten's	Address disignation of hundred's	Data set of hundred's	Address disignation of thousand's	Data set of thousand's	Address designation of mode setting	Data set of mode setting
A	1	A_1	0	A_2	1	A_3	0	A_4	1	A_5
B	1	B_1	0	B_2	0	B_3	1	B_4	1	B_5
C	0	C_1	1	C_2	1	C_3	1	C_4	1	C_5
D	1	D_1	1	D_2	1	D_3	1	D_4	1	0
	F=11	F=0∿9	F=12	F=0∿9	F=13	F=0∿9	F=14	F=0∿9	F=15	F=0∿7

Data input is performed in 4 bit binary.

4. The mode of reference frequency and P_{OUT} terminals varies according to mode setting data A_5, B_5, C_5 (D_5 = "0") as shown in Table 3.

Table 3

REFERENCE FREQUENCY DATA			REFERENCE FREQUENCY [kHz]	P_{OUT}-1	P_{OUT}-2
A_5	B_5	C_5			
0	0	0	1	Sig.	1
1	0	0	5	Sig.	1
0	1	0	9	Sig.	1
1	1	0	10	Sig.	1
0	0	1	12.5	1	Sig'.
1	0	1	12.5	Sig.	Sig'.
1	1	1	15.625	Sig.	Sig'.

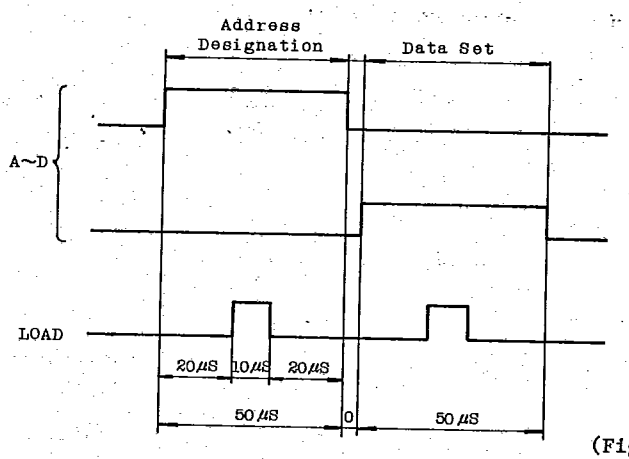
"1" indicates that "H" level is retained.
"Sig." and "Sig'." are frequency divided outputs of the programmable coutner. (Refer to Fig. 3.)

5. Load signal input is the input to instruct to read in the data given on terminals A through D. While this input is "1", the data on A through D are read into the internal latches and when it is "0", the previously read data are retained regardless of A through D.

In order to prevent erroneous data read operation at the time of changing data on A through D, it is desirable to give the signal described in 3 Timing of Program Input.

TC9125BP

6. Minimum Pulse Width of Input Data



(Fig. 5)

7. It is effective for improving S/N ratio of the radio set to transfer the input data once immediately after selection of station and to inhibit the transfer afterward keeping all of terminals A through D and LOAD at "L" level.

8. Example of Program

As an example of program for TC9125BP, the timing chart of A through D when receiving 82.5 MHz of Japan FM band (reference frequency : 12.5 kHz) is shown in Fig. 6.

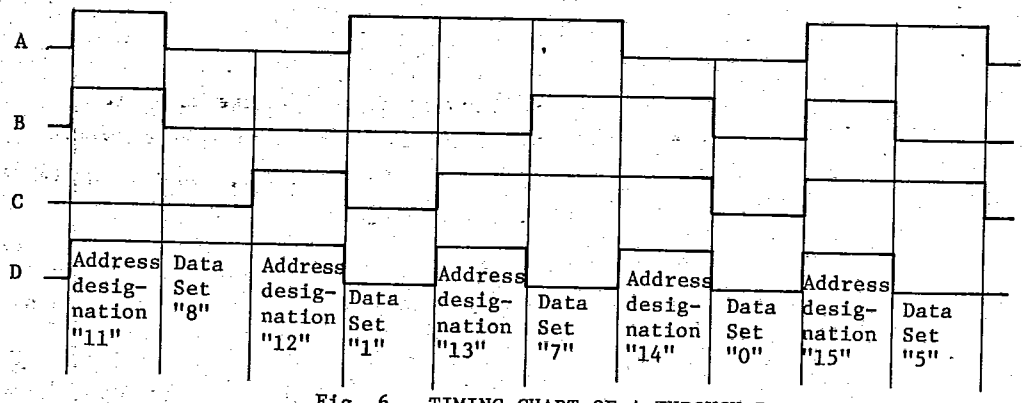


Fig. 6 TIMING CHART OF A THROUGH D

The frequency division factor of programmable counter is 825 - 107 = 718.

* There is FM/AM synthesizer controller TC9128P/29P using one chip micro computer TCP4620P as the controller of TC9125BP.

FINE ADJUSTMENT OF INTERMEDIATE FREQUENCY FOR FM RECEIVING

Since IF frequency in FM band of TC9125BP can be freely selected from seven kinds of frequencies, ±25, ±50 and ±75 kHz around standard 10.7 MHz. the variations of IF filters used can be compensated realizing ideal receiving condition.

This operation is achieved by the program data control by the controller and the combination of TC9125BP and prescaller TD6102P. The operation is described in detail below.

1. The basic principles of this operation are as follows.

   1) 12.5 kHz is selected as the reference frequency of TC9125BP and TD6102P is used as the prescaller.

   2) It is required for the controller to have the function which arbitrarily forces the frequency division data sent to TC9125BP to be -1.

   3) When one of P_{OUT}-1 and P_{OUT}-2 of TC9125BP is connected to +25 kHz terminal of TD6102P, the frequency of local oscillator is shifted by +25 kHz.

   4) Similarly, when one of P_{OUT} is connected to +50 kHz terminal, it is shifted by +50 kHz.

   5) When both of +25 kHz and +50 kHz terminals are connected to one of P_{OUT}, it is shifted by +75 kHz.

TC9125BP

6) Since programmable counter frequency divider outputs P_{OUT}-1 and P_{OUT}-2 are output with different phases, if both of these are connected to +25 kHz terminal, it is shifted by +50 kHz.

7) Similarly, if both of P_{OUT} are connected to +50 kHz terminal, it is shifted by +100 kHz.

8) If both of P_{OUT}-1 and P_{OUT}-2 are connected to both of +25 kHz an +50 kHz, it is shifted by +150 kHz.

However, the above descriptions are applicable when the frequency division outputs exist on both terminals of P_{OUT}-1 and P_{OUT}-2.

9) When the frequency division data is forced to be -1 by the controller, the local oscillator is shifted by -100 kHz.

10) In the case of domestic FM, when the local oscillator frequency is shifted by $+\Delta f$, IF frequency will be 10.7 MHz - Δf and when shifted by - Δf, IF will be 10.7 MHz + Δf.

11) In the case of international FM, on the contrary, when shifted by + Δf, IF will be 10.7 MHz +Δf and when shifted by Δf, IF will be 10.7 MHz - Δf.

2. An example of connecting TC9125BP and TD6102P is shown.

The mode setting data sent to TC9125BP are A_5 = "1", B_6 = "0" and C_5 = "1" (F = 5).

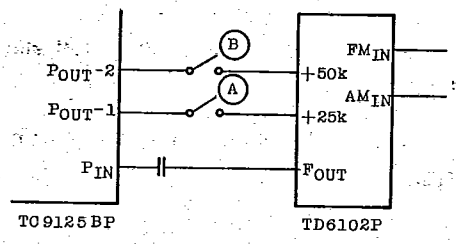


Fig. 7

3. Connections for performing seven kinds of IF fine adjustments in Fig. 7 are as shown in the table below.

Table 4

DESIRED IF FREQUENCY		DOMESTIC FM			INTERNATIONAL FM		
IF [MHz]	Δ IF [kHz]	(A)	(B)	FREQUENCY DIVISION FACTOR - 1	(A)	(B)	FREQUENCY DIVISION FACTOR - 1
10.775	+75	0		0	0	0	
10.750	+50		0	0		0	
10.725	+25	0	0	0	0		
10.700	0						
10.675	-25	0			0	0	0
10.650	-50		0			0	0
10.625	-75	0	0		0		0

(Notes) 1. 0 in the columns of (A) and (B) indicates that switch (A) and/or switch (B) should be turned on.

2. 0 in the column of Frequency division factor-1 indicates that the frequency division data sent to TC9125BP should be -1 shifted by the controller.

4. IF fine adjustment can be achieved with 50 kHz Channel Step in FM Band in Europe, but it is explained in the item of 50 kHz Channel Step.

5. IF Fine Adjustment without -1 Shift Function in Controller

As described above, it is required to have the function which performs -1 shift of frequency division data in the controller for seven kinds of IF fine adjustments, but it is also possible to achieve IF fine adjustment without this function. In this case, however, there are five kinds of IF fine adjustments.

1) The controller should be so designed that the frequency division data to TC9125BP in FM band has been -1 shifted from the actual frequency division data in advance.

Namely, the frequency division data in FM is always programmed in TC9125BP with the value shifted by -1.

2) The mode setting data of TC9125BP shall be A_5 = "1", B_5 = "0" and C_5 = "1".

3) Connection of TC9125BP and TD6102P is shown in Fig.8.

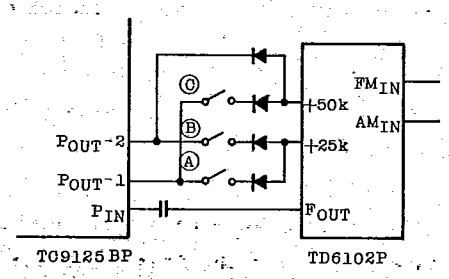


Fig. 8

4) Table 5 shows the connections for performing IF fine adjustment without the controller having the function of shifting the frequency division data by -1.

Table 5

DESIRED IF FREQUENCY		DOMESTIC FM			INTERNATIONAL FM		
IF [kHz]	⊿IF [kHz]	Ⓐ	Ⓑ	Ⓒ	Ⓐ	Ⓑ	Ⓒ
10.750	+50				0	0	0
10.725	+25		0			0	0
10.700	0			0			0
10.675	-25		0	0		0	
10.650	-50	0	0	0			

Note: 0 indicates that the respective switch should be turned ON.

APPLICATION OF 50 KHz Channel Step in FM Band

The channel space of domestic FM and international FM is 100 kHz, however, there are some areas in Europe where the spacing is only 50 kHz. TC9125BP can be used in the radio sets for these areas. And IF fine adjustment with 50 kHz step can be achieved.

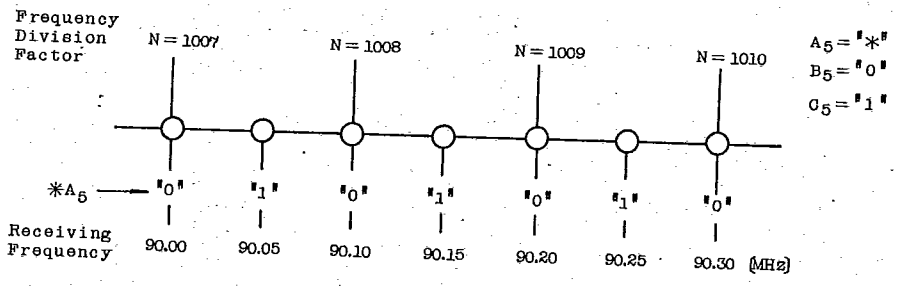
1. Basic operation of TC9125BP with 50kHz channel step is as follows.

1) As shown in Table 3, the output of P_{OUT}-1 terminal of TC9125BP can be turned on/off by the signal of mode setting data A_5 keeping the reference frequency at 12.5 kHz.

Namely, when A_5, B_5, C_5 = 1, 0, 1, the frequency division output signal appears on P_{OUT}-1 and when A_5, B_5, C_5 = 0, 0, 1, the frequency division output stops keeping P_{OUT}-1 at "H" level.

2) When the frequency division output of programmable counter is connected to +50 kHz terminal of prescaller, the local oscillator frequency is shifted by +50 kHz and consequently the receiving frequency is also shifted by +50 kHz

2. Therefore, P_{OUT}-1 terminal and +50 kHz terminal of prescaller is connected together. If the programe data is varied in such manner that A_5 = "0" with the frequency division data is N, then A_5 = "1" keeping the data N as it is, and A_5 = "0" at the same time as N is stepped up to N+1,... the receiving frequency can be scanned with 50 kHz step.



3. IF Fine Adjustment with 50 kHz Channel Step

1) IF fine adjustment of TC9125BP is further advanced providing two programmable counter frequency division output terminals (P_{OUT}-1 and P_{OUT}-2) enabling IF fine adjustment with 50 kHz channel step for European areas. Namely, always connecting P_{OUT}-1 terminal to +50 kHz terminal, as previously explained, if P_{OUT}-2 terminal is connected to +25 kHz or +50 kHz terminal, seven kinds of IF fine adjustments can be achieved.

2) In order to achieve fine adjustment of negative side, the controller is equipped with the function that the programmable counter frequency division data to TC9125BP in FM band can be arbitrarily decremented by -1.

TC9125BP

T-50-17

3) Fig. 9 illustrates the connection of IF fine adjustment with 50 kHz channel step.

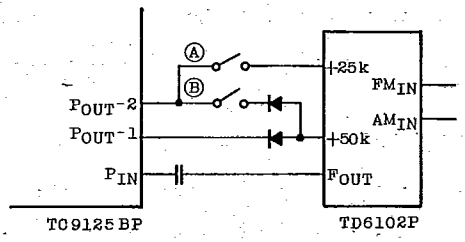


FIG. 9 CONNECTION FOR IF FINE ADJUSTMENT

4) The connections to perform seven kinds of IF fine adjustments in Fig. 9 are as shown in Table 6.

Table 6

DESIRED IF FREQUENCY		50 kHz STEP FOR EUROPEAN FM		
IF [MHz]	Δ IF [kHz]	Ⓐ	Ⓑ	FREQUENCY DIVISION FACTOR -1
10.775	+75	0	0	
10.750	+50		0	
10.725	+25	0		
10.700	0			
10.675	-25	0	0	0
10.650	-50		0	0
10.625	-75	0		0

TC9125BP

(Notes) 1. 0 in the columns of Ⓐ and Ⓑ indicates that switches Ⓐ and/or Ⓑ should be turned on.

2. 0 in the column of frequency division factor -1 indicates that the frequency division data sent to TC9125BP is -1 shifted by the controller.

CONFIGURATION OF ACTIVE LOW PASS FILTER

The low pass filter of PLL is to convert the digital output from the phase comparator to analog output voltage, which controls VCO.

As an example here, active low pass filter with high input impedance obtained by Darlington connection of FET and NPN transistor is shown.

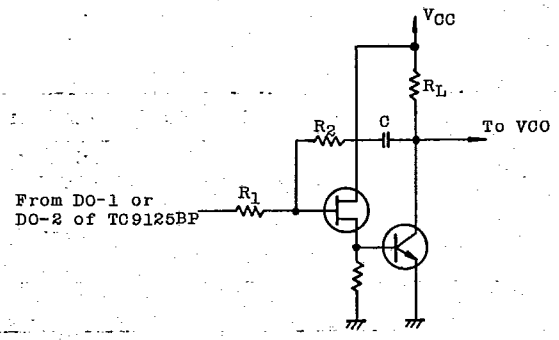


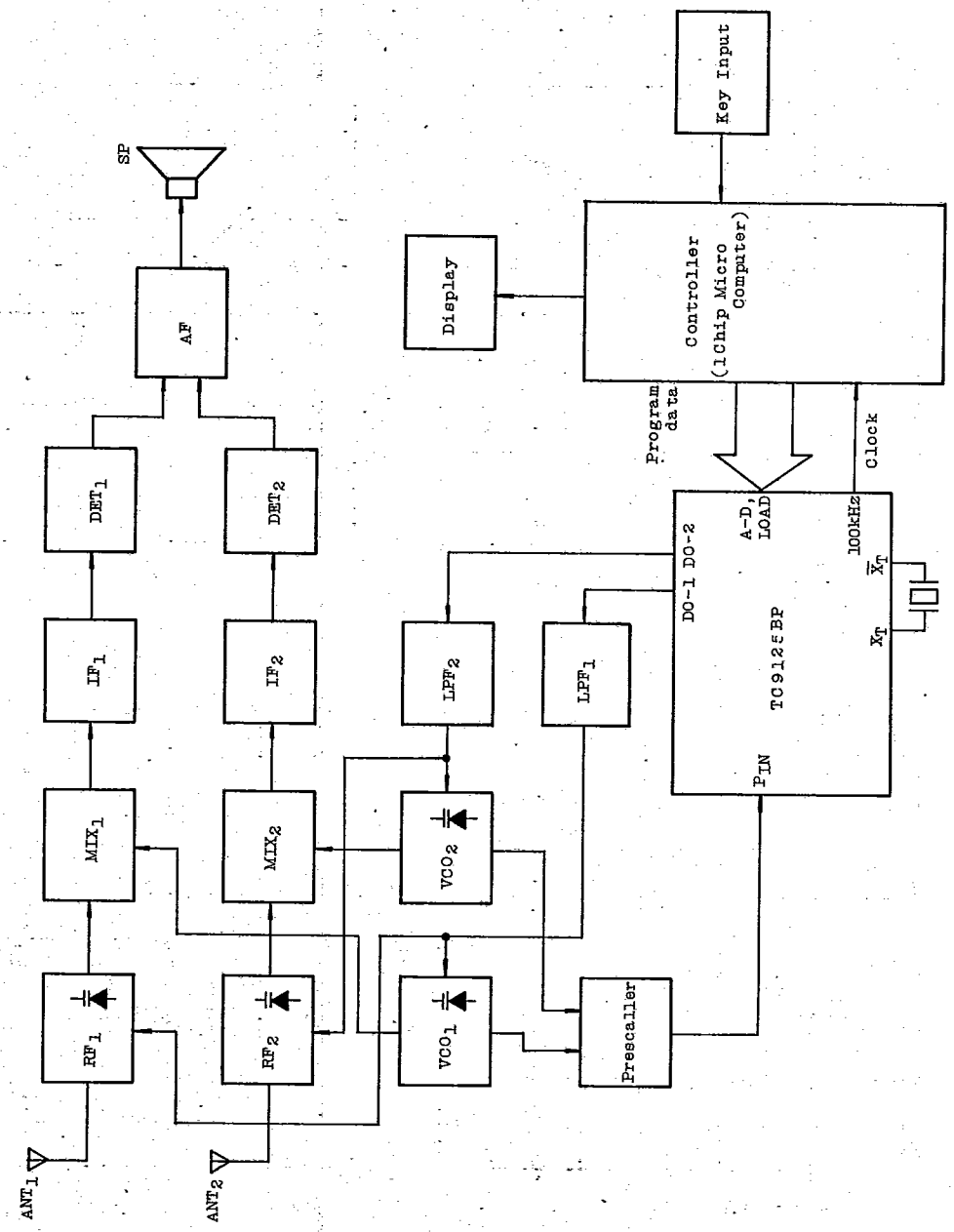
FIG. 10 LOW PASS FILTER CIRCUIT

(Note) : Although TC9125BP is equipped with two terminals of phase comparator outputs, it is not required to use both of them.

TC9125BP

T-50-17

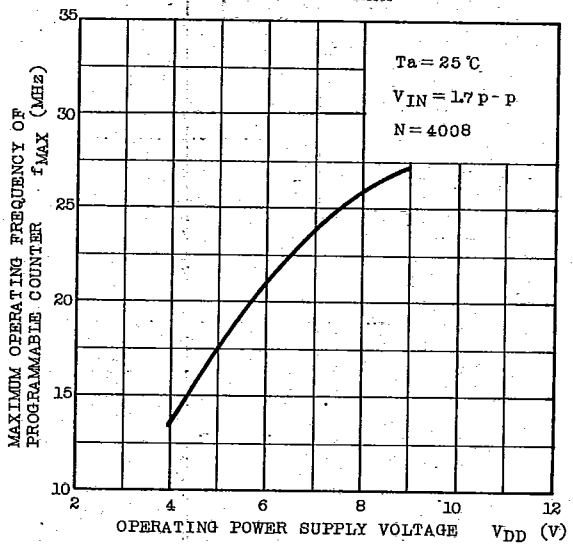
BLOCK DIAGRAM OF MULTI BAND PLL SYNTHESIZER SYSTEM



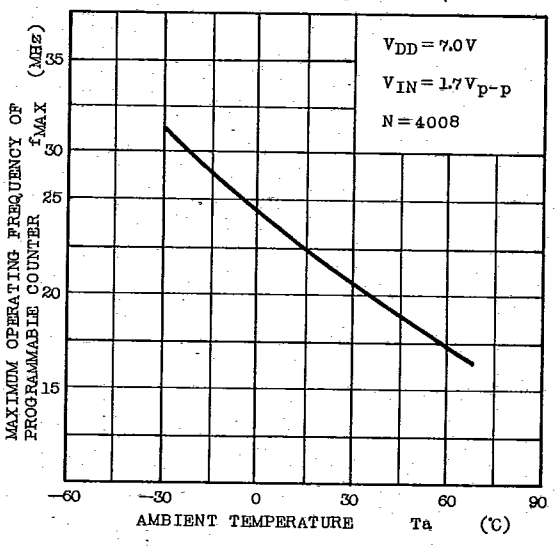
TC9125BP

T-50-17

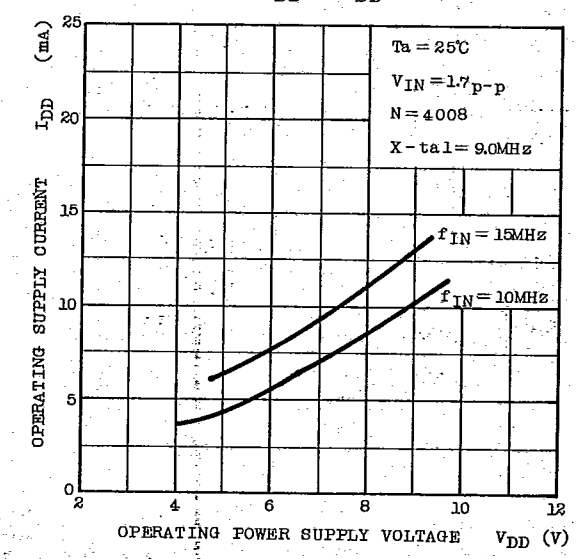
V_{DD} – f_{MAX}



Ta – f_{MAX}



V_{DD} – I_{DD}



V_{DD} – V_{th}