

## N-CHANNEL POWER MOS TRANSISTORS

### HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

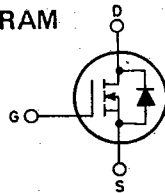
V <sub>DSS</sub>	R <sub>DS(ON)</sub>	I <sub>D</sub>
200V	0.75Ω	6A
250V	1.2 Ω	6A

### ABSOLUTE MAXIMUM RATINGS

		SOT-82 TO-220 TO-3	SGSP216 SGSP316 SGSP516	SGSP217 SGSP317 SGSP517
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)		250V	200V
V <sub>DGR</sub>	Drain-gate voltage (R <sub>GS</sub> = 20 KΩ)		250V	200V
V <sub>GS</sub>	Gate-source voltage			±20V
I <sub>D</sub>	Drain current (continuous) T <sub>case</sub> = 25°C at T <sub>case</sub> = 100°C			6A 3.8A
I <sub>DM</sub> (*)	Drain current (pulsed)			24A
I <sub>DLM</sub> (*)	Drain inductive current, clamped			24A
P <sub>tot</sub>	Total dissipation at T <sub>case</sub> = 25°C Derating factor		SOT-82 50W 0.4W/°C	TO-220 75W 0.6W/°C
T <sub>stg</sub>	Storage temperature			TO-3 75W 0.6W/°C
T <sub>J</sub>	Max. operating junction temperature			-55 to 150°C 150°C

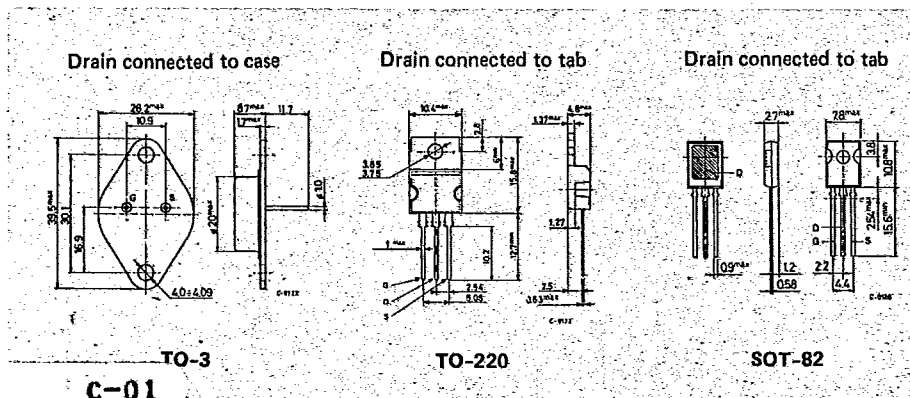
(\*) Pulse width limited by safe operating area

### INTERNAL SCHEMATIC DIAGRAM



### MECHANICAL DATA

Dimensions in mm

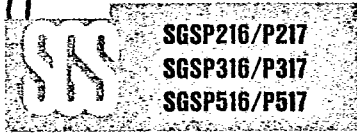


1896

C-01

9/85

C-78



**THERMAL DATA**

		SOT-82	TO-220	TO-3
$R_{th\ j-case}$	Thermal resistance junction-case max	2.5°C/W	1.6°C/W	1.6°C/W
$T_L$	Maximum lead temperature for soldering purpose	275		°C

**ELECTRICAL CHARACTERISTICS** ( $T_{case} = 25^\circ C$  unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
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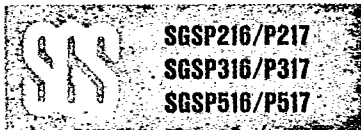
**OFF**

$V_{(BR)\ DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A$ $V_{GS} = 0$ for SGSP216/P316/P516 for SGSP217/P317/P517		250 200	V V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max. Rating}$		250	$\mu A$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\ V$		100	nA

**ON\***

$V_{GS\ (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu A$		2	4	V
$V_{DS\ (on)}$	Drain-source voltage	$V_{GS} = 10V$ $I_D = 3\ A$ for SGSP216/P316/P516 for SGSP217/P317/P517 $V_{GS} = 10\ V$ $I_D = 6\ A$ for SGSP216/P316/P516 for SGSP217/P317/P517 $V_{GS} = 10\ V$ $I_D = 3\ A$ $T_{case} = 100^\circ C$ for SGSP216/P316/P516 for SGSP217/P317/P517			3.60 2.25 8.10 5.00 7.20 4.50	V V V V V V
$R_{DS\ (on)}$	Static drain-source on resistance	$V_{GS} = 10\ V$ $I_D = 3\ A$ for SGSP216/P316/P516 for SGSP217/P317/P517			1.20 0.75	$\Omega$ $\Omega$
$g_{fs}$	Forward transconductance	$V_{DS} = 25V$ $I_D = 3\ A$		1.5		mho

73C 17357 D T-39-11



**ELECTRICAL CHARACTERISTICS** (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit.
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**DYNAMIC**

$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$	380	500	pF
$C_{oss}$	Output capacitance		100	130	pF
$C_{rss}$	Reverse transfer capacitance		50	65	pF

**SWITCHING**

$t_d(\text{on})$	Turn-on time	$V_{CC} = 100\text{ V}$ $I_D = 2.5\text{ A}$ $V_I = 10\text{ V}$ $R_I = 50\Omega$ (see test circuit)	27		ns
$t_r$	Rise time		27		ns
$t_d(\text{off})$	Turn-off delay time		30		ns
$t_f$	Fall time		30		ns

**SOURCE DRAIN DIODE**

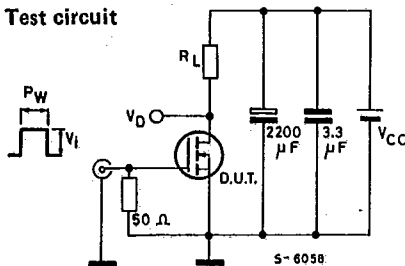
$I_{SD}$	Source drain current			6	A
$I_{SDM}(\bullet)$	Source drain current (pulsed)			24	A
$V_{SD}$	Forward on voltage	$I_{SD} = 6\text{ A}$ $V_{GS} = 0$		1.3	V
$t_{on}$	Turn-on time	$I_{SD} = 6\text{ A}$ $V_{GS} = 0$ $di/dt = 100\text{ A}/\mu\text{s}$	100		ns
$t_{rr}$	Reverse recovery time		180		ns

\* Pulsed: pulse duration  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$

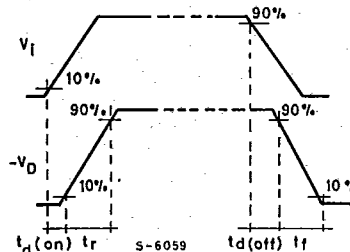
( $\bullet$ ) Pulse width limited by safe operating area.

**SWITCHING TIMES RESISTIVE LOAD**

Test circuit



Waveforms

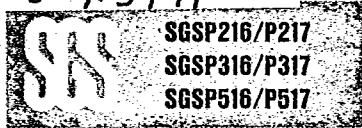


Pulse width  $\leq 100\mu\text{s}$

Duty cycle  $\leq 2\%$

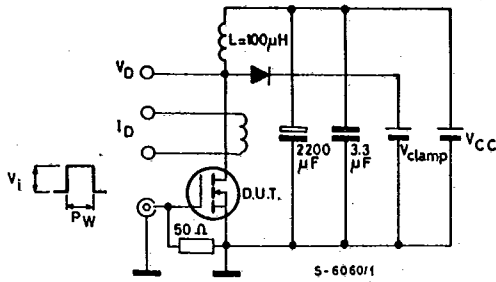
$V_I = 10\text{ V}$

C-80

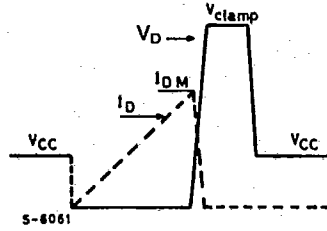


**CLAMPED INDUCTIVE LOAD**

Test circuit



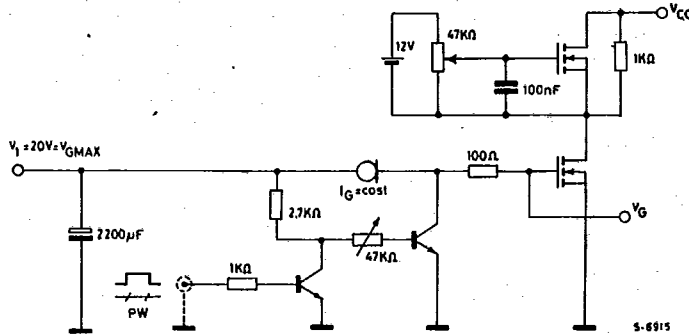
Waveforms



$V_1 = 12V$

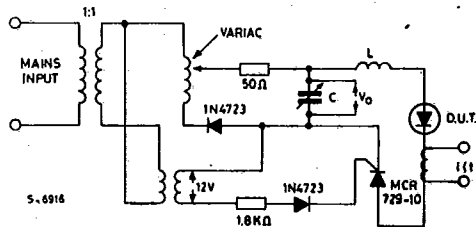
Pulse width: adjusted to obtain specified  $I_{DM}$ .  $V_{clamp} = 0.75 V_{(BR) DSS}$

**GATE CHARGE TEST CIRCUIT**

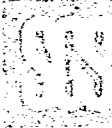


PW adjusted to obtain required  $V_G$

**DIODE BODY-DRAIN  $t_{rr}$  MEASUREMENT**

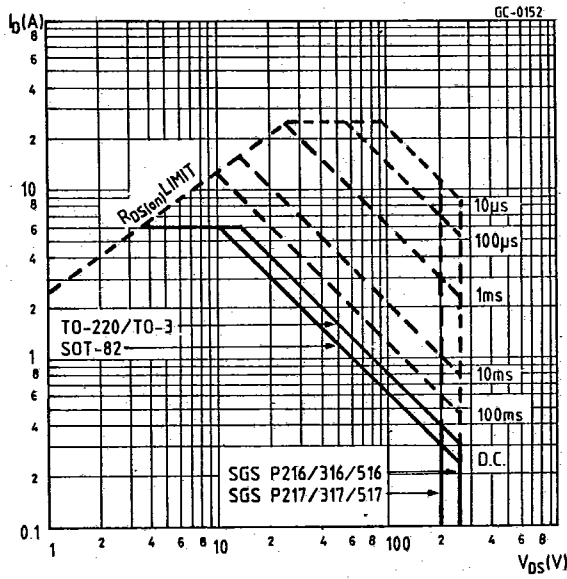


Jedec test circuit

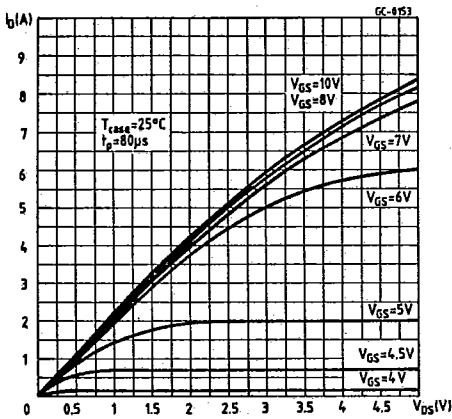


SGSP216/P217  
 SGSP316/P317  
 SGSP516/P517

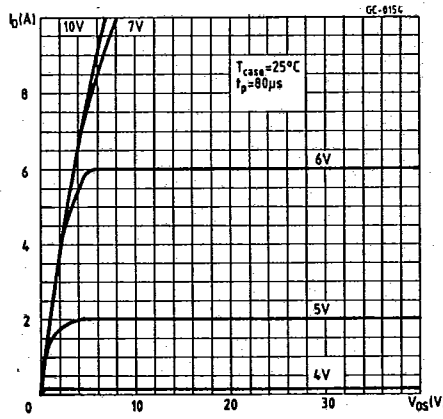
Safe operating areas



Output characteristics



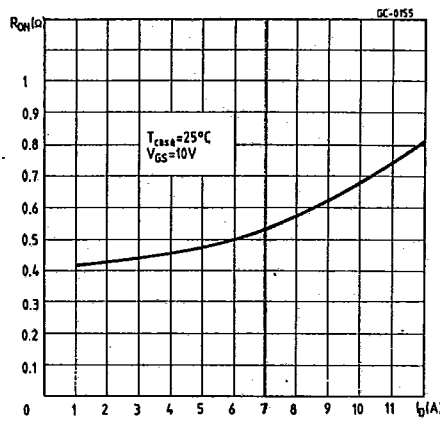
Output characteristics



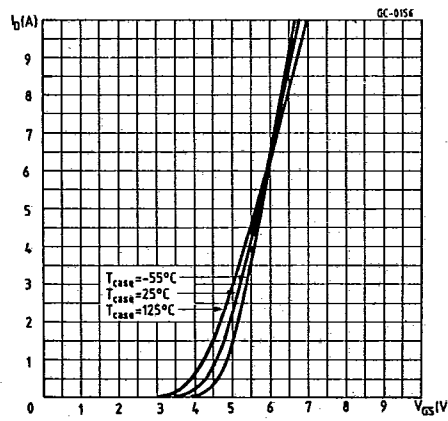


SGSP216/P217  
 SGSP316/P317  
 SGSP516/P517

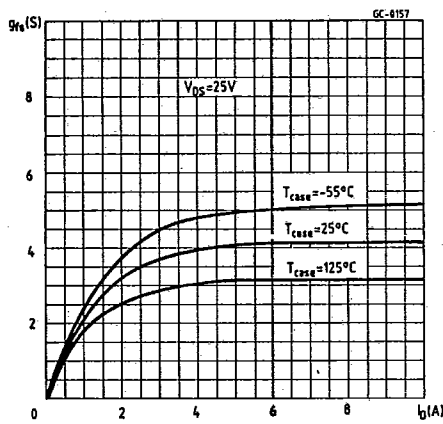
Static drain-source on resistance



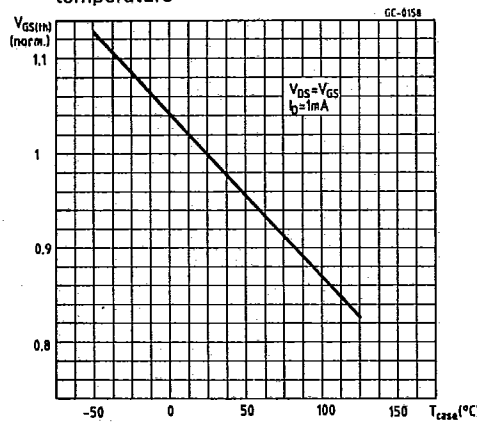
Transfer characteristics

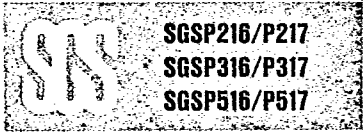


Transconductance

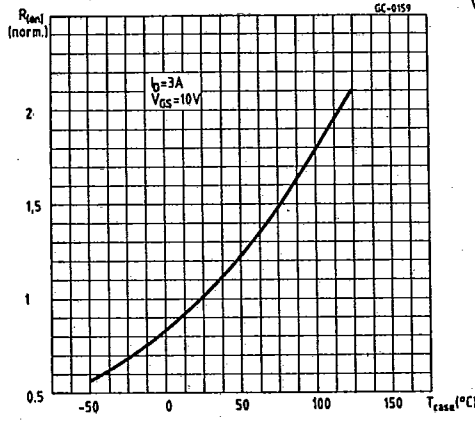


Normalized gate threshold vs. temperature

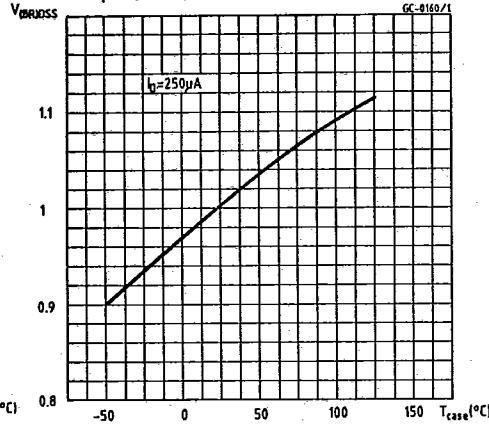




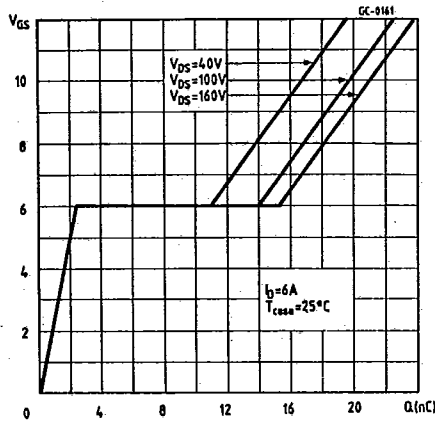
Normalized on resistance vs temperature



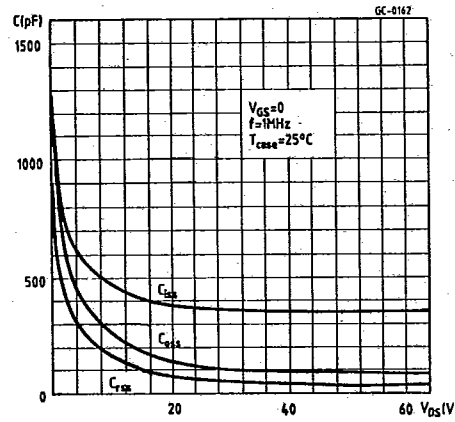
Normalized breakdown voltage vs temperature



Gate charge vs. gate to source voltage

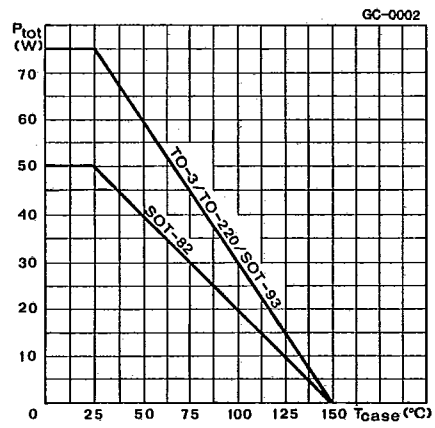


Capacitance variation



SGSP216/P217  
SGSP316/P317  
SGSP516/P517

Derating curve



Source-drain diode forward characteristics

