Data Sheet | January 2004 | FN9111.2

Flexible Double Ended Voltage and Current Mode PWM Controllers

The ISL6740, ISL6741 family of adjustable frequency, low power, pulse width modulating (PWM) voltage mode (ISL6740) and current mode (ISL6741) controllers is designed for a wide range of power conversion applications using half-bridge, full bridge, and push-pull configurations. These controllers provide an extremely flexible oscillator that allows precise control of frequency, duty cycle, and deadtime.

This advanced BiCMOS design features low operating current, adjustable switching frequency up to 1MHz, adjustable soft start, internal and external over temperature protection, fault annunciation, and a bidirectional SYNC signal that allows the oscillator to be locked to paralleled units or to an external clock for noise sensitive applications.

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. DWG. #
ISL6740IB	-40 to 105	16 Ld SOIC	M16.15
ISL6740IV	-40 to 105	16 Ld TSSOP	M16.173
ISL6741IB	-40 to 105	16 Ld SOIC	M16.15
ISL6741IV	-40 to 105	16 Ld TSSOP	M16.173

Add -T suffix to part number for tape and reel packaging

x =	CONTROL MODE
0	Voltage Mode
1	Current Mode

Features

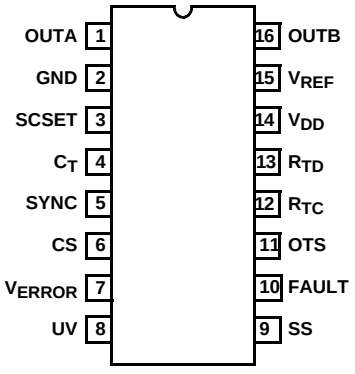
- Precision Duty Cycle and Deadtime Control
- 95μA Startup Current
- Adjustable Delayed Over Current Shutdown and Re-Start (ISL6740)
- Adjustable Short Circuit Shutdown and Re-Start
- Adjustable Oscillator Frequency Up to 2MHz
- Bidirectional Synchronization
- Inhibit Signal
- Internal Over Temperature Protection
- System Over Temperature Protection Using a Thermistor or Sensor
- Adjustable Soft Start
- Adjustable input Under Voltage Lockout
- Fault Signal
- Tight Tolerance Voltage Reference Over Line, Load, and Temperature

Applications

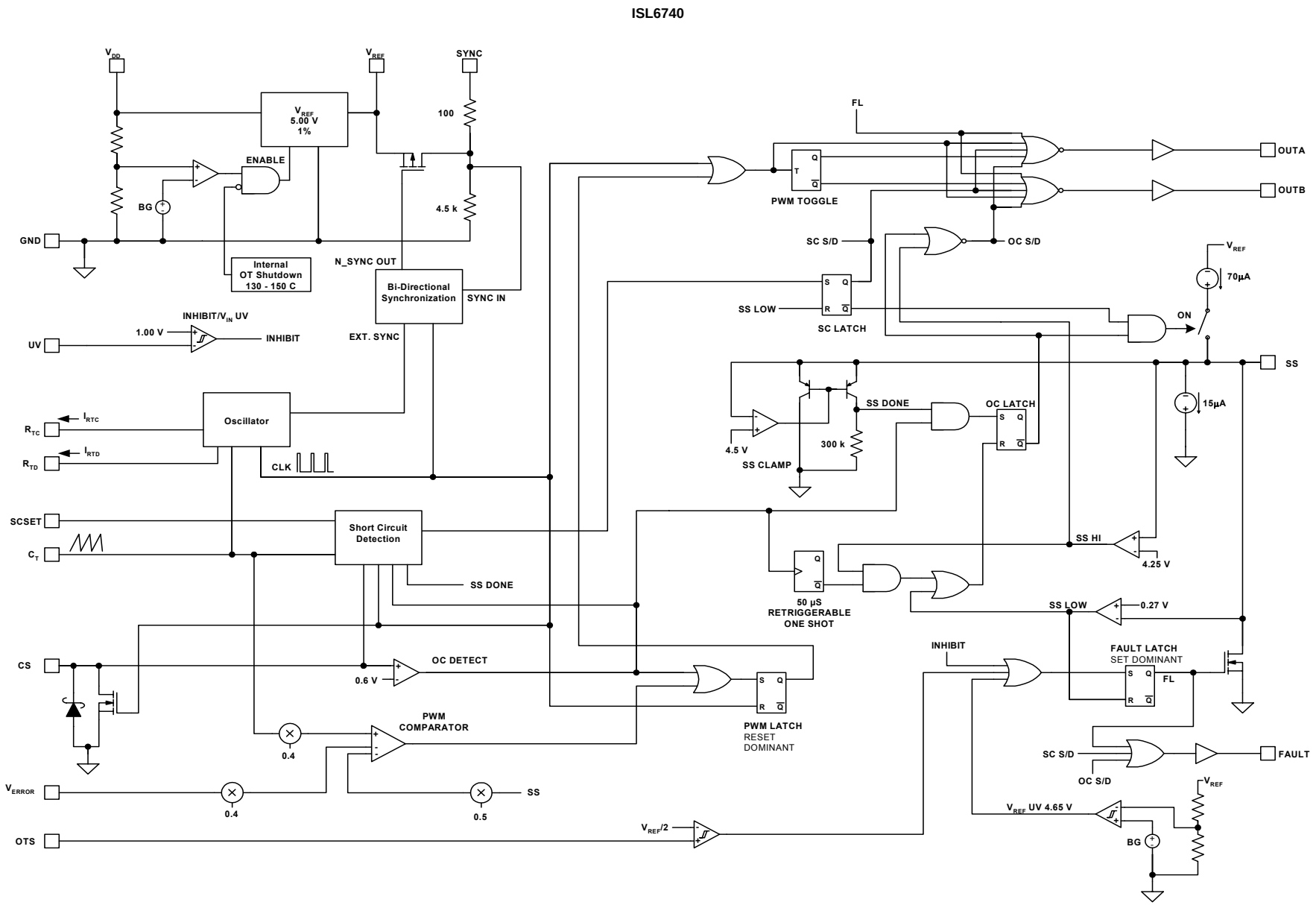
- Telecom and Datacom Power
- Wireless Base Station Power
- File Server Power
- Industrial Power Systems
- DC Transformers and Buss Regulators

Pinout

ISL6740, ISL6741 (SOIC, TSSOP)
TOP VIEW

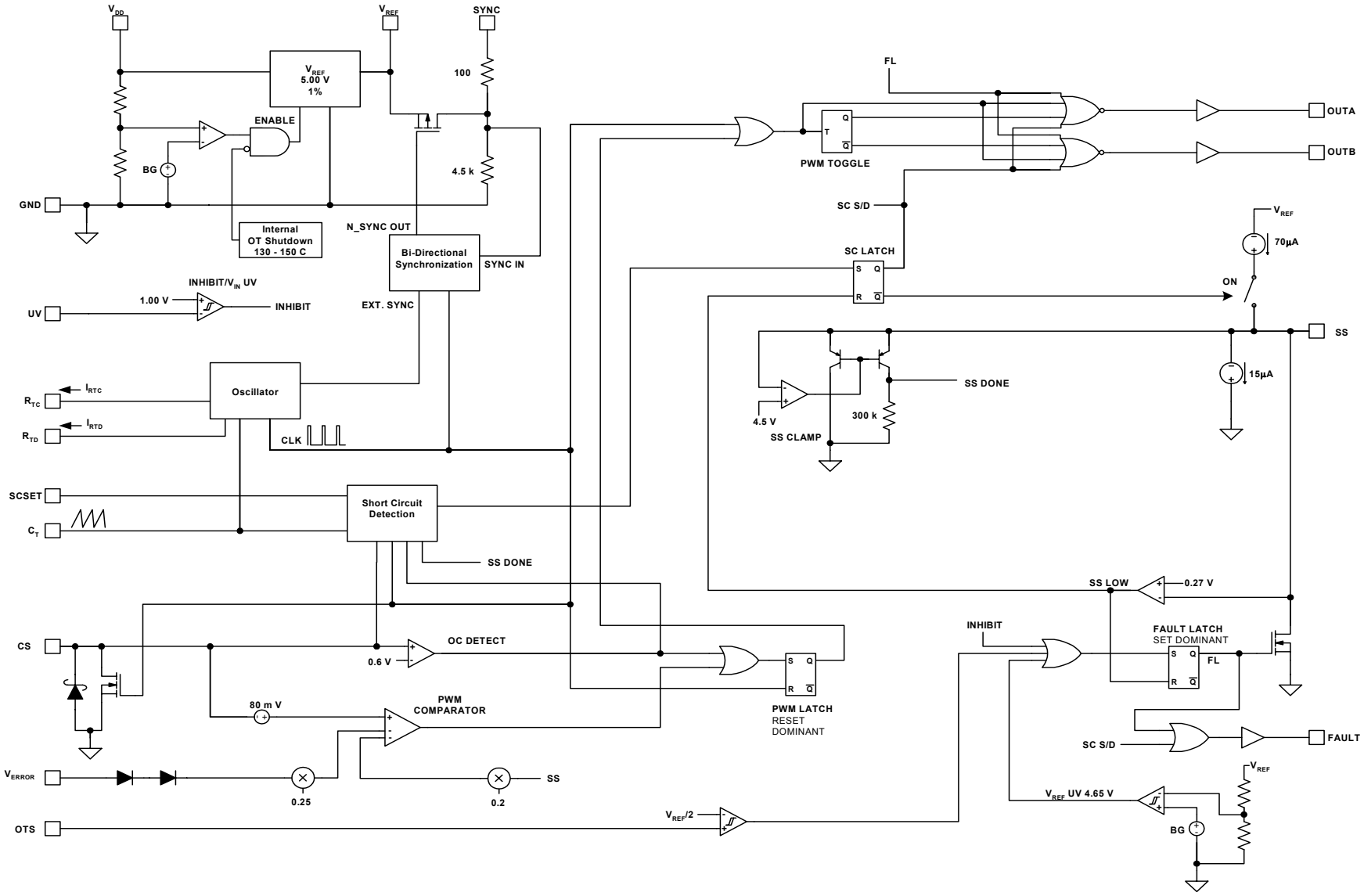


Functional Block Diagram

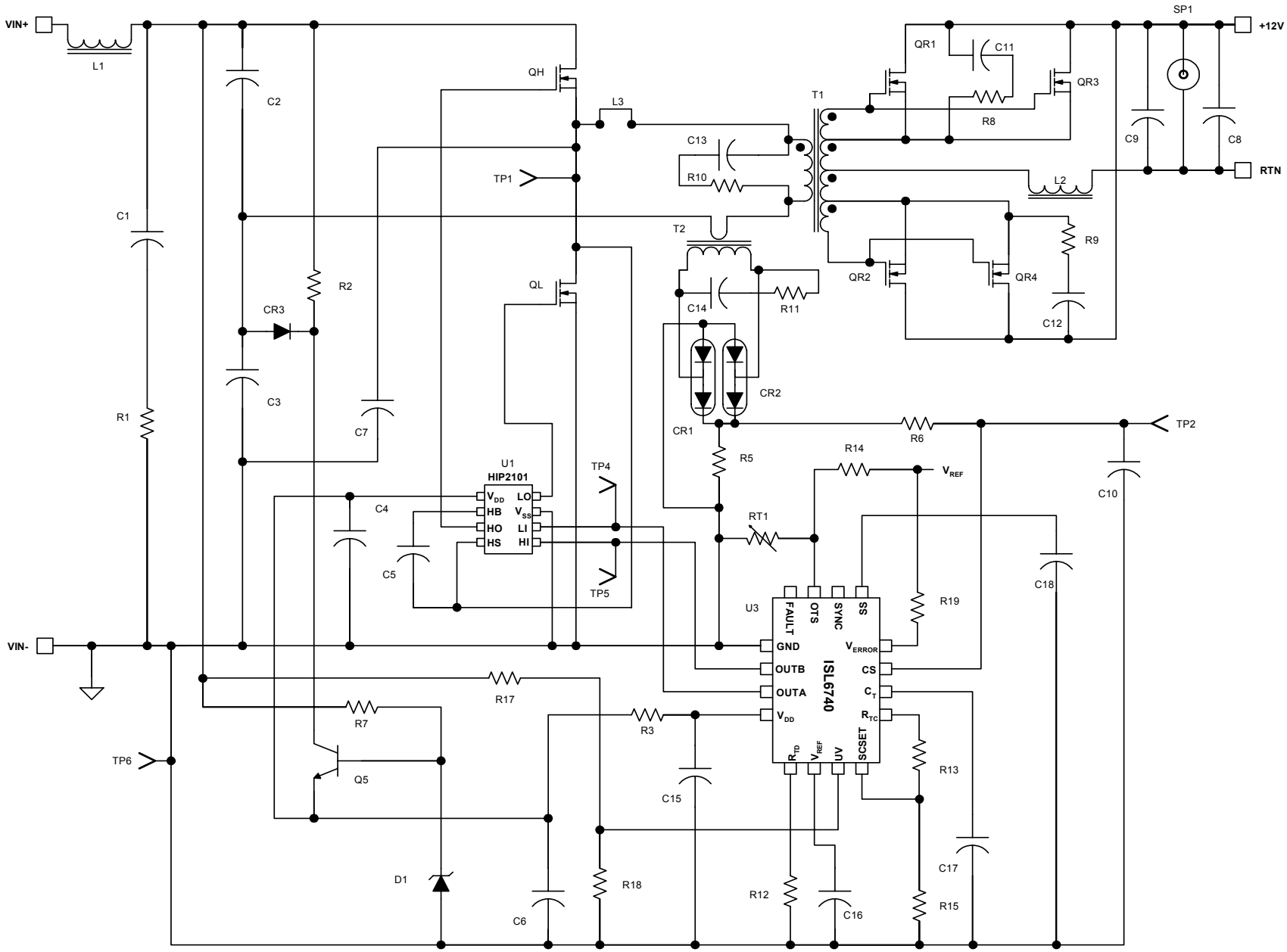


Functional Block Diagram (Continued)

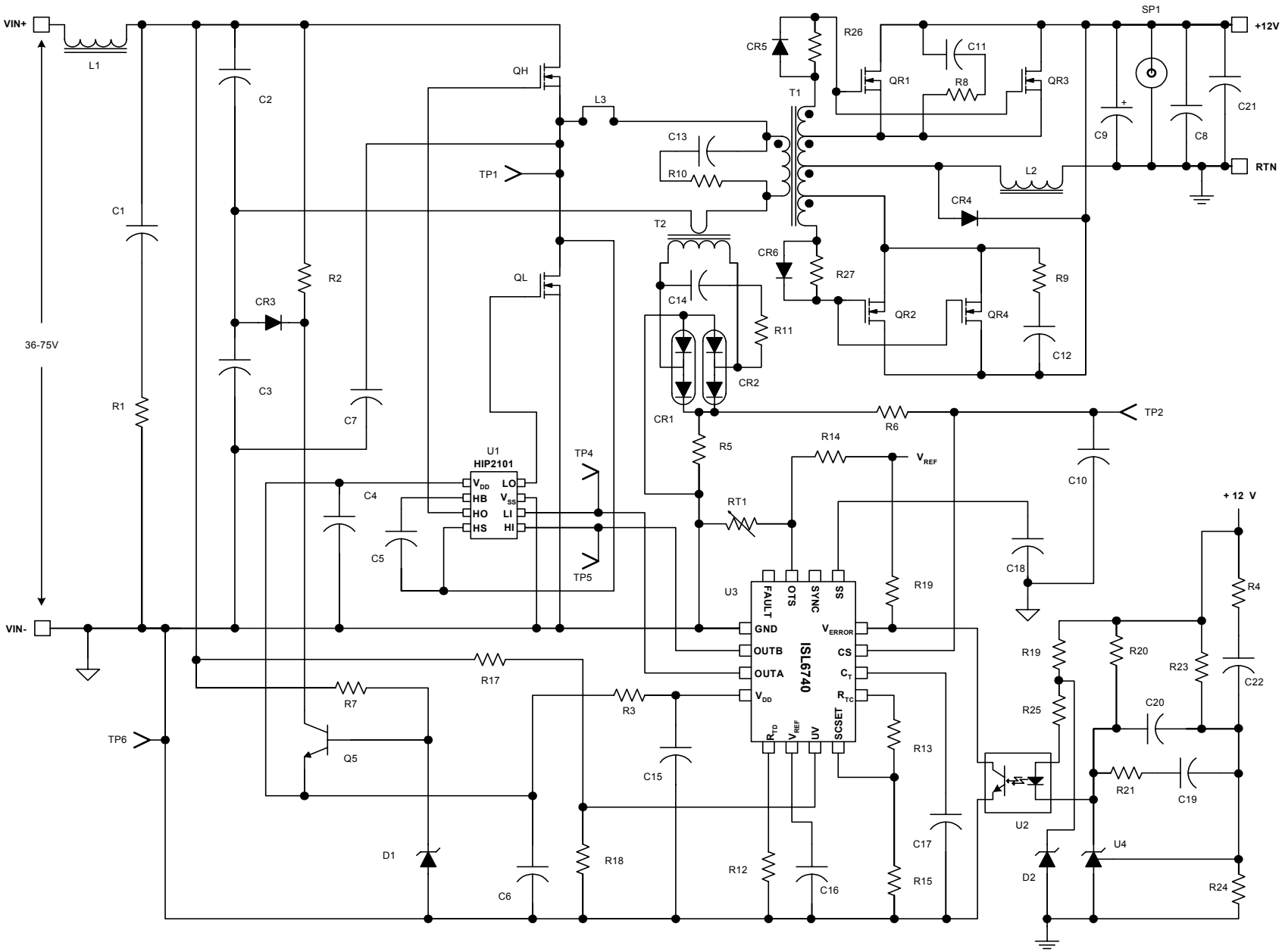
ISL6741



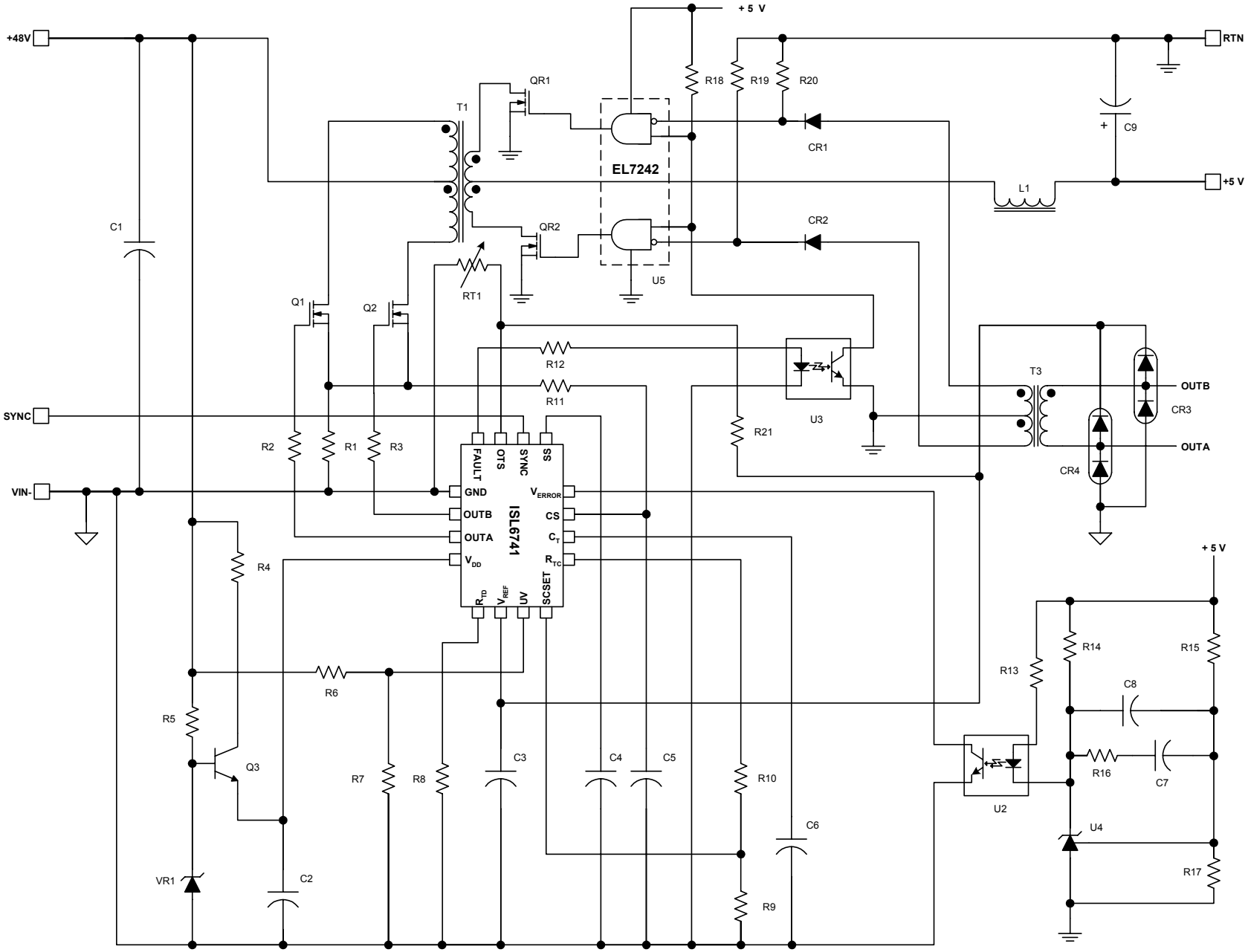
Typical Application (ISL6740) - 48V Input DC Transformer, 12V @ 8A Output (ISL6740EVAL1)



Typical Application (ISL6740) - 36 to 75 V Input, Regulated 12V @ 8A Output (ISL6740EVAL2)



Typical Application (ISL6741) - 48 to 5 Volt Push-Pull DC-DC Converter



Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . GND - 0.3V to +20.0V
OUTA, OUTB, Signal Pins . . . . . .GND - 0.3V to V_{REF}
VREF . . . . . GND - 0.3V to 6.0V
Peak GATE Current 0.5A
ESD Classification
Human Body Model (Per MIL-STD-883 Method 3015.7) . . .1500V
Charged Device Model (Per EOS/ESD DS5.3, 4/14/93) . . .1000V

Thermal Information

Thermal Resistance Junction to Ambient (Typical)	θ_{JA} (^{o}C/W)
16 Lead SOIC (Note 1)	77
16 Lead TSSOP (Note 1)	102

Maximum Junction Temperature . . . . . -55^{o}C to 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . .300^{o}C
(SOIC, TSSOP- Lead Tips Only)

Operating Conditions

Temperature Range
ISL6740Ix . . . . . -40^{o}C to 105^{o}C
ISL6741Ix . . . . . -40^{o}C to 105^{o}C
Supply Voltage Range (Typical) . . . . . 9VDC-16 VDC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. All voltages are with respect to GND.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application Schematic. 9V < V_{DD} < 20 V, R_{TD} = 51.1kΩ, R_{TC} = 10kΩ, C_T = 470pF, T_A = -40^{o}C to 105^{o}C (Note 4), Typical values are at T_A = 25^{o}C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE					
Start-Up Current, I_{DD}	V_{DD} < START Threshold	-	95	140	µA
Operating Current, I_{DD}	R_{LOAD}, $C_{OUTA,B}$ = 0	-	5.0	8.0	mA
	$C_{OUTA,B}$ = 1nF	-	7.0	12.0	mA
UVLO START Threshold		6.50	7.25	8.00	V
UVLO STOP Threshold		6.00	6.75	7.50	V
Hysteresis		0.25	0.50	0.75	V
REFERENCE VOLTAGE					
Overall Accuracy	I_{VREF} = 0, -20mA	4.900	5.000	5.050	V
Long Term Stability	T_A = 125^{o}C, 1000 hours (Note 4)	-	3	-	mV
Fault Voltage		4.10	4.55	4.75	V
VREF Good Voltage		4.25	4.75	V_{REF} -.05	V
Hysteresis		75	165	250	mV
Operational Current (source)		-20	-	-	mA
Operational Current (sink)		5	-	-	mA
Current Limit		-25	-	-100	mA
CURRENT SENSE					
Current Limit Threshold	V_{ERROR} = V_{REF}	0.55	0.6	0.65	V
CS to OUT Delay		-	35	50	ns
CS Sink Current		-	10	-	mA
Input Bias Current		-1.00	-	1.00	µA
CS to PWM Comparator Input Offset (ISL6741)	(Note 4)	-	80	-	mV
Gain (ISL6741)	A_{CS} = $\Delta V_{ERROR}/\Delta V_{CS}$ (Note 4)	-	4	-	V/V

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application Schematic. 9V < V_{DD} < 20 V, R_{TD} = 51.1kΩ, R_{TC} = 10kΩ, C_T = 470pF, T_A = -40°C to 105°C (Note 4), Typical values are at T_A = 25°C **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SCSET Input Impedance		1	-	-	MΩ
SC Setpoint Accuracy		-	10	-	%
PULSE WIDTH MODULATOR					
V_{ERROR} Input Impedance		400	-	-	kΩ
Minimum Duty Cycle	V_{ERROR} < CS Offset (ISL6741)	-	-	0	%
	V_{ERROR} < C_T Valley Voltage (ISL6740)	-	-	0	%
Maximum Duty Cycle	V_{ERROR} > 4.75V (Note 6)	-	83	-	%
V_{ERROR} to PWM Comparator Input Offset (ISL6741)	(Note 4)	0.4	1.0	1.25	V
V_{ERROR} to PWM Comparator Input Gain (ISL6741)	(Note 4)	-	0.25	-	
V_{ERROR} to PWM Comparator Input Gain (ISL6740)	(Note 4)	-	0.4	-	V/V
C_T to PWM Comparator Input Gain (ISL6740)	(Note 4)	-	0.4	-	V/V
SS to PWM Comparator Input Gain (ISL6740)	(Note 4)	-	0.5	-	V/V
SS to PWM Comparator Input Gain (ISL6741)	(Note 4)	-	0.2	-	V/V
OSCILLATOR					
Frequency Accuracy	T_A = 25°C	333	351	369	kHz
Frequency Variation with V_{DD}	T = 105°C (F_{20V} - F_{9V})/F_{9V}	-	2	3	%
	T = -40°C (F_{20V} - F_{9V})/F_{9V}	-	2	3	%
Temperature Stability	(Note 4)	-	8	-	%
Charge Current Gain		1.88	2.0	2.12	µA/µA
Discharge Current Gain		45	55	65	µA/µA
C_T Valley Voltage		0.75	0.80	0.85	V
C_T Peak Voltage		2.70	2.80	2.90	V
RTD, RTC Voltage	R_{LOAD} = 0	-	2.000	-	V
SYNCHRONIZATION					
Input High Threshold (VIH), Minimum		4.0	-	-	V
Input Low Threshold (VIL), Maximum		-	-	0.8	V
Input Impedance			4.5	-	kΩ
Input Frequency Range	(Note 4)	0.6x Free Running	-	Free Running	Hz
High Level Output Voltage (VOH)	I_{LOAD} = -1mA	-	4.5	-	V
Low Level Output Voltage (VOL)	I_{LOAD} = 10µA	-	-	100	mV
SYNC Output Current	VOH > 2.0V (Note 4)	-10	-	-	mA
SYNC Output Pulse Duration (minimum)	(Notes 4, 5)	250	-	400	ns
SYNC Advance	SYNC rising edge to GATE falling edge, C_{GATE} = C_{SYNC} = 100pF (Note 4)	-	5	-	ns
SOFTSTART					
Charging Current	SS = 2V	-45	-55	-75	µA
SS Clamp Voltage		4.35	4.5	4.65	V

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application Schematic. 9V < V_{DD} < 20 V, R_{TD} = 51.1kΩ, R_{TC} = 10kΩ, C_T = 470pF, T_A = -40°C to 105°C (Note 4), Typical values are at T_A = 25°C **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Sustained Over Current Threshold Voltage (ISL6740)	Charged Threshold minus:	0.20	0.25	0.30	V
Over Current/Short Circuit Discharge Current	SS = 2V	13	18	23	µA
Fault SS Discharge Current	SS = 2V	-	10.0	-	mA
Reset Threshold Voltage		0.25	0.27	0.33	V
FAULT					
Fault High Level Output Voltage (VOH)	I_{LOAD} = -10mA	2.85	3.5	-	V
Fault Low Level Output Voltage (VOL)	I_{LOAD} = 10mA	-	0.4	0.9	V
Fault Rise Time	C_{LOAD} = 100pF (Note 4)	-	15	-	ns
Fault Fall Time	C_{LOAD} = 100pF (Note 4)	-	15	-	ns
OUTPUT					
High Level Output Voltage (VOH)	V_{REF} - OUTA or OUTB, I_{OUT} = -50mA	-	0.5	1.0	V
Low Level Output Voltage (VOL)	OUTA or OUTB - GND, I_{OUT} = 50mA	-	0.5	1.0	V
Rise Time	C_{GATE} = 1nF, V_{DD} = 15V (Note 4)	-	50	100	ns
Fall Time	C_{GATE} = 1nF, V_{DD} = 15V (Note 4)	-	40	80	ns
THERMAL PROTECTION					
Thermal Shutdown	(Note 4)	135	145	155	°C
Thermal Shutdown Clear	(Note 4)	120	130	140	°C
Hysteresis, Internal Protection	(Note 4)	-	15	-	°C
Reference, External Protection		2.375	2.50	2.625	V
Hysteresis, External Protection		18	25	30	µA
SUPPLY UVLO/INHIBIT					
Input Voltage Low/Inhibit Threshold		0.97	1.00	1.03	V
Hysteresis, Switched Current Amplitude		7	10	15	µA
Input High Clamp Voltage		4.8	-	-	V
Input Impedance		1	-	-	MΩ

NOTES:

3. Specifications at -40°C and 105° C are guaranteed by design, not production tested.
4. Guaranteed by design, not 100% tested in production.
5. SYNC pulse width is the greater of this value or the CT discharge time.
6. This is the maximum duty cycle achievable using the specified values of R_{TC}, R_{TD}, and C_T. Larger or smaller maximum duty cycles may be obtained using other values for these components. See Equations 2-4.

Typical Performance Curves

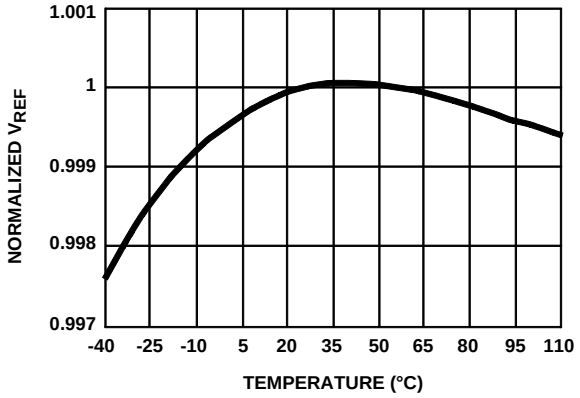


FIGURE 1. REFERENCE VOLTAGE vs TEMPERATURE

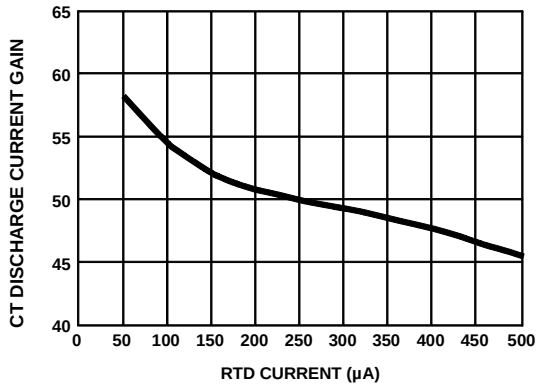


FIGURE 2. OSCILLATOR CT DISCHARGE CURRENT GAIN

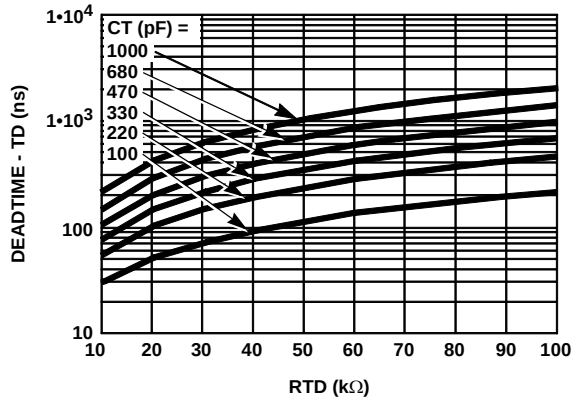


FIGURE 3. DEADTIME (TD) vs CAPACITANCE

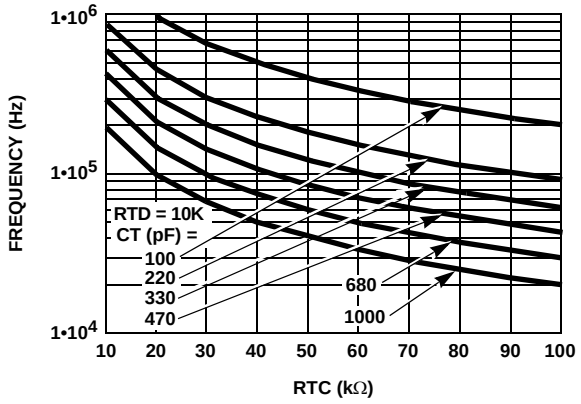


FIGURE 4. CAPACITANCE vs FREQUENCY

Pin Descriptions

V_{DD} - V_{DD} is the power connection for the IC. To optimize noise immunity, bypass V_{DD} to GND with a ceramic capacitor as close to the V_{DD} and GND pins as possible.

The total supply current, I_{DD}, will be dependent on the load applied to outputs OUTA and OUTB. Total I_{DD} current is the sum of the quiescent current and the average output current. Knowing the operating frequency, Fsw, and the output loading capacitance charge, Q, per output, the average output current can be calculated from:

$$I_{OUT} = 2 \bullet Q \bullet F_{SW} \quad A \qquad \text{(EQ. 1)}$$

SYNC - A bidirectional synchronization signal used to coordinate the switching frequency of multiple units. Synchronization may be achieved by connecting the SYNC signal of each unit together or by using an external master clock signal. The oscillator timing capacitor, C_T, is always required regardless of the synchronization method used. The paralleled unit with the highest oscillator frequency assumes control.

R_{TC} - This is the oscillator timing capacitor charge current control pin. A resistor is connected between this pin and GND. The current flowing through the resistor determines the magnitude of the charge current. The charge current is nominally twice this current. The PWM maximum ON time is determined by the timing capacitor charge duration.

R_{TD} - This is the oscillator timing capacitor discharge current control pin. A resistor is connected between this pin and GND. The current flowing through the resistor determines the magnitude of the discharge current. The discharge current is nominally 50x this current. The PWM deadtime is determined by the timing capacitor discharge duration.

C_T - The oscillator timing capacitor is connected between this pin and GND.

V_{ERROR} - The inverting input of the PWM comparator. The error voltage is applied to this pin to control the duty cycle. Increasing the signal level increases the duty cycle. The node may be driven with an external error amplifier or opto-coupler.

The ISL6740, ISL6741 features a built-in soft start. Soft start is implemented as a clamp on the error voltage input.

OTS - The non-inverting input to the over temperature shutdown comparator. The signal input at this pin is compared to an internal threshold of $V_{REF}/2$. If the voltage at this pin exceeds the threshold, the Fault signal is asserted and the outputs are disabled until the condition clears. There is a nominal 25µA switched current source used for hysteresis. The amount of hysteresis is adjustable by varying the source impedance of the signal into this pin.

OTS may be used to monitor parameters other than temperature, such as voltage. Any signal for which a high out-of-bounds monitor is desired may utilize the OTS comparator.

FAULT - The Fault signal is asserted high whenever the outputs, OUTA and OUTB, are disabled. This occurs during an over temperature fault, an input UV fault, a V_{REF} UV fault, or during an over current (ISL6740) or short circuit shutdown fault. Fault can be used to disable synchronous rectifiers whenever the outputs are disabled.

Fault is a three-state output and is high impedance during the soft start cycle. Adding a pull-up resistor to VREF or a pull-down resistor to ground determines the state of Fault during soft start. This feature allows the designer to use the Fault signal to enable or disable output synchronous rectifiers during soft start.

UV - Undervoltage monitor input pin. A resistor divider between the input source voltage and GND sets the under voltage lock out threshold. The signal is compared to an internal 1.00V reference to detect an under voltage or inhibit condition.

CS - This is the input to the current sense comparator(s). The IC has the PWM comparator for peak current mode control (ISL6741) and an over current protection comparator. The over current comparator threshold is set at 0.600V nominal.

The CS pin is shorted to GND at the end of each switching cycle. Depending on the current sensing source impedance, a series input resistor may be required due to the delay between the internal clock and the external power switch. This delay may allow an overlap such that the CS signal may be discharged while the current signal is still active. If the current sense source is low impedance it will cause increased power dissipation.

ISL6740 - Exceeding the over-current threshold will start a delayed shutdown sequence. Once an over current condition is detected, the soft start charge current source is disabled. The soft start capacitor begins discharging through a 25µA current source, and if it discharges to less than 4.25V (Sustained Over Current Threshold), a shutdown condition occurs and the OUTA and OUTB outputs are forced low. When the soft start voltage reaches 0.27V (Reset Threshold) a soft start cycle begins.

An over current condition must be absent for 50µs before the delayed shutdown control resets. If the over current condition ceases, and an additional 50µs period elapses before the shutdown threshold is reached, no shutdown occurs. The SS charging current is re-enabled and the soft start voltage is allowed to recover.

ISL6741 - The ISL6741 current mode controller does not shutdown due to an overcurrent condition. The pulse-by-pulse current limit characteristic of peak current mode control limits the output current to acceptable levels.

GND - Reference and power ground for all functions on this device. Due to high peak currents and high frequency operation, a low impedance layout is necessary. Ground planes and short traces are highly recommended.

OUTA and OUTB - Alternate half cycle output stages. Each output is capable of 0.5A peak currents for driving logic level power MOSFETs or MOSFET drivers. Each output provides very low impedance to overshoot and undershoot.

VREF - The 5.00V reference voltage output. +1/-2% tolerance over line, load and operating temperature. Bypass to GND with a 0.047µF to 2.2µF ceramic capacitor. Capacitors outside of this range may cause oscillation.

SS - Connect the soft start timing capacitor between this pin and GND to control the duration of soft start. The value of the capacitor determines the rate of increase of the duty cycle during start up, controls the over current shutdown delay (ISL6740), and the over current and short circuit hiccup restart period.

SCSET - Sets the duty cycle threshold that corresponds to a short circuit condition. A resistive divider between R_{TC} and GND or R_{TD} and GND, or a voltage between 0 and 2V may be used to adjust the SCSET threshold. If using a resistor divider from either RTC or RTD, the impedance to GND affects the oscillator timing and should be considered when determining the oscillator timing components. Connecting SCSET to GND disables short circuit shutdown and hiccup.

Functional Description

Features

The ISL6740, ISL6741 PWMs are an excellent choice for low cost bridge and push-pull topologies for applications requiring accurate duty cycle and deadtime control. With its many protection and control features, a highly flexible design with minimal external components is possible. Among its many features are current mode control (ISL6741), adjustable soft start, over current protection, thermal protection, bidirectional synchronization, fault indication, and adjustable frequency.

Oscillator

The ISL6740, ISL6741 have an oscillator with a programmable frequency range to 2MHz, which can be programmed with two resistors and capacitor. The use of three timing elements, R_{TC}, R_{TD}, and C_T allow great flexibility and precision when setting the oscillator frequency.

The switching period may be considered the sum of the timing capacitor charge and discharge durations. The charge duration is determined by R_{TC} and C_T. The discharge duration is determined by R_{TD} and C_T.

$$T_C \approx 0.5 \bullet R_{TC} \bullet C_T \quad S \qquad \text{(EQ. 2)}$$

$$T_D \approx 0.02 \bullet R_{TD} \bullet C_T \quad S \qquad \text{(EQ. 3)}$$

$$T_{SW} = T_C + T_D = \frac{1}{F_{SW}} \quad S \qquad \text{(EQ. 4)}$$

where T_C and T_D are the charge and discharge times, respectively, T_{SW} is the oscillator free running period, and f is the oscillator frequency. One output switching cycle requires two oscillator cycles. The actual times will be slightly longer than calculated due to internal propagation delays of approximately 10ns/transition. This delay ads directly to the switching duration, but also causes overshoot of the timing capacitor peak and valley voltage thresholds, effectively increasing the peak-to-peak voltage on the timing capacitor. Additionally, if very low charge and discharge currents are used, there will be increased error due to the input impedance at the C_T pin.

The maximum duty cycle, D, and percent deadtime, DT, can be calculated from:

$$D = \frac{T_C}{T_{SW}} \qquad \text{(EQ. 5)}$$

$$DT = 1 - D \qquad \text{(EQ. 6)}$$

Implementing Synchronization

The oscillator can be synchronized to an external clock applied to the SYNC pin or by connecting the SYNC pins of multiple ICs together. If an external master clock signal is used, the free running frequency of the oscillator should be ~10% slower than the desired synchronous frequency. The external master clock signal should have a pulse width greater than 20ns. The SYNC circuitry will not respond to an external signal during the first 60% of the oscillator switching cycle.

The SYNC input is edge triggered and its duration does not affect oscillator operation. However, the deadtime is affected by the SYNC frequency. A higher frequency signal applied to the SYNC input will shorten the deadtime. The shortened deadtime is the result of the timing capacitor charge cycle being prematurely terminated by the external SYNC pulse. Consequently, the timing capacitor is not fully charged when the discharge cycle begins. This effect is only a concern when an external master clock is used, or if units with different operating frequencies are paralleled.

Soft Start Operation

The ISL6740, ISL6741 feature a soft start using an external capacitor in conjunction with an internal current source. Soft start reduces stresses and surge currents during start up.

Upon start up, the soft start circuitry clamps the error voltage input (V_{ERROR} pin) indirectly to a value equal to the soft start voltage. The soft start clamp does not actually clamp the error voltage input as is done in many implementations. Rather the PWM comparator has two inverting inputs such that the lower voltage is in control.

The output pulse width increases as the soft start capacitor voltage increases. This has the effect of increasing the duty cycle from zero to the regulation pulse width during the soft start period. When the soft start voltage exceeds the error voltage, soft start is completed. Soft start occurs during start-up, after recovery from a Fault condition or over current/short circuit shutdown. The soft start voltage is clamped to 4.5V.

The Fault signal output is high impedance during the soft start cycle. A pull-up resistor to VREF or a pull-down resistor to ground should be added to achieve the desired state of Fault during soft start.

Gate Drive

The ISL6740, ISL6741 are capable of sourcing and sinking 0.5A peak current, but are primarily intended to be used in conjunction with a MOSFET driver due to the 5V drive level. To limit the peak current through the IC, an external resistor may be placed between the totem-pole output of the IC (OUTA or OUTB pin) and the gate of the MOSFET. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance.

Under Voltage Monitor and Inhibit

The UV input is used for input source under voltage lockout and inhibit functions. If the node voltage falls below 1.00V a UV shutdown fault occurs. This may be caused by low source voltage or by intentional grounding of the pin to disable the outputs. There is a nominal 10μA switched current source used to create hysteresis. The current source is active only during an UV/Inhibit fault; otherwise, it is inactive and does not affect the node voltage. The magnitude of the hysteresis is a function of the external resistor divider impedance. If the resistor divider impedance results in too little hysteresis, a series resistor between the UV pin and the divider may be used to increase the hysteresis. A soft start cycle begins when the UV/Inhibit fault clears.

The voltage hysteresis created by the switched current source and the external impedance is generally small due to the large resistor divider ratio required to scale the input voltage down to the UV threshold level. A small capacitor placed between the UV input and ground may be required to filter noise out.

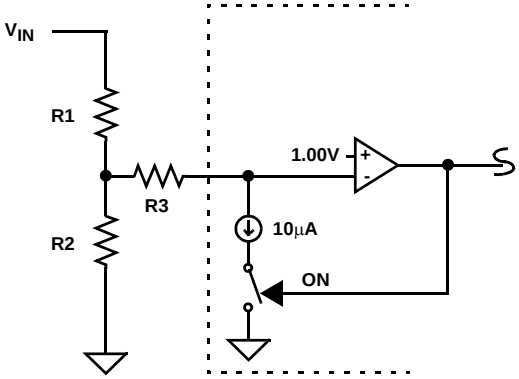


FIGURE 5. UV HYSTERESIS

As V_{IN} decreases to a UV condition, the threshold level is:

$$V_{IN(DOWN)} = \frac{R1 + R2}{R2} \quad V \qquad \text{(EQ. 7)}$$

The hysteresis voltage, ΔV, is:

$$\Delta V = 10^{-5} \bullet \langle R1 + R3 \bullet \left(\frac{R1 + R2}{R2}\right) \rangle \quad V \qquad \text{(EQ. 8)}$$

Setting R3 equal to zero results in the minimum hysteresis, and yields:

$$\Delta V = 10^{-5} \bullet R1 \quad V \qquad \text{(EQ. 9)}$$

As V_{IN} increases from a UV condition, the threshold level is:

$$V_{IN(UP)} = V_{IN(DOWN)} + \Delta V \quad V \qquad \text{(EQ. 10)}$$

Over Current Operation

ISL6740 - Over current delayed shutdown is enabled once the soft start cycle is complete. If an over current condition is detected, the soft start charging current source is disabled and the soft start capacitor is allowed to discharge through a 15µA source. At the same time a 50µs re-triggerable one-shot timer is activated. It remains active for 50µs after the over current condition ceases. If the soft start capacitor discharges by more then 0.25V to 4.25V, the output is disabled and the Fault signal asserted. This state continues until the soft start voltage reaches 270mV, at which time a new soft start cycle is initiated. If the over current condition stops at least 50µs prior to the soft start voltage reaching 4.25V, the soft start charging currents revert to normal operation and the soft start voltage is allowed to recover.

The duration of the OC shutdown period can be increased by adding a resistor between VREF and SS. The value of the resistor must be large enough so that the minimum specified SS discharge current is not exceeded. Using a 422kΩ resistor, for example, will result in a small current being injected into SS, effectively reducing the discharge current. This will increase the OFF time by about 60%, nominally. The external pull-up resistor will also decrease the SS duration, so its effect should be considered when selecting the value of the SS capacitor.

Latching OC shutdown is also possible by using a lower valued resistor between VREF and SS. If the SS node is not allowed to discharge below the SS reset threshold, the IC will not recover from an over-current fault. The value of the resistor must be low enough so that the maximum specified discharge current is not sufficient to pull SS below 0.33V. A 200kΩ resistor, for example, prevents SS from discharging below ~0.4V. Again, the external pull-up resistor will decrease the SS duration, so its effect should be considered when selecting the value of the SS capacitor.

ISL6741 - Over current results in pulse-by-pulse duty cycle reduction as occurs in any peak current mode controller. This results in a well controlled decrease in output voltage with increasing current beyond the over current threshold. An over current condition in the ISL6741 will not cause a shutdown.

Short Circuit Operation

A short circuit condition is defined as the simultaneous occurrence of current limit and a reduced duty cycle. The degree of reduced duty cycle is user adjustable using the SCSET input. A resistor divider between either R_{TD} or R_{TC} and GND to RCSET sets a threshold that is compared to the voltage on the timing capacitor, C_T. The resistor divider percentage corresponds to the fraction of the maximum duty cycle below which a short circuit may exist. If the timing capacitor voltage fails to exceed the threshold before an over current pulse is detected, a short circuit condition exists. A shutdown and soft start cycle will begin if 8 short circuit events occur within 32 oscillator cycles. Connecting SCSET to GND disables this feature.

Since the current sourced from both R_{TC} and R_{TD} determine the charge and discharge currents for the timing capacitor, the effect of the SCSET divider must be included in the timing calculations. Typically the resistor between R_{TC} and GND is formed by two series resistors with the center node connected to SCSET.

Alternatively, SCSET may be set using a voltage between 0V and 2V. This voltage divided by 2 determines the percentage of the maximum duty cycle that corresponds to a short circuit when current limit is active. For example, if the maximum duty cycle is 95% and 1V is applied to SCSET, then the short circuit duty cycle is 50% of 95% or 47.5%.

Fault Conditions

A fault condition occurs if V_{REF} falls below 4.65V, the UV input falls below 1.00V, the thermal protection is triggered, or if OTS faults. When a fault is detected, OUTA and OUTB outputs are disabled, the Fault signal is asserted, and the soft start capacitor is quickly discharged. When the fault condition clears and the soft start voltage is below the reset threshold, a soft start cycle begins. The Fault signal is high impedance during the soft start cycle.

An over current condition that results in shutdown (ISL6740), or a short circuit shutdown also cause assertion of the Fault signal. The difference between a current fault and the faults described earlier is that the soft start capacitor is not quickly discharged. The initiation of a new soft start cycle is delayed while the soft start capacitor is discharged at a 15μA rate. This keeps the average output current to a minimum.

Thermal Protection

Two methods of over temperature protection are provided. The first method is an on board temperature sensor that protects the device should the junction temperature exceed 145°C. There is approximately 15°C of hysteresis.

The second method uses an internal comparator with a 2.5V reference (V_{REF}/2). The non-inverting input to the comparator is accessible through the OTS pin. A thermistor or thermal sensor located at or near the area of interest may be connected to this input. There is a nominal 25μA switched current source used to create hysteresis. The current source is active only during an OT fault; otherwise, it is inactive and does not affect the node voltage. The magnitude of the hysteresis is a function of the external resistor divider impedance. Either a positive temperature coefficient (PTC) or a negative temperature coefficient (NTC) thermistor may be used. If a NTC is desired, position R1 may be substituted.

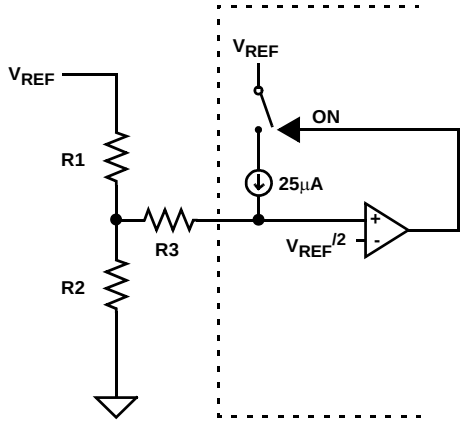


FIGURE 6. OTS HYSTERESIS

If a PTC is desired, then position R2 may be substituted. The threshold with increasing temperature is set by making the fixed resistance equal in value to the thermistor resistance at the desired trip temperature.

$V_{TH}\uparrow$ = 2.5V and R1 = R2 (HOT)

To determine the value of the hysteresis resistor, R3, select the value of thermistor resistance that corresponds to the desired reset temperature.

$$R3 = \frac{10^5 \bullet (R1 - R2) - R1 \bullet R2}{R1 + R2} \quad \Omega \qquad \text{(EQ. 11)}$$

If the hysteresis resistor, R3, is not desired, the value of the thermistor resistance at the reset temperature can be determined from:

$$R1 = \frac{2.5 \bullet R2}{2.5 - 10^{-5} \bullet R2} \quad \Omega \quad (NTC) \qquad \text{(EQ. 12)}$$

$$R2 = \frac{2.5 \bullet R1}{2.5 + 10^{-5} \bullet R1} \quad \Omega \quad (PTC) \qquad \text{(EQ. 13)}$$

The OTS comparator may also be used to monitor signals other than suggested above. It may also be used to monitor any voltage signal for which an excess requires a response as described above. Input or output voltage monitoring are examples of this.

Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. V_{DD} should be bypassed directly to GND with good high frequency capacitance.

Typical Application

The Typical Application Schematic features the ISL6740 in an unregulated half-bridge DC-DC converter configuration, often referred to as a DC Transformer or Bus Regulator. The ISL6740EVAL1 demonstration unit implements this design and is available for evaluation.

The input voltage range is 48 ±10%V DC. The output is a nominal 12V when the input voltage is at 48V. Since this is an unregulated topology, the output voltage will vary proportionately with input voltage. The load regulation is a function of resistance between the source and the converter output. The output is rated at 8A.

Circuit Element Descriptions

The converter design may be broken down into the following functional blocks:

Input Filtering: L1, C1, R1

Half-Bridge Capacitors: C2, C3

Isolation Transformer: T1

Primary Snubber: C13, R10

Start Bias Regulator: CR3, R2, R7, C6, Q5, D1

Supply Bypass Components: R3, C15, C4, C5

Main MOSFET Power Switch: QH, QL

Current Sense Network: T2, CR1, CR2, R5, R6, R11, C10, C14

Control Circuit: U3, RT1, R14, R19, R13, R15, R17, R18, C16, C18, C17

Output Rectification and Filtering: QR1, QR2, QR3, QR4, L2, C9, C8

Secondary Snubber: R8, R9, C11, C12

FET Driver: U1

ZVS Resonant Delay (Optional): L3, C7

Design Criteria

The following design requirements were selected:

Switching Frequency, Fsw: 235kHz

V_{IN}: 48 ±10%V

V_{OUT}: 12V (nominal) @ I_{OUT} = 8A

P_{OUT}: 100W

Efficiency: 95%

Ripple: 1%

Transformer Design

The design of a transformer for a half-bridge application is a straight forward affair, although iterative. It is a process of many compromises, and even experienced designers will produce different designs when presented with identical requirements. The iterative design process is not presented here for clarity.

The abbreviated design process follows:

- Select a core geometry suitable for the application. Constraints of height, footprint, mounting preference, and operating environment will affect the choice.
- Determine the turns ratio.
- Select suitable core material(s).
- Select maximum flux density desired for operation.
- Select core size. Core size will be dictated by the capability of the core structure to store the required energy, the number of turns that have to be wound, and the wire gauge needed. Often the window area (the space used for the windings) and power loss determine the final core size.
- Determine maximum desired flux density. Depending on the frequency of operation, the core material selected, and the operating environment, the allowed flux density must be determined. The decision of what flux density to allow is often difficult to determine initially. Usually the highest flux density that produces an acceptable design is used, but often the winding geometry dictates a larger core than is indicated based on flux density alone.
- Determine the number of primary turns.
- Select the wire gauge for each winding.
- Determine winding order and insulation requirements.
- Verify the design.

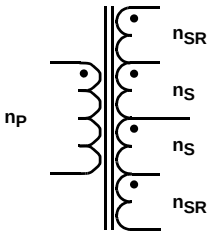


FIGURE 7. TRANSFORMER SCHEMATIC

For this application we have selected a planar structure to achieve a low profile design. A PQ style core was selected because of its round center leg cross section, but there are many suitable core styles available.

Since the converter is operating open loop at nearly 100% duty cycle, the turns ratio, N, is simply the ratio of the input voltage to the output voltage divided by 2.

$$N = \frac{V_{IN}}{V_{OUT} \bullet 2} = \frac{48}{12 \bullet 2} = 2 \qquad \text{(EQ. 14)}$$

The factor of 2 divisor is due to the half-bridge topology. Only half of the input voltage is applied to the primary of the transformer.

A PC44HPQ20/6 “E-Core” plus a PC44PQ20/3 “I-Core” from TDK were selected for the transformer core. The ferrite material is PC44.

The core parameter of concern for flux density is the effective core cross sectional area, Ae. For the PQ core pieces selected:

Ae = 0.62cm^2 or 6.2e -5m^2

Using Faraday’s Law, V = N dΦ/dt, the number of primary turns can be determined once the maximum flux density is set. An acceptable Bmax is ultimately determined by the

allowable power dissipation in the ferrite material and is influenced by the lossiness of the core, core geometry, operating ambient temperature, and air flow. The TDK datasheet for PC44 material indicates a core loss factor of ~400 mW/cm^3 with a ± 2000 gauss 100kHz sinusoidal excitation. The application uses a 235kHz square wave excitation, so no direct comparison between the application and the data can be made. Interpolation of the data is required. The core volume is approximately 1.6cm^3, so the estimated core loss is

$$P_{loss} \approx \frac{mW}{cm^3} \bullet cm^3 \bullet \frac{f_{act}}{f_{meas}} = 0.4 \bullet 1.6 \bullet \frac{200kHz}{100kHz} = 1.28 \quad W \qquad \text{(EQ. 15)}$$

1.28W of dissipation is significant for a core of this size. Reducing the flux density to 1200 gauss will reduce the dissipation by about the same percentage, or 40%. Ultimately, evaluation of the transformer's performance in the application will determine what is acceptable.

From Faraday's Law and using 1200 gauss peak flux density (ΔB = 2400 gauss or 0.24 tesla)

$$N = \frac{V_{IN} \bullet T_{ON}}{2 \bullet A_e \bullet \Delta B} = \frac{53 \bullet 2 \bullet 10^{-6}}{2 \bullet 6.2 \bullet 10^{-5} \bullet 0.24} = 3.56 \quad \text{turns} \qquad \text{(EQ. 16)}$$

Rounding up yields 4 turns for the primary winding. The peak flux density using 4 turns is ~1100 gauss. From EQ. 1, the number of secondary turns is 2.

The volts/turn for this design ranges from 5.4V at V_{IN} = 43V to 6.6V at V_{IN} = 53V. Therefore, the synchronous rectifier (SR) windings may be set at 1 turn each with proper FET selection. Selecting 2 turns for the synchronous rectifier windings would also be acceptable, but the gate drive losses would increase.

The next step is to determine the equivalent wire gauge for the planar structure. Since each secondary winding conducts for only 50% of the period, the RMS current is

$$I_{RMS} = I_{OUT} \bullet \sqrt{D} = 10 \bullet \sqrt{0.5} = 7.07 \quad A \qquad \text{(EQ. 17)}$$

where D is the duty cycle. Since an FR-4 PWB planar winding structure was selected, the width of the copper traces is limited by the window area width, and the number of layers is limited by the window area height. The PQ core selected has a usable window area width of 0.165 inches. Allowing one turn per layer and 0.020 inches clearance at the edges allows a maximum trace width of 0.125 inches. Using 100 circular mils(c.m.)/A as a guideline for current density, and from EQ. 17, 707c.m. are required for each of the secondary windings (a circular mil is the area of a circle 0.001 inches in diameter). Converting c.m. to square mils yields 555mils^2 (0.785 sq. mils/c.m.). Dividing by the trace width results in a copper thickness of 4.44mils (0.112mm). Using 1.3mils/oz. of copper requires a copper weight of 3.4oz. For reasons of cost, 3oz. copper was selected.

One layer of each secondary winding also contains the synchronous rectifier winding. For this layer the secondary trace width is reduced by 0.025 inches to 0.100 inches(0.015 inches for the SR winding trace width and 0.010 inches spacing between the SR winding and the secondary winding).

The choice of copper weight may be validated by calculating the DC copper losses of the secondary winding as follows. Ignoring the terminal and lead-in resistance, the resistance of each layer of the secondary may be approximated using EQ. 18.

$$R = \frac{2\pi\rho}{t \bullet \ln\left(\frac{r_2}{r_1}\right)} \quad \Omega \qquad \text{(EQ. 18)}$$

where

R = Winding resistance

ρ = Resistivity of copper = 669e-9Ω-inches at 20°C

t = Thickness of the copper (3 oz.) = 3.9e-3 inches

r_2 = Outside radius of the copper trace = 0.324 or 0.299 inches

r_1 = Inside radius of the copper trace = 0.199 inches

The winding without the SR winding on the same layer has a DC resistance 2.21mΩ. The winding that shares the layer with the SR winding has a DC resistance of 2.65mΩ. With the secondary configured as a 4 turn center tapped winding (2 turns each side of the tap), the total DC power loss for the secondary at 20°C is 486mW.

The primary windings have an RMS current of approximately 5 A (I_{OUT} x N_S/N_P at ~ 100% duty cycle). The primary is configured as 2 layers, 2 turns per layer to minimize the winding stack height. Allowing 0.020 inches edge clearance and 0.010 inches between turns yields a trace width of 0.0575 inches. Ignoring the terminal and lead-in resistance, and using EQ. 18, the inner trace has a resistance of 4.25mΩ, and the outer trace has a resistance of 5.52mΩ. The resistance of the primary then is 19.5mΩ at 20°C. The total DC power loss for the secondary at 20°C is 489mW.

Improved efficiency and thermal performance could be achieved by selecting heavier copper weight for the windings. Evaluation in the application will determine its need.

The order and geometry of the windings affects the AC resistance, winding capacitance, and leakage inductance of the finished transformer. To mitigate these effects, interleaving the windings is necessary. The primary winding is sandwiched between the two secondary windings. The winding layout appears below.

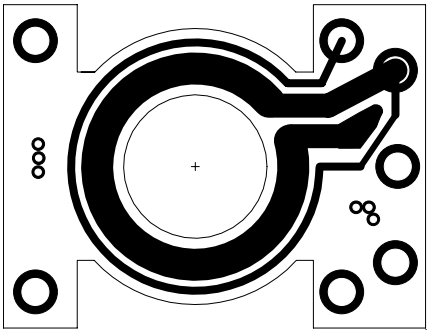


FIGURE 7A. TOP LAYER: 1 TURN SECONDARY AND SR WINDINGS

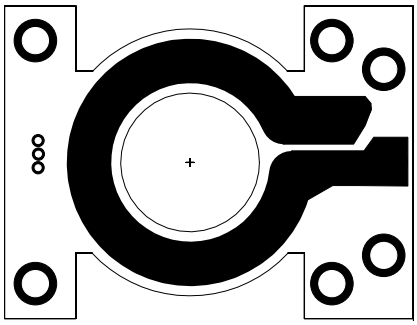


FIGURE 7B. INT. LAYER 1: 1 TURN SECONDARY WINDING

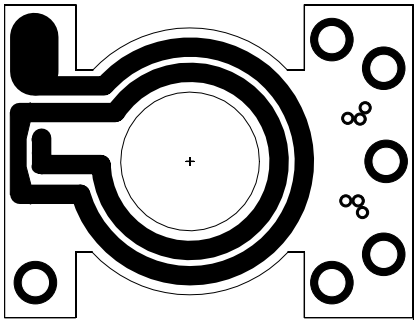


FIGURE 7C. INT. LAYER 2: 2 TURNS PRIMARY WINDING

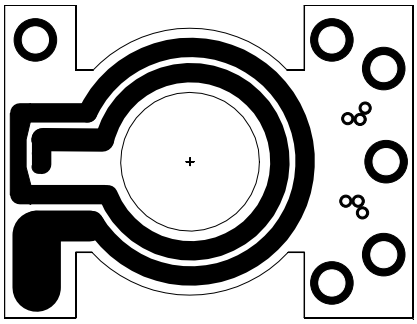


FIGURE 7D. INT. LAYER 3: 2 TURNS PRIMARY WINDING

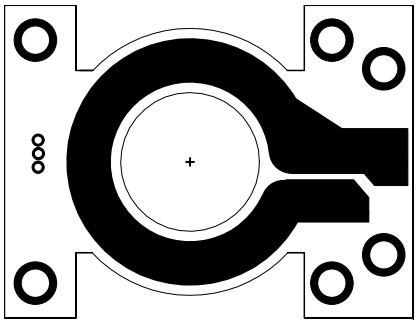


FIGURE 7E. INT. LAYER 4: 1 TURN SECONDARY WINDING

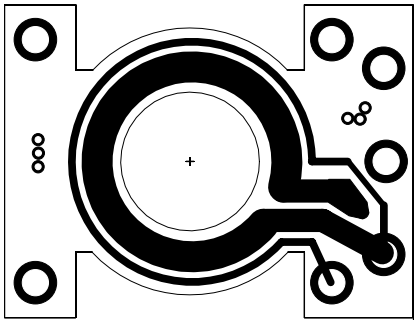


FIGURE 7F. BOTTOM LAYER: 1 TURN SECONDARY AND SR WINDINGS

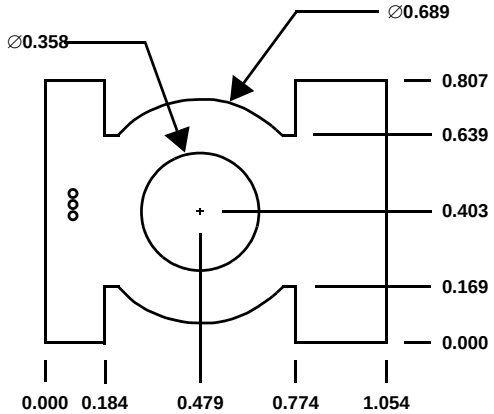


FIGURE 7G. PWB DIMENSIONS

MOSFET Selection

The criteria for selection of the primary side half-bridge FETs and the secondary side synchronous rectifier FETs is largely based on the current and voltage rating of the device. However, the FET drain-source capacitance and gate charge cannot be ignored.

The zero voltage switch (ZVS) transition timing is dependent on the transformer's leakage inductance and the capacitance at the node between the upper FET source and the lower FET drain. The node capacitance is comprised of the drain-source capacitance of the FETs and the transformer parasitic capacitance. The leakage inductance and capacitance form an LC resonant tank circuit which determines the duration of the transition. The amount of energy stored in the LC tank circuit determines the transition voltage amplitude. If the leakage inductance energy is too low, ZVS operation is not possible and near or partial ZVS operation occurs. As the leakage energy increases, the voltage amplitude increases until it is clamped by the FET body diode to ground or V_{IN}, depending on which FET conducts. When the leakage energy exceeds the minimum required for ZVS operation, the voltage is clamped until the energy is transferred. This behavior increases the time window for ZVS operation. This behavior is not without consequences, however. The transition time and the period of time during which the voltage is clamped reduces the effective duty cycle.

The gate charge affects the switching speed of the FETs. Higher gate charge translates into higher drive requirements and/or slower switching speeds. The energy required to drive the gates is dissipated as heat.

The maximum input voltage, V_{IN}, plus transient voltage, determines the voltage rating required. With a maximum input voltage of 53V for this application, and if we allow a 10% adder for transients, a voltage rating of 60V or higher will suffice.

The RMS current through the each primary side FET can be determined from EQ. 17, substituting 5A of primary current for I_{OUT}. The result is 3.5A RMS. Fairchild FDS3672 FETs, rated at 100V and 7.5A ($r_{DS(ON)}$ = 22mΩ), were selected for the half-bridge switches.

The synchronous rectifier FETs must withstand approximately one half of the input voltage assuming no switching transients are present. This suggests a device capable of withstanding at least 30V is required. Empirical testing in the circuit revealed switching transients of 20V were present across the device indicating a rating of at least 60V is required.

The RMS current rating of 7.07A for each SR FET requires a low $r_{DS(ON)}$ to minimize conduction losses, which is difficult to find in a 60V device. It was decided to use two devices in parallel to simplify the thermal design. Two Fairchild FDS5670 devices are used in parallel for a total of four SR FETs. The FDS5670 is rated at 60V and 10A ($r_{DS(ON)}$ = 14mΩ).

Oscillator Component Selection

The desired operating frequency of 235kHz for the converter was established in the ***Design Criteria*** section. The oscillator frequency operates at twice the frequency of the converter because two clock cycles are required for a complete converter period.

During each oscillator cycle the timing capacitor, C_T, must be charged and discharged. Determining the required discharge time to achieve zero voltage switching (ZVS) is the critical design goal in selecting the timing components. The discharge time sets the deadtime between the two outputs, and is the same as ZVS transition time. Once the discharge time is determined, the remainder of the period becomes the charge time.

The ZVS transition duration is determined by the transformer's primary leakage inductance, L_{lk}, by the FET Coss, by the transformer's parasitic winding capacitance, and by any other parasitic elements on the node. The parameters may be determined by measurement, calculation, estimate, or by some combination of these methods.

$$t_{zvs} \approx \frac{\pi \sqrt{L_{lk} \bullet (2C_{oss} + C_{xfrmr})}}{2} \quad S \qquad \text{(EQ. 19)}$$

Device output capacitance, Coss, is non-linear with applied voltage. To find the equivalent discrete capacitance, Cfet, a charge model is used. Using a known current source, the time required to charge the MOSFET drain to the desired operating voltage is determined and the equivalent capacitance is calculated.

$$Cfet = \frac{Ichg \bullet t}{V} \quad F \qquad \text{(EQ. 20)}$$

Once the estimated transition time is determined, it must be verified directly in the application. The transformer leakage inductance was measured at 125nH and the combined capacitance was estimated at 2000pF. Calculations indicate a transition period of ~ 25ns. Verification of the performance yielded a value of T_D closer to 45ns.

The remainder of the switching half-period is the charge time, T_C, and can be found from

$$T_C = \frac{1}{2 \bullet F_S} - T_D = \frac{1}{2 \bullet 235 \bullet 10^3} - 45 \bullet 10^{-9} = 2.08 \quad \mu s \qquad \text{(EQ. 21)}$$

where F_S is the converter switching frequency.

Using Fig. 4, the capacitor value appropriate to the desired oscillator operating frequency of 470kHz can be selected. A C_T value of 100pF, 220pF, or 330pF is appropriate for this frequency. A value of 220pF was selected.

To obtain the proper value for R_{TD}, EQ. 3 is used. Since there is a 10ns propagation delay in the oscillator circuit, it must be included in the calculation. The value of R_{TD} selected is 8.06kΩ.

A similar procedure is used to determine the value of R_{TC} using EQ. 2. The value of R_{TC} selected is the series combination of 17.4kΩ and 1.27kΩ. See section ***Over Current Component Selection*** for further explanation.

Output Filter Design

The output filter inductor and capacitor selection is simple and straightforward. Under steady state operating conditions the voltage across the inductor is very small due to the large duty cycle. Voltage is applied across the inductor only during the switch transition time, about 45ns in this application. Ignoring the voltage drop across the SR FETs, the voltage across the inductor during the ON time with V_{IN} = 48V is

$$V_L = V_S - V_{OUT} = \frac{V_{IN} \bullet N_S \bullet (1 - D)}{2N_P} \approx 250 \quad mV \quad \text{(EQ. 22)}$$

where

V_L is the inductor voltage

V_S is the voltage across the secondary winding

V_{OUT} is the output voltage

If we allow a current ramp, ΔI, of 5% of the rated output current, the minimum inductance required is

$$L \geq \frac{V_L \bullet T_{ON}}{\Delta I} = \frac{0.25 \bullet 2.08}{0.5} = 1.04 \quad \mu H \quad \text{(EQ. 23)}$$

An inductor value of 1.4μH, rated for 18A was selected.

With a maximum input voltage of 53V, the maximum output voltage is about 13V. The closest higher voltage rated capacitor is 16V. Under steady state operating conditions the ripple current in the capacitor is small, so it would seem appropriate to have a low ripple current rated capacitor. However, a high rated ripple current capacitor was selected based on the nature of the intended load, multiple buck regulators. To minimize the output impedance of the filter, a Sanyo OSCON 16SH150M capacitor in parallel with a 22μF ceramic capacitor were selected.

Over Current Component Selection

There are two circuit areas to consider when selecting the components for over current protection, current limit and short circuit shutdown. The current limit threshold is fixed at 0.6V while the short circuit threshold is set to a fraction of the duty cycle the designer wishes to define as a short circuit.

The current level that corresponds to the over current threshold must be chosen to allow for the dynamic behavior of an open loop converter. In particular, the low inductor ripple current under steady state operation increases significantly as the duty cycle decreases.

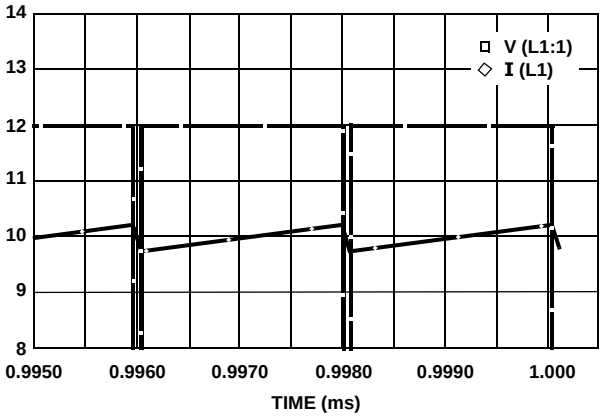


FIGURE 8. STEADY STATE SECONDARY WINDING VOLTAGE AND INDUCTOR CURRENT

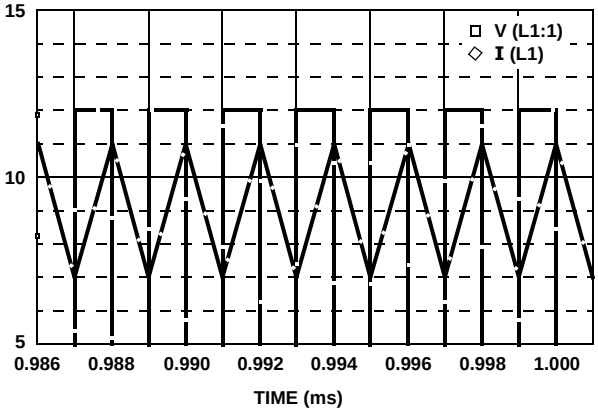


FIGURE 9. SECONDARY WINDING VOLTAGE AND INDUCTOR CURRENT DURING CURRENT LIMIT OPERATION

Figures 8 and 9 show the behavior of the inductor ripple under steady state and over current conditions. In this example, the peak current limit is set at 11A. The peak current limit causes the duty cycle to decrease resulting in a reduction of the average current through the inductor. The implication is that the converter can not supply the same output current in current limit that it can supply under steady state conditions. The peak current limit setpoint must take this behavior into consideration. A 3.32Ω current sense resistor was selected for the rectified secondary of current transformer T2, corresponding to a peak current limit setpoint of 16.5A.

The short circuit protection involves setting a voltage between 0 and 2V on the SCSET pin. The applied voltage divided by 2 is the percent of maximum duty cycle that corresponds to a short circuit when the peak current limit is active. A divider from RTC to ground provides an easy method to achieve this. The divider between RTC and GND

formed by R13 and R15 determines the percent of maximum duty cycle that corresponds to a short circuit. The divider ratio formed by R13 and R15 is

$$\frac{R13}{R13+R15} = \frac{1.27k}{1.27k+17.4k} = 0.068 \quad \text{(EQ. 24)}$$

Therefore, the duty cycle that corresponds to a short circuit is 6.8% of D max (97.9%), or ~6.6%.

Performance

The major performance criteria for the converter are efficiency, and to a lesser extent, load regulation. Efficiency, load regulation and line regulation performance are demonstrated in the following Figures.

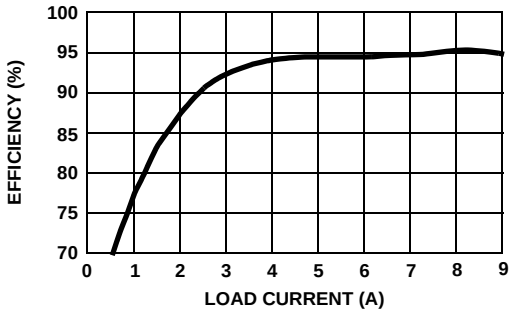


FIGURE 10. EFFICIENCY vs LOAD V_{IN} = 48V_t

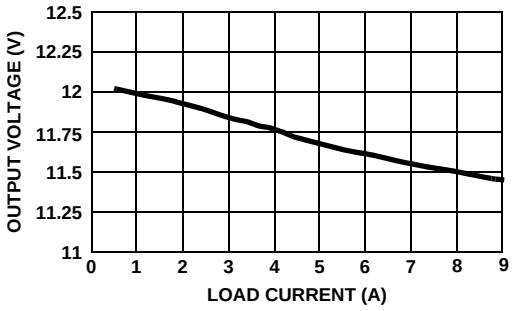


FIGURE 11. LOAD REGULATION AT V_{IN} = 48V

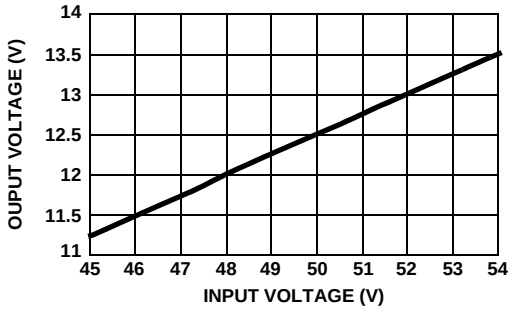


FIGURE 12. LINE REGULATION AT I_{OUT} = 1A

As expected, the output voltage varies considerably with line and load when compared to an equivalent converter with closed loop feedback. However, for applications where tight regulation is not required, such as those application that use downstream DC-DC converters, this design approach is viable.

Waveforms

Typical waveforms can be found in the following Figures. Figure 13 shows the output voltage during start up.

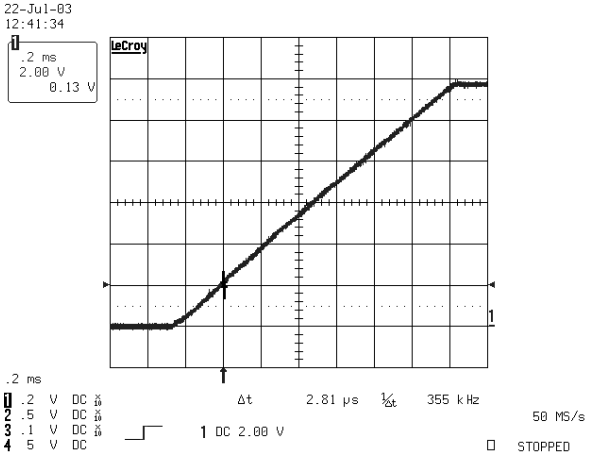


FIGURE 13. OUTPUT SOFT START

Figure 14 shows the output voltage ripple and noise at a 5A load.

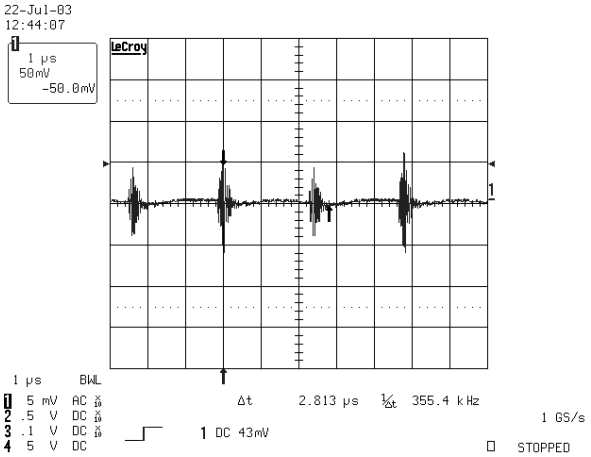


FIGURE 14. OUTPUT RIPPLE AND NOISE - 20MHz BW

Figures 15 and 16 show the voltage waveforms at the switching node shared by the upper FET source and the lower FET drain. In particular, Figure 16 shows near ZVS operation at 8A of load when the upper FET is turning off and the lower FET turning on. There is insufficient energy stored in the leakage inductance to allow complete ZVS operation. However, since the energy stored in the node capacitance is proportional to V^2, a significant portion of the energy is still recovered. Figure 17 shows the switching transition between outputs, OUTA and OUTB during steady state operation. The deadtime duration of 48.6ns is clearly shown.

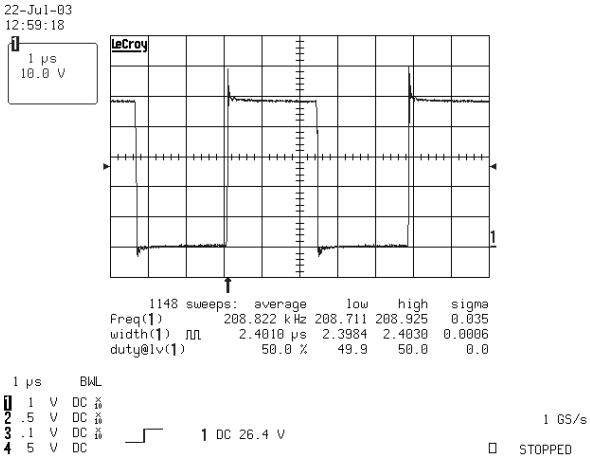


FIGURE 15. FET DRAIN-SOURCE VOLTAGE

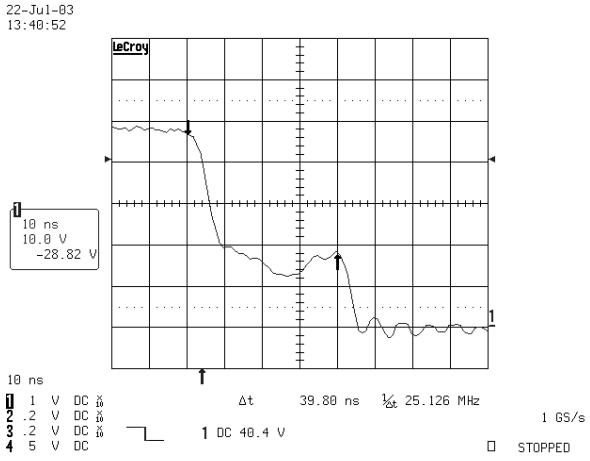


FIGURE 16. FET D-S VOLTAGE NEAR-ZVS TRANSITION

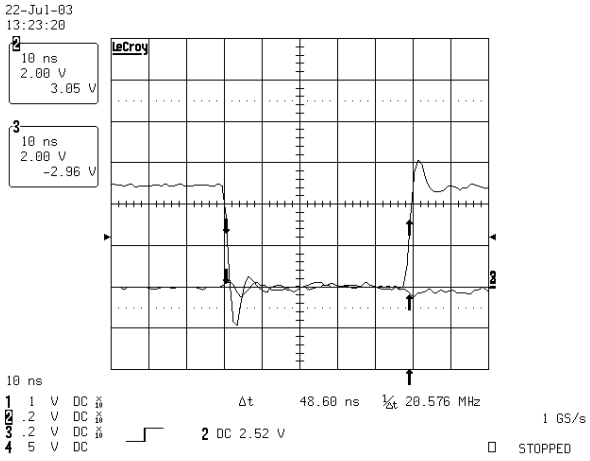


FIGURE 17. OUTA - OUTB TRANSITION

Component List

REFERENCE DESIGNATOR	VALUE	DESCRIPTION
C1	1.0µF	Capacitor, 1812, X7R, 100V, 20% TDK C4532X7R2A105M
C2, C3	3.3µF	Capacitor, 1812, X5R, 50V, 20% TDK C4532X5R1H335M
C4, C6	1.0µF	Capacitor, 0805, X5R, 16V, 10% TDK C2012X5R1C105K
C5, C15, C16	0.1µF	Capacitor, 0603, X7R, 50V, 10% TDK C1608X7R1H104K
C7	Open	Capacitor, 0603, Open
C8	22µF	Capacitor, 1812, X5R, 16V, 20% TDK C4532X5R1C226M
C9	150µF	Capacitor, Radial, Sanyo 16SH150M
C10, C11, C12, C13, C14	1000pF	Capacitor, 0603, X7R, 50V, 10% TDK C1608X7R1H102K
C17	220pF	Capacitor, 0603, COG, 16V, 5% TDK C1608COG1C221J
C18	0.047µF	Capacitor, 0603, X7R, 16V, 10% TDK C1608X7R1C473K
CR1, CR2		Diode, Schottky, BAT54S
CR3		Diode, Schottky, BAT54
D1		Zener, 10V, Philips BZX84C10ZXCT-ND
L1	190nH	Pulse, P2004T
L2	1.5µH	Pulse, PG0077.142
L3	Short	Jumper or Optional Discrete Leakage Inductance
Q5		Transistor, ON MJD31C
QL, QH		FET, Fairchild FDS3672
QR1, QR2, QR3, QR4		FET, Fairchild FDS5670
R1, R10	3.3	Resistor, 2512, 5%
R2	3.01K	Resistor, 2512, 1%
R3, R6	10.0	Resistor, 0603, 1%
R5	3.32	Resistor, 0603, 1%
R7	75.0K	Resistor, 0805, 1%
R8, R9	20.0	Resistor, 0805, 1%
R11	100	Resistor, 0603, 1%
R12	8.06K	Resistor, 0603, 1%
R13	17.4K	Resistor, 0603, 1%
R14	Open	Resistor, 0603, Open
R15	1.27K	Resistor, 0603, 1%
R17	97.6K	Resistor, 0603, 1%
R18	3.01K	Resistor, 0603, 1%
R19, RT1	10.0K	Resistor, 0603, 1%
T1		Midcom 31718
T2		Pulse P8205T
U1		Intersil HIP2101IB
U3		ISL6740IB

Adding Line Only Regulation - Feed Forward

Output voltage variation caused by changes in the supply voltage may be virtually removed through a technique known as feed forward compensation. Using feed forward, the duty cycle is directly controlled based on changes in the input voltage only. No closed loop feedback system is required. Voltage feed forward may be implemented as shown below.

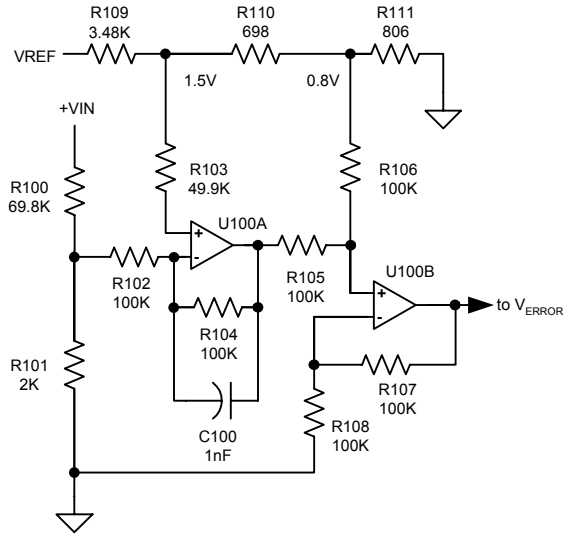


FIGURE 18. VOLTAGE FEED FORWARD CIRCUIT

The circuit provides feed forward compensation for a 2:1 input voltage range. Resistors R100 and R101 set the input voltage divider to generate a 1.00 volt signal at the input voltage that corresponds to maximum duty cycle (V_{IN} minimum). Resistors R109, R110, and R111 form a voltage divider from VREF to create reference voltages for the amplifiers. The first stage uses U100A, R102, R103, R104, and C100 to form a unity gain inverting amplifier. Its output varies inversely with input voltage and ranges from 1 to 2V. The bandwidth of the circuit may be controlled by varying the value of C100. The gain of the first amplifier stage is:

$$V_A = -V_D + 3.00 \quad V \qquad \text{(EQ. 25)}$$

where:

V_A = Output voltage of U100A

V_D = The input divider voltage

The second stage uses U100B, R105, R106, R107, and R108 to form a summing amplifier which offsets the first stage output by 0.8V (the value of CT valley voltage). The signal applied to the V_{ERROR} input now matches the offset and amplitude of the oscillator sawtooth so that the duty cycle varies linearly from 100% to 50% of maximum with a 2:1 input voltage variation.

Other duty ranges are possible, but are still limited to a 2:1 ratio. The voltage applied to V_{ERROR} must be scaled to the peak-to-peak voltage on CT, and offset by the valley voltage. Since the peak-to-peak CT voltage is 2.00V nominal, the voltage at the output of U100A must be divided by 2.0V to obtain the desired duty cycle. For example, if an 80% duty cycle was required at the minimum operating voltage, the output of U100A must be 1.60V (80% of 2.00V). From (EQ. 25), the divider voltage must be set to 1.4V for the input voltage that corresponds to the 80% duty cycle.

It should be noted that the synchronous rectifiers (SRs), being driven from the transformer secondary, are only gated on during the ON time of the primary FETs. Conduction continues through the body diodes during the OFF time when operating in continuous inductor current mode. This mode of operation usually results in significant conduction and switching losses in the SR FETs. These losses may be reduced considerably by either adding schottky diodes in parallel to the SR FETs or by driving the SR FETs directly with a control signal.

Adding Regulation - Closed Loop Feedback

The second Typical Application schematic adds closed loop feedback with isolation. The ISL6740EVAL2 demonstration platform implements this design and is available for evaluation. The input voltage range was increased to 36V - 75V, which necessitates a few modifications to the open loop design. The output inductor value was increased to 4.0µH, schottky rectifier CR4 was added to minimize SR FET body diode conduction, the turns ratio of the main transformer was changed to 4:3, and the synchronous rectifier gate drives were modified. The design process is essentially the same as it was for the unregulated version, so only the feedback control loop design will be discussed.

The major components of the feedback control loop are a programmable shunt regulator and an opto-coupler. The opto-coupler is used to transfer the error signal across the isolation barrier. The opto-coupler offers a convenient means to cross the isolation barrier, but it adds complexity to the feedback control loop. It adds a pole at about 10kHz and a significant amount of gain variation due the current transfer ratio (CTR). The CTR of the opto-coupler varies with initial tolerance, temperature, forward current, and age.

A block diagram of the feedback control loop follows in Figure 19.

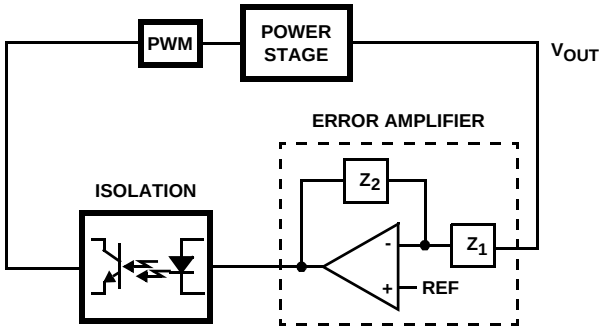


FIGURE 19. CONTROL LOOP BLOCK DIAGRAM

The loop compensation is placed around the Error Amplifier (EA) on the secondary side of the converter. A Type 3 error amplifier configuration was selected.

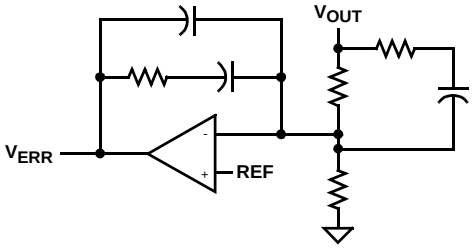


FIGURE 20. TYPE 3 ERROR AMPLIFIER

The control to output transfer function may be represented as [1]

$$\frac{v_o}{v_c} = \frac{V_{IN}}{V_S \bullet 2} \bullet \frac{N_S}{N_P} \bullet \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{(Q)\omega_o} + \left(\frac{s}{\omega_o}\right)^2} \quad \text{(EQ. 26)}$$

where

$$Q = \frac{R_o}{\omega_o \bullet L}$$

$$\omega_o = \frac{1}{\sqrt{LC}} \quad \text{or} \quad f_o = \frac{1}{2\pi\sqrt{LC}}$$

$$\omega_z = \frac{1}{R_c C} \quad \text{or} \quad f_z = \frac{1}{2\pi R_c C}$$

R_O = Output Load Resistance

L = Output Inductance

C = Output Capacitance

R_C = Output Capacitance ESR

V_S = Sawtooth Ramp Amplitude

Gain and phase plots of (EQ. 26) appear below using L = 4.0µH, C = 150µF, Rc = 28mΩ, Ro = 1.2Ω, and Vin = 75V.

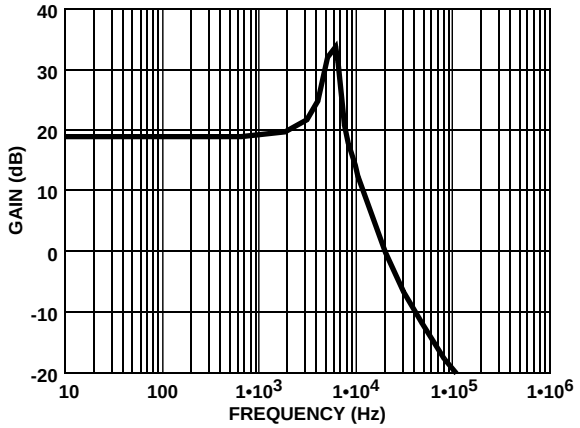


FIGURE 21A. CONTROL-TO-OUTPUT GAIN

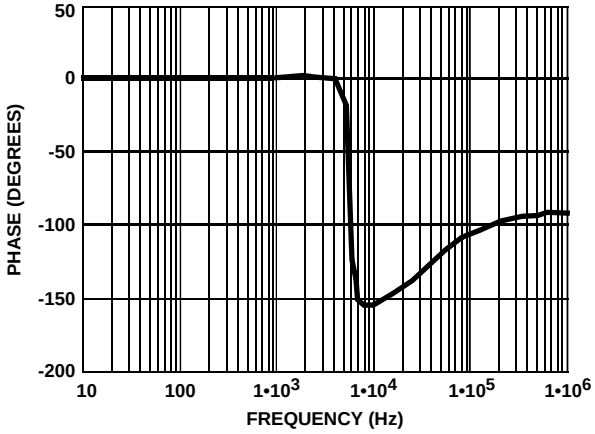


FIGURE 21B. CONTROL-TO-OUTPUT PHASE

The Type 3 compensation configuration has three poles and two zeros. The first pole is at the origin, and provides the integration characteristic which results in excellent DC regulation. Referring to the Typical Application Schematic for the regulated output, the remaining poles and zeros for the compensator are located at:

$$f_{p2} = \frac{1}{2\pi \bullet R21 \bullet C20} \quad \text{(EQ. 27)}$$

$$f_{p3} \approx \frac{1}{2\pi \bullet R4 \bullet C22} \quad C19 \gg C20 \quad \text{(EQ. 28)}$$

$$f_{z1} = \frac{1}{2\pi \bullet R21 \bullet C19} \quad \text{(EQ. 29)}$$

$$f_{z2} \approx \frac{1}{2\pi \bullet R23 \bullet C22} \quad R23 \gg R4 \quad \text{(EQ. 30)}$$

From (EQ. 26), it can be seen that the control to output transfer function frequency dependence is a function of the output load resistance, the value of output capacitor and inductor, and the output capacitance ESR. These variations must be considered when compensating the control loop. The worst case small signal operating point for a voltage mode converter tends to be at maximum Vin, maximum load, maximum Cout, and minimum ESR.

The higher the desired bandwidth of the converter, the more difficult it is to create a solution that is stable over the entire operating range. A good rule of thumb is to limit the bandwidth to about Fsw/4, where Fsw is the switching frequency of the converter. However, due to the bandwidth constraints of the opto-coupler and the LM431 shunt regulator, the bandwidth was reduced to about 25kHz.

The first pole is placed at the origin by default (C20 is an integrating capacitor). If the two zeroes are placed at the same frequency, they should be placed at $f_{LC}/2$, where f_{LC} is the resonant frequency of the output L-C filter. To reduce the gain peaking at the L-C resonant frequency, the two zeroes are often separated. When they are separated, the first zero may be placed at $f_{LC}/5$, and the second at just above f_{LC}. The second pole is placed at the lowest expected zero cause by the output capacitor ESR. The third, and last pole is placed at about 1.5 times the cross over frequency.

Some liberties where taken with the generally accepted compensation procedure described above due to the transfer characteristics of the opto coupler. The effects of the opto-coupler tend to dominate over those of the LM431 so the GBWP effects of the LM431 are not included here.

The gain and phase characteristics of the opto coupler are shown below.

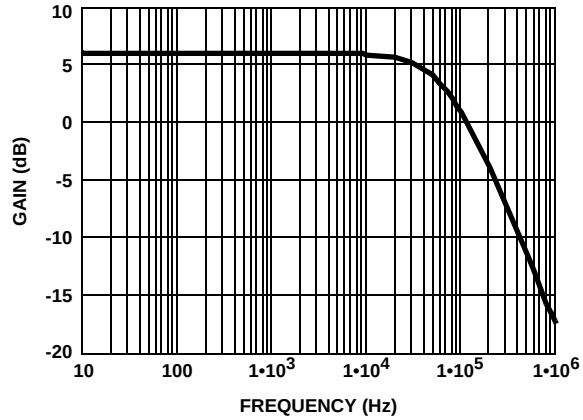


FIGURE 22A. OPTO COUPLER GAIN

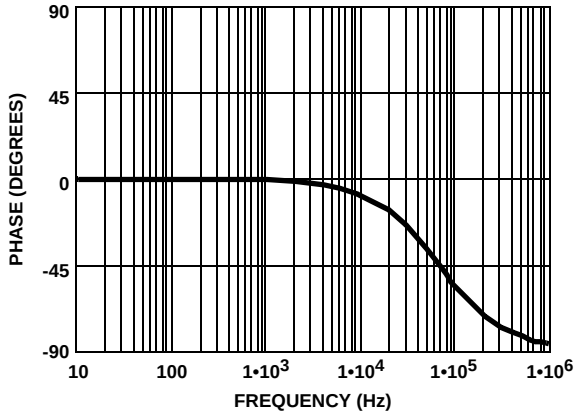


FIGURE 22B. OPTO COUPLER

The following compensation components were selected

R23 = 9.53kΩ

R24 = 2.49kΩ

R4 = 499Ω

R21 = 4.22kΩ

C22 = 1nF

C20 = 82pF

C19 = 0.22µF

From (EQ. 27-30), the poles and zeroes are:

f_{z1} = 171Hz

f_{z2} = 16.7kHz

f_{p2} = 460kHz

f_{p3} = 319kHz

The calculated gain and phase plots of the error amplifier appear below using an ideal op amp.

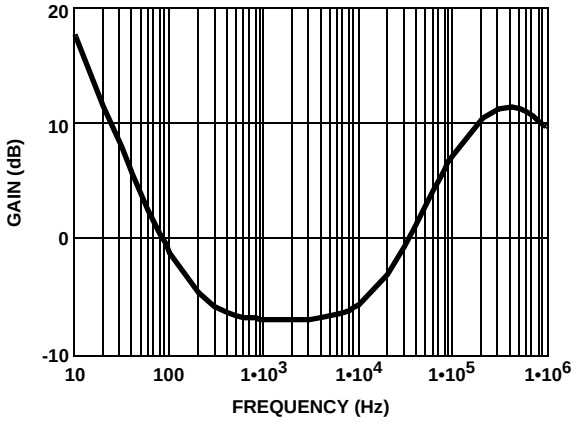


FIGURE 23A. IDEAL ERROR AMPLIFIER GAIN

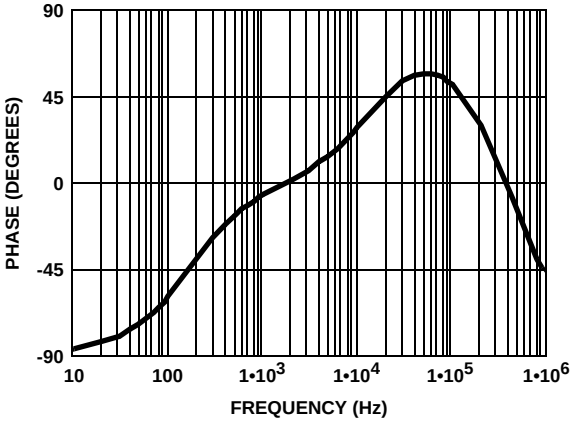


FIGURE 23B. IDEAL ERROR AMPLIFIER PHASE

The gain and phase plots combined with the opto coupler's transfer characteristics appear below:

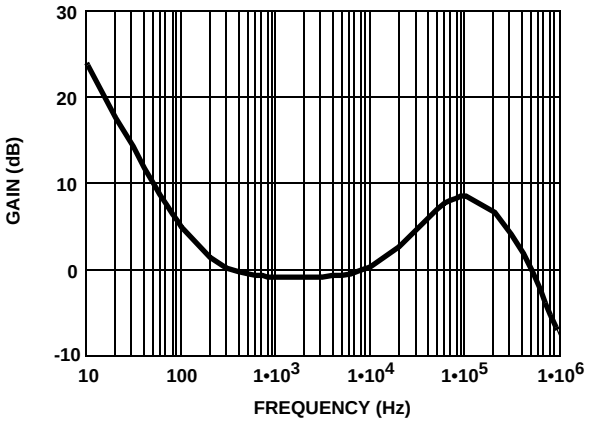


FIGURE 24A. EA PLUS OPTO COUPLER GAIN

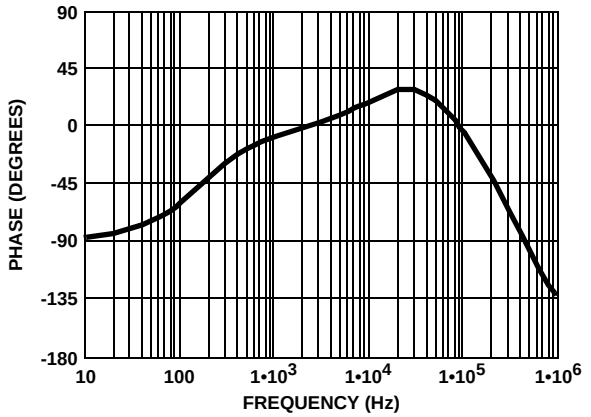


FIGURE 24B. EA PLUS OPTO COUPLER GAIN

Using the control-to-output transfer function combined with the EA transfer function, the loop gain and phase may be predicted. The predicted loop gain and phase margin of the converter appear below:

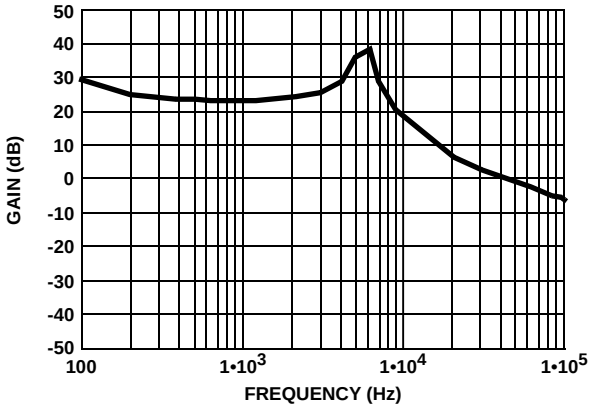


FIGURE 25A. PREDICTED LOOP GAIN

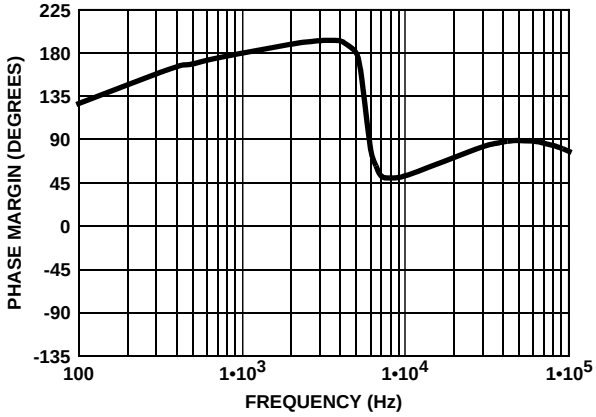


FIGURE 25B. PREDICTED LOOP PHASE MARGIN

The actual loop gain and phase margin measured on the ISL6740EVAL2 demonstration board appear below:

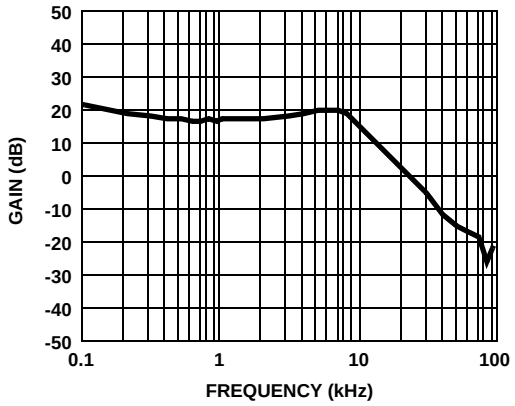


FIGURE 26A. MEASURED LOOP GAIN

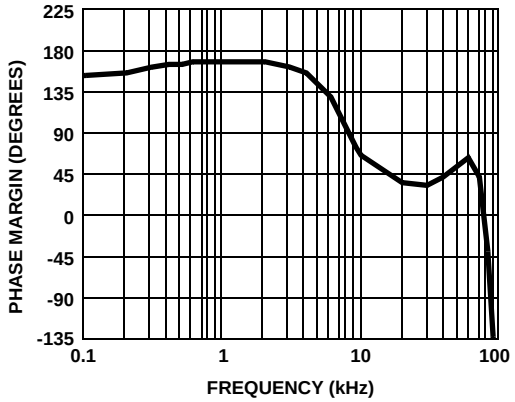


FIGURE 26B. MEASURE LOOP PHASE MARGIN

The only major discrepancies between the predicted behavior and the measured results are the Q of the L-C filter and the phase behavior above 60kHz. The actual Q appears to be significantly less than predicted resulting in less gain peaking and a less rapid phase shift near the resonant frequency. This is most likely the result of neglecting other losses in the converter's output, such as the FET on resistance, copper losses, and inductor resistance. The phase discrepancy above 60kHz is not particularly relevant to the loop performance since it occurs well above the cross over frequency. The predicted behavior indicates a much gentler drop off of phase than was observed in the measured performance. The discrepancy was not investigated.

Performance

The major performance criteria for the converter are efficiency and load regulation. These quantities are detailed in the following Figures.

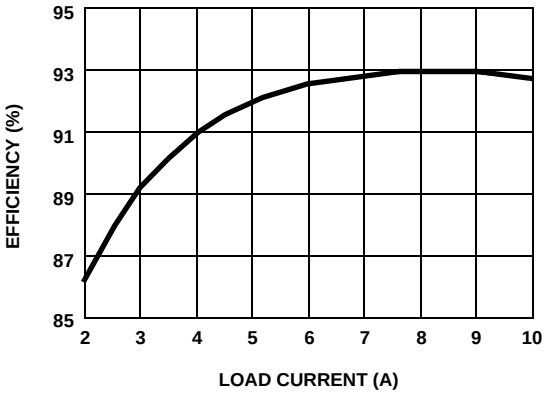


FIGURE 27. EFFICIENCY vs LOAD V_{IN} = 48V_t

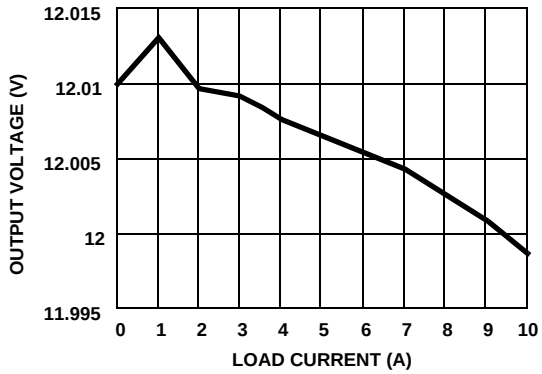


FIGURE 28. LOAD REGULATION AT V_{IN} = 48V

The efficiency, although very good, could be further improved using a controlled SR method instead of using a self-driven method with an auxiliary schottky diode. The schottky diode conducts when the main switching FETs are off. Its forward voltage drop is considerably larger than that of the SR FETs and causes a measurable reduction in efficiency. The effect becomes more significant as the input voltage is increased due to the reduction of duty cycle (and consequent increase in the OFF time).

Component List

REFERENCE DESIGNATOR	VALUE	DESCRIPTION
C1	1.0µF	Capacitor, 1812, X7R, 100V, 20% TDK C4532X7R2A105M
C2, C3	3.3µF	Capacitor, 1812, X5R, 50V, 20% TDK C4532X5R1H335M
C4, C6	1.0µF	Capacitor, 0805, X5R, 16V, 10% TDK C2012X5R1C105K
C5, C15, C16	0.1µF	Capacitor, 0603, X7R, 50V, 10% TDK C1608X7R1H104K
C7	Open	Capacitor, 0603, Open
C8, C21	22µF	Capacitor, 1812, X5R, 16V, 20% TDK C4532X5R1C226M
C9	150µF	Capacitor, Radial, Sanyo 16SH150M
C10, C14, C22	1000pF	Capacitor, 0603, X7R, 50V, 10% TDK C1608X7R1H102K
C11, C12	560 pF	Capacitor, 0603, X7R, 100V, 10% TDK C1608X7R2A561K
C13	220pF	Capacitor, 0603, X7R, 100V, 10% TDK C1608X7R2A221K
C17	220pF	Capacitor, 0603, COG, 16V, 5% TDK C1608COG1C221J
C18	0.047µF	Capacitor, 0603, X7R, 16V, 10% TDK C1608X7R1C473K
C19	0.22µF	Capacitor, 0603, X7R, 16V, 10% TDK C1608X7R1C224K
C20	82pF	Capacitor, 0603, X7R, 16V, 10% TDK C1608X7R1C820K
CR1, CR2		Diode, Schottky, BAT54S
CR3, CR5, CR6		Diode, Schottky, BAT54
CR4		Diode, Schottky, IR 12CWQ06FN
D1		Zener, 10V, Philips BZX84C10ZXCT-ND
D2		Zener, 6.8V, Philips BZX84C6Z8XCT-ND
L1	190nH	Pulse, P2004T
L2	4.0µH	BI Technologies, HM65-H4R0
L3	Short	0 Ohm Jumper
Q5		Transistor, ON MJD31C
QL, QH, QR1, QR2, QR3, QR4		FET, Fairchild FDS3672
R1	3.3	Resistor, 2512, 5%
R2	3.01K	Resistor, 2512, 2%
R3	10.0	Resistor, 0603, 1%
R4, R25	499	Resistor, 0603, 1%
R5	2.20	Resistor, 0805, 1%

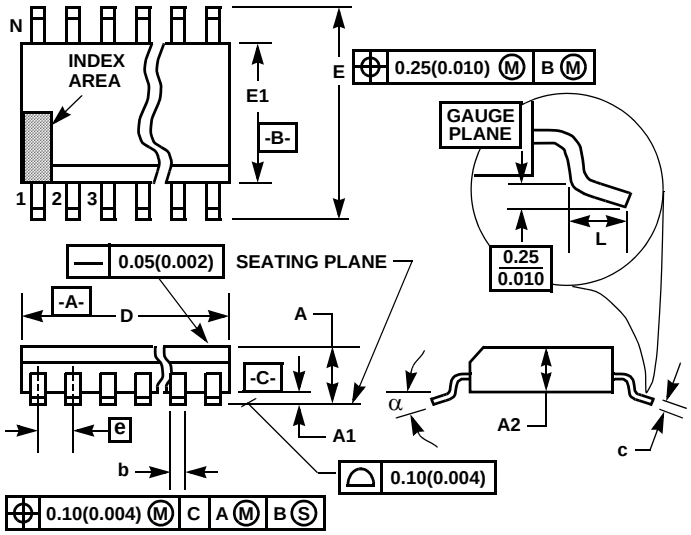
Component List (Continued)

REFERENCE DESIGNATOR	VALUE	DESCRIPTION
R6	200	Resistor, 0603, 1%
R7	75.0K	Resistor, 0805, 1%
R8, R9, R10	18	Resistor, 2512, 5%
R11	205	Resistor, 0603, 1%
R12	8.06K	Resistor, 0603, 1%
R13	18.2K	Resistor, 0603, 1%
R14	Open	Resistor, 0603, Open
R15	1.27K	Resistor, 0603, 1%
R16, R19	1.00K	Resistor, 0603, 1%
R17	97.6K	Resistor, 0603, 1%
R18	3.01K	Resistor, 0603, 1%
R20	2.00K	Resistor, 0603, 1%
R21	4.22K	Resistor, 0603, 1%
R23	9.53K	Resistor, 0603, 1%
R24	2.49K	Resistor, 0603, 1%
R26, R27	5.11	Resistor, 0805, 1%
RT1	10.0K	Resistor, 0603, 1%
T1		Midcom 31660
T2		Pulse P8205T
U1		Intersil HIP2101IB
U2		NEC PS2801-1
U3		ISL6740IB
U4		National LM431BIM3/N1C

References

[1] Dixon, Lloyd H., “Closing the Feedback Loop”, Unitrode Power Supply Design Seminar, SEM-700, 1990.

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AB, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M16.173

16 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.043	-	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.033	0.037	0.85	0.95	-
b	0.0075	0.012	0.19	0.30	9
c	0.0035	0.008	0.09	0.20	-
D	0.193	0.201	4.90	5.10	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.020	0.028	0.50	0.70	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

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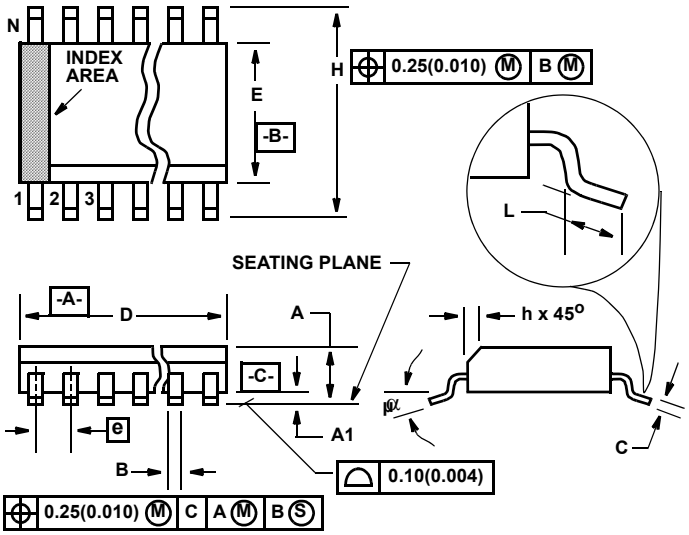
Small Outline Plastic Packages (SOIC)



M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
B	0.014	0.019	0.35	0.49	9
C	0.007	0.010	0.19	0.25	-
D	0.386	0.394	9.80	10.00	3
E	0.150	0.157	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.228	0.244	5.80	6.20	-
h	0.010	0.020	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.