OKI Semiconductor

MSM6322

PITCH CONTROL LSI FOR THE SPEECH SIGNAL

GENERAL DESCRIPTION

The MSM6322 converts in realtime the pitch of the speech signal in a range of one octave upward or downward.

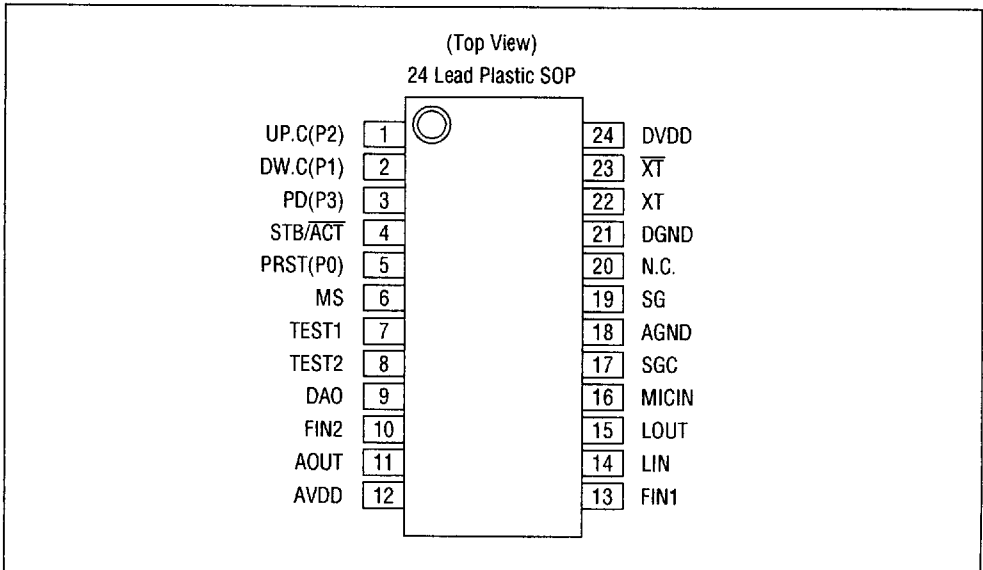Two pitch control methods can be selected. One is to change the pitch in 17 steps by two switch inputs, and the other is to select one of 16 steps by four binary input lines.

Since a microphone preamplifier and a low pass filter are built in, the pitch conversion set can easily be configured by connecting a microphone, amplifier and speaker in the peripheral circuit.
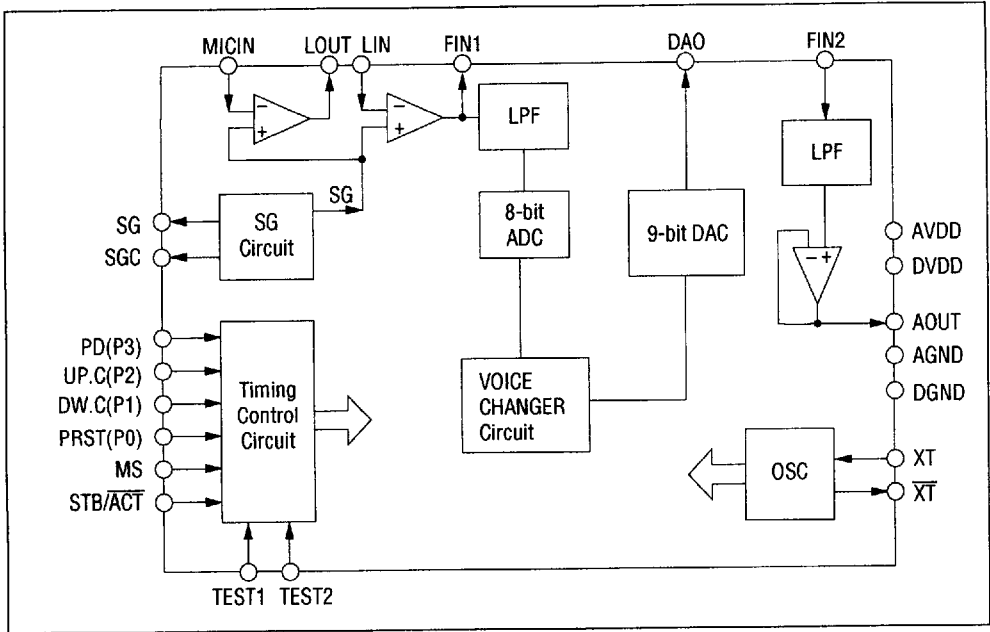
FEATURES

- Built-in microphone preamplifier
- Built-in low pass filters (4th order LPF on input and 3rd order LPF on output)
- Built-in 8-bit AD converter
- Built-in 9-bit DA converter
- Speech pitch alterable in 17 steps
- Oscillation frequency at 4 MHz

- 5V single power supply
- Silicon construction (Si gate CMOS IC)
  Note) Designed for application to home electronic equipment (toys).
- 24-pin plastic SOP (SOP24-P-430-K)

PIN ASSIGNMENT

(Top View)
24 Lead Plastic SOP

UP.C(P2)	1		24	DVDD
DW.C(P1)	2		23	$\overline{XT}$
PD(P3)	3		22	XT
STB/$\overline{ACT}$	4		21	DGND
PRST(P0)	5		20	N.C.
MS	6		19	SG
TEST1	7		18	AGND
TEST2	8		17	SGC
DAO	9		16	MICIN
FIN2	10		15	LOUT
AOUT	11		14	LIN
AVDD	12		13	FIN1

CIRCUIT CONFIGURATION

ELECTRICAL CHARACTERISTICS

- **Absolute Maximum Ratings**

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage (1)	DVDD		−0.3 ~ +7.0	V
Supply voltage (2)	AVDD	For DGND and	−0.3 ~ +7.0	V
Analog input voltage	V_IN (ANALOG)	AGND Ta = 25°C	AGND −0.3 ~ AVDD +0.3	V
Digital input voltage	V_IN (DIGITAL)		DGND −0.3 ~ AVDD +0.3	V
Storage temperature range	T_stg	—	−55 ~ +150	°C

- **Operating Ratings**

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage (1)	DVDD	For DGND	4.0 ~ 6.0	V
Supply voltage (2)	AVDD	For AGND	4.0 ~ 6.0	V
Rated operating temperature range	Top	–	−40 ~ 85	°C

• DC Characteristics

(Ta = -40~+85°C, F_{OSC} = 4MHz, DVDD = AVDD = 4.5V~5.5V, DGND = AGND = 0V)

Parameter		Symbol	Conditions	Limits			Unit
				Min.	Typ.	Max.	
"H" input voltage (excluding XT and RST)		$V_{IH}(1)$	–	3.6	–	–	V
"H" input voltage (applicable to XT and RST)		$V_{IH}(2)$	–	$0.8 \times VDD$	–	–	V
"L" input voltage		V_{IL}	–	–	–	0.8	V
"H" input current for match 3, 4, 6, 22, 23 pin		I_{IH1}	V_{IH} = DVDD	–	–	10	μA
"H" input current for match 1, 2, 5, 7, 8 pin		I_{IH2}	V_{IH} = DVDD	–	–	400	μA
"L" output current		I_{IL}	V_{IL} = DGND	–10	–	–	μA
Output impedance	LOUT	RO_{LOUT}	–	–	15	–	kΩ
Output impedance	DAO	RO_{DAO}	–	–	10	–	kΩ
	AOUT	RO_{AOUT}	–	–	15	–	kΩ
	FIN1	RO_{FIN1}	–	–	15	–	kΩ
Input impedance	MICIN	RI_{MICIN}	–	–	100	–	MΩ
	LIN	RI_{LIN}	–	–	100	–	MΩ
	FIN2	RI_{FIN2}	–	–	30	–	MΩ
AD conversion precision		$IV_{ADE}I$	AVDD = DVDD = 5V	–	–	40	mV
DA conversion precision		$IV_{DAE}I$	AVDD = DVDD = 5V No load	–	–	40	mV
Operating current consumption		I_{DD}	In case of 4 MHz oscillator	–	–	10	mA
Standby current		I_{DS}	In case of 4 MHz oscillator with STB/$\overline{ACT}$ = "H"	–	–	7	mA
Power down current		I_{DP}	In case of PD = "H"	–	–	10	μA

• AC Characteristics

(Ta = −40~85°C, F_{OSC} = 4MHz, DVDD = AVDD = 4.5V~5.5V, DGND = AGND = 0V)

Parameter	Symbol	Conditions	Min.	Max.	Unit
DAO output delay from falling edge of STB/$\overline{ACT}$	t_{CSD}	−	−	15.36	ms
DAO output delay from falling edge of PD	t_{PDD}	−	−	15.36	ms
Pulse width of PRST, UP.C, DW.C pulses	t_{UDPW}	−	61.44	−	ms
Time between UP.C, and DW.C pulses	t_{RUD}	−	30.72	−	ms
Scale change delay from positive edge of PRST	t_{CHG1}	−	61.44	−	ms
Scale change delay from falling edge of UP.C and DW.C	t_{CHG2}	−	−	15.36	ms
Maximum operating frequency	t_{CMAX}	−	−	4.5	MHz

• LPF Characteristics

(Ta = 25°C, AVDD = DVDD = 4.5V~5.5V,,
DGND = AGND = 0V)

Frequency (Hz)	Gain characteristic (dB)		
	Min.	Typ.	Max.
300 ~ fc	−3.0	−	3.0
fc	−	−3.0	−
2 × fc	−	−	−20.0

See the pitch conversion Table

TIMING DIAGRAM
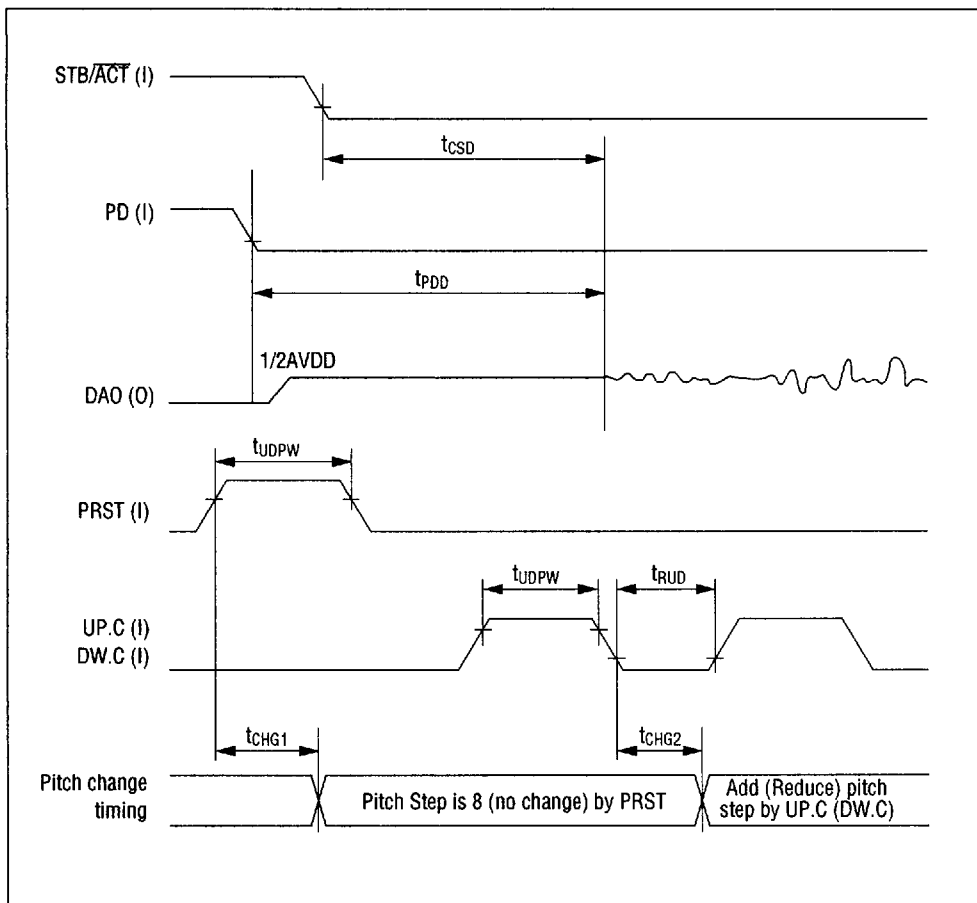
- **PIN FUNCTION** (Setting method = "UP/DOWN") [MS pin fixed to "L"]

Pin Name	I/O	Function
MS	I	Mode select pin always connected to the "L" level.
MICIN	I	Connects the microphone input via a coupling capacitor.
LOUT	O	Output obtained by amplifying the audio signal input from the microphone.
LIN	I	Input pin for connecting the LOUT output or line out signal from other audio equipment.
FIN1	O	Sets the input audio signal amplitude in combination with the LIN pin. The gain of the built-in amplifier can be set by two pins each of MICIN and LOUT, and LIN and FIN1.
UP.C	I	Pulse switch input to raise the pitch by one stage at a time.
DW.C	I	Pulse switch input to lower the pitch by one stage at a time. The pitch varies by one stage upward (or downward) each time a pulse is input to the UP.C (or DW.C) pin along the 17 stages shown in the pitch conversion table. Cyclic up or down operation is also possible.
STB/$\overline{ACT}$	I	Standby/active pin. When the standby/$\overline{active}$ is at the "H" level, the processing is interrrupted by stopping only the clocks other than the oscillator clock. The DAO pin outputs 1/2 V_{DD} for about 15ms (in case of 4MHz oscillator) after the standby/$\overline{active}$ goes to the "L" level.
PD	I	Power down pin. All clocks including the oscillator are stopped when the power down pin is set to the "H" level. The DAO pin outputs the "L" level in this state. It requires ten milliseconds after the power down pin is set to the "L" level until clock stabilization.
PRST	I	Reset pin to connect the pulse switch input to set the scale to stage 8 upon resetting.
TEST1 TEST2	I	Test pins to be fixed to the "L" level.
XT, $\overline{XT}$	I, O	Crystal oscillator connecting pins
SG,SGC	I	Reference voltage pins.
DAO	O	DA converter output.
FIN2	I	Input pin for built-in filter (for output).
AOUT	O	Output pin for built-in filter (for output).
DGND DVDD	—	Power supply pins.
AGND AVDD	—	Analog power supply pins.

• **PIN FUNCTION** (Setting method = "BIN") [MS pin fixed to "H"]

| Pin Name	I/O	Function
MS	I	Mode select pin always connected to the "H" level.
MICIN	I	Pin for connecting the microphone input via a coupling capacitor.
LOUT	O	Output obtained by amplifying the audio signal input from the microphone.
LIN	I	Input pin for connecting the LOUT output or line out signal from other audio equipment.
FIN1	O	Sets the input audio signal amplitude in combination with the LIN pin. The gain of the built-in amplifier can be set by two pins each of MICIN and LOUT, and LIN and FIN1.
P3 P2 P1 P0	I	16 stages are set by 4-bit of P3 (MSB) to P0 (LSB). Stages 0 (p3=p2=p1=p0=0) to 16 (P3=P2=P1=P0=1) shown on the pitch conversion table can be set.
STB/$\overline{ACT}$	I	Chip select pin. The processing is interrupted by stopping clocks other then the oscillator when the chip select pin level "H". The DAO outputs 1/2 VDD for about 15ms (in case of 4 MHz oscillator) after the chip select pin is set to the "L" level.
TEST1 TEST2	I	Test pins to be fixed to the "L" level.
XT, $\overline{XT}$	I, O	Crystal oscillator connecting pins.
SG,SGC	I	Reference voltage input pins.
DAO	O	DA converter output pin.
FIN2	I	Input pin for built-in filter (for output).
AOUT	O	Output pin for built-in filter (for output).
DGND DVDD	—	Power supply pins.
AGND AVDD	—	Analog power supply pins.

FUNCTIONAL EXPLANATION

- **Analog Input/output (MICIN, LOUT, LIN and FIN1)**

These pins are to connect microphone or other audio equipment line inputs and to set the input gain. Fig.1 shows the basic circuit. Amplifier 1, and the LIN and FIN1 pins are connected to the input and output of amplifier 2.
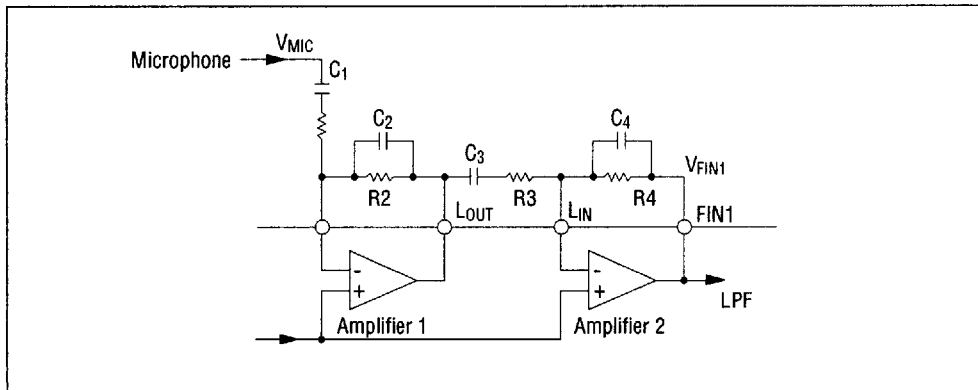
Figure 1 Analog Input Block
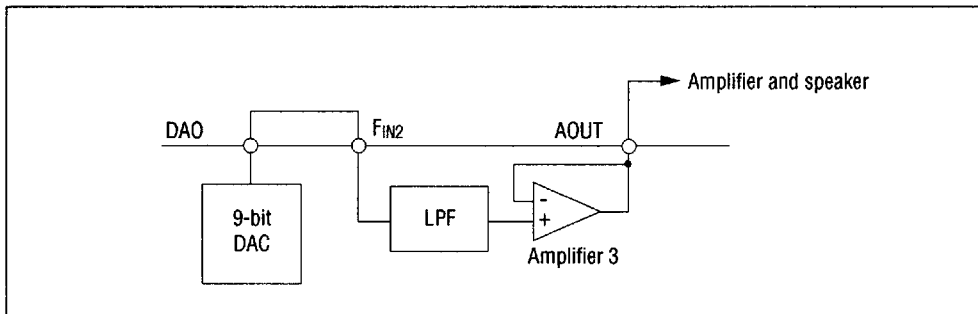
Figure 2 Analog Output Block

The output of amplifier 2 is also connected to the LPF (low pass filter) configured by the SCF (switched capacitance filter).

For input from the microphone, DC cutoff of the microphone input is carried out by capacitor C1 (approx. 1μF), (1/2 AVDD becomes the center internally.)

The amplitude (generally ten millivolts) of the microphone input is amplified by R1 and R2 (to $V_{LOUT} = (R2/R1)*V_{MIN}$). Similarly, the DC component of the LOUT output is cut off by capacitor C3 (approx. 1μF), and the resultant signal is amplified by R3 and R4 (to $V_{FIN1} = (R4/R3)*V_{LOUT}$).

Capacitors C2 and C4 are to prevent oscillation of the internal amplifier. 20 to 50pF is used.

When considering connection of other audio equipment, it is recommended to suppress the maximum amplitude at the LOUT pin to within 500mV. The maximum amplitude shall be suppressed to within 5V (AVDD - AGND voltage width) by the FIN1 pin.

- **Analog Output (DAO, FIN2 and AOUT)**

The output signal after scale conversion is output through the 9-bit DAC (digital-analog converter) to the DAO pin. The maximum amplitude of this signal is ±2.5V with 1/2 AVDD as the reference voltage. The DAO signal again goes through the internal LPF using SCF to amplifier 3 for impedance conversion, and the resultant signal is output from the AOUT pin.

It is possible to insert an external filter or equalizer between the DAO and FIN2 pins.

- **Analog Reference Voltage (SG and SGC)**

The SG and SGC pins are to connect external capacitors for stabilizing the internal analog reference voltage of 1/2 AVDD.

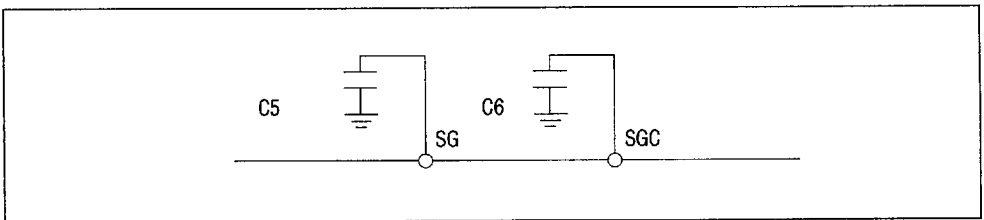Connect respective these pins to the ground through capacitor C5 or C6 as shown in Fig. 3.

Figure 3 Analog Reference Voltage Block
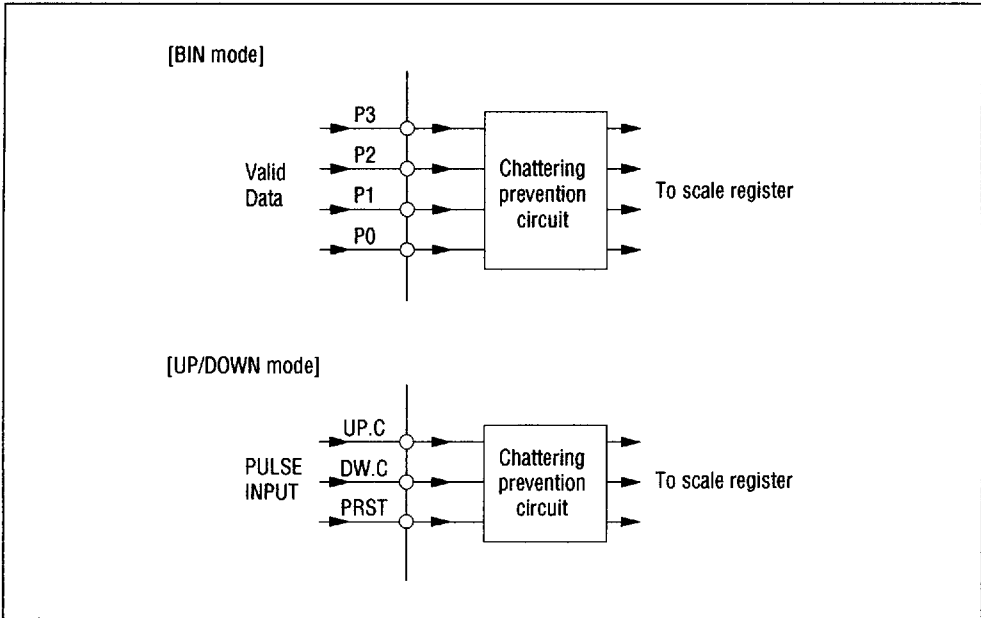
• **Pitch-control Circuit**

[BIN mode] (P3, P2, P1 and P0)

As shown in Fig. 4, this LSI has an internal 46ms chattering prevention circuit. P2 to P0 are internally terminated by over 10kΩ resistors.

16 pitch stages are provided however the 16th stage cannot be set.

[UP/DOWN mode] (UP.C, DW.C and PRST)

As shown in Fig. 4, this LSI has internal 46ms chattering prevention circuit.

Figure 4 Scale Control Circuit

A high input to the UP.C pin raises the scale by one stage, and inputting one pulse to the DW.C pin lowers the scale by one stage. One pulse input to the PRST pin sets the no scale conversion state (scale stage 8).

Since the scale stage change functions cycli-

cally, change from scale stage 0 to 16 or 16 to 0 occurs. The UP.C, DW.C and PRST pins are terminated by over 10kΩ resistors. The tone scale stage is undefined after power on. First of all, use the circuit at the state of changeless tone scale by using the PRST.

- **System Control Circuit**

[BIN mode] (STB/$\overline{ACT}$)

The STB/$\overline{ACT}$ signal is the power control signal not affecting the scale.

When the STB/$\overline{ACT}$ goes to the "H" level, any scale stage control signal input is ignored.

The DAO pin, however, outputs 1/2 AVDD if the STB/$\overline{ACT}$ is "H", or outputs the AGND irrelevant to the STB/$\overline{ACT}$ state if the PD is "H".

Since the oscillation circuit is instable for ten milliseconds after power on or the falling edge of the PD, it is recommended to set the STB/$\overline{ACT}$ to "H" in this period and make the STB/$\overline{ACT}$ fall after the stabilization of the oscillator to minimize abnormal output af-

ter power on or the fall of the PD.

Such an abnormal output, however, can hardly be distinguished from pop noise.

- **Oscillation circuit (XT and $\overline{XT}$)**

Since the feedback resistor and amplifier are provided internally, the oscillation circuit can be realized by connecting only a crystal or ceramic oscillator and oscillation stabilizing capacitors (C7 and C8) externally. It is recommended to use C7 = C8 = 30pF for Murata's ceramic oscillator CSA4.00MG, CST4.00MGW, 4.19 MHz OR 4.5MHz, or use C7 = C8 = 33pF for Kyocera's ceramic oscillator KBR-4.0MS.

Fig. 5 shows the circuit example. To use the external clock, input it to the XT pin and leave the $\overline{XT}$ pin open.
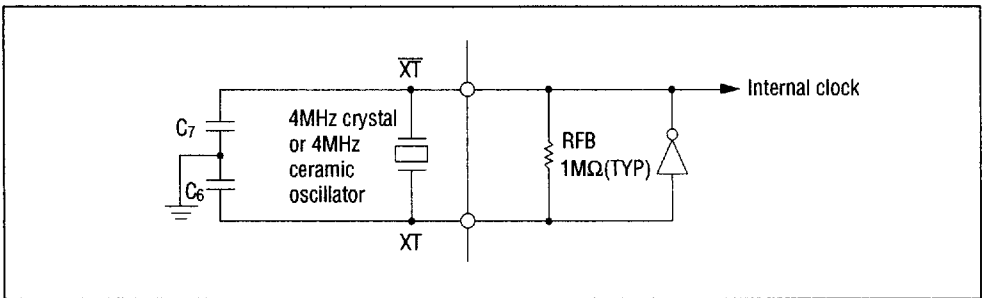

Figure 5 Oscillation Circuit

• **Power Supply Circuit (DVDD/DGND, AVDD and AGND)**

To prevent the power noise from entering the analog circuit, insert a capacitor of about 10μF each between AVDD and AGND and between DVDD and DGND to obtain a stable level without power noise.

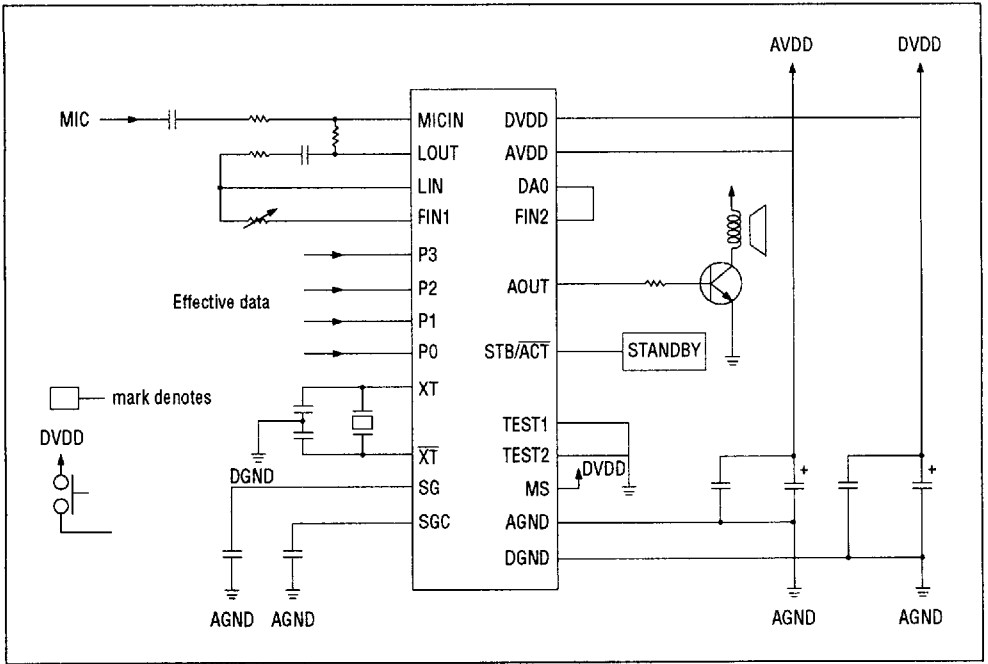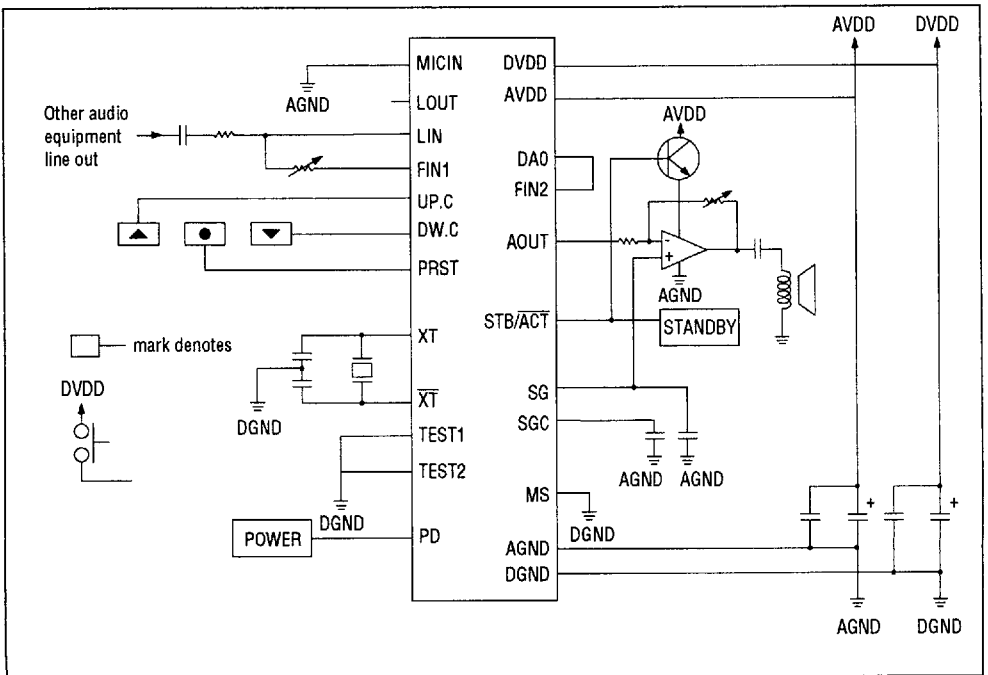Be sure that the capacity between AVDD and AGND equals the capacity between DVDD and DGND.

DVDD

DGND
AVDD

AGND
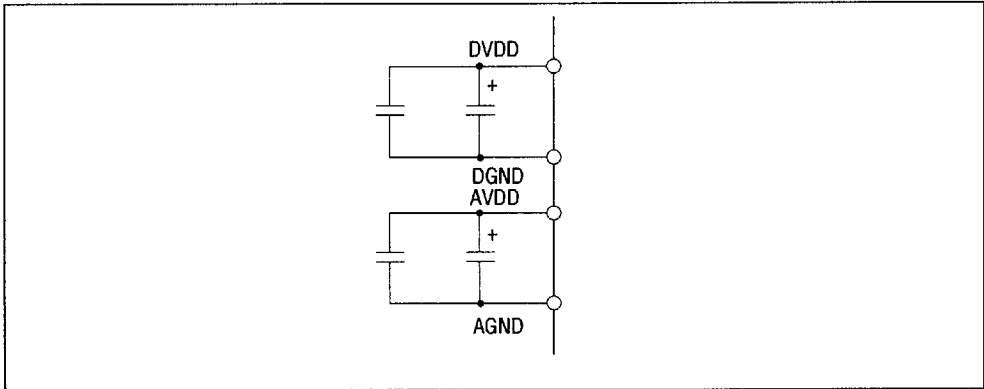
Note: The voltages of AVDD and DVDD should rise from 0V to 4V within 2ms when the power is risen.

Figure 6 Power Supply Circuit

APPLICATION CIRCUIT EXAMPLE 1 [BIN mode]

APPLICATION CIRCUIT EXAMPLE 2 [UP/DOWN mode]

Pitch Conversion Table

Scale and cutoff frequency

Scale stage	Remarks	DA sampling cycle (µS)/ frequency (kHz)	LPF cutoff frequency (kHz)	Interval of discontinuous point (ms)
16	One octave up	60/16.6	7.60	Approx 7.0
15	Major sixth up	71/14.0	7.60	Approx 10.0
14	Minor sixth up	76/13.1	5.70	Approx 12.0
13	Fifth up	80/12.5	5.70	Approx 15.0
12	Fourth up	90/11.1	5.70	Approx 22.0
11	Major third up	95/10.5	5.70	Approx 28.0
10	Minor third up	101/9.90	4.56	Approx 40.0
9	Minor second up	113/8.84	4.56	Approx 120.0
8	No change	120/8.33	3.80	—
7	Minor second down	127/7.87	3.80	Approx 110.0
6	Minor third down	143/6.99	3.26	Approx 45.0
5	Major third down	151/6.62	3.26	Approx 40.0
4	Fourth down	160/6.25	3.26	Approx 38.0
3	Fifth down	180/5.55	2.85	Approx 30.0
2	Minor sixth down	190/5.26	2.53	Approx 20.0
1	Major sixth down	202/4.95	2.53	Approx 20.0
0	Above one octave down	227/4.40	2.07	Approx 18.0