PHOTOCOUPLER

T-41-85

6N138, 6N139
GaAlAs INFRARED+ PHOTO-IC

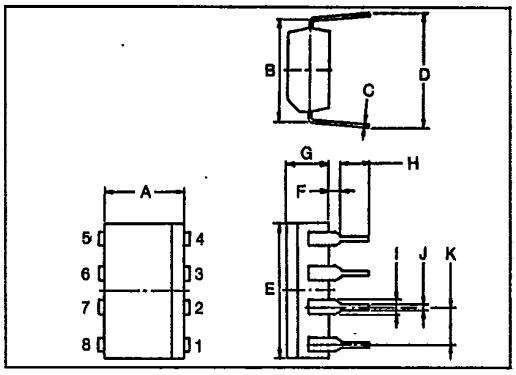
The 6N138 and 6N139 consist of a GaAlAs infrared emitting diode coupled with a split-Darlington output configuration. A high speed GaAlAs infrared manufactured with a unique LPE junction, has the virtue of fast rise and fall time at low drive current.

APPLICATIONS

- CURRENT LOOP DRIVER
- LOW INPUT CURRENT LINE RECEIVER
- CMOS LOGIC INTERFACE

FEATURES

- Isolation voltage: 2500V_{rms} (Min.)
- Current transfer ratio: 6N138 - 300% Min. (I_F=1.6mA)
  6N139 - 400% Min. (I_F=0.5mA)
- Switching time: 6N138 - t_{PHL}=10μs Max.
  - t_{PLH}=35μs Max.
  6N139 - t_{PHL}=1μs Max.
  - t_{PLH}=7μs Max.



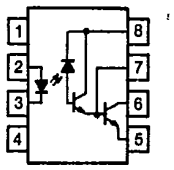
SYMBOL	INCHES	MM
A	0.252	6.4
B	0.300	7.62±0.25
C	0.010 $^{+0.004}_{-0.022}$	0.25 $^{+0.1}_{-0.05}$
D	0.309 ~ 0.346	7.85 ~ 8.80
E	0.380±0.010	9.66±0.25
F	0.031	0.8
G	0.144	3.65
H	0.100 MIN	2.5 MIN
I	0.047	1.2
J	0.020	0.5
K	0.100±0.010	2.54±0.25

MAXIMUM RATINGS (Ta=25°C)

	CHARACTERISTIC		SYMBOL	RATING	UNIT
A	Forward Current	(Note 1)	I_F	20	mA
	Pulse Forward Current		I_{FP}*1	40	mA
	Total Pulse Forward Current		I_{FP}*2	1	A
	Reverse Voltage		V_R	5	V
	Diode Power Dissipation	(Note 2)	P_D	35	mW
B	Output Current	(Note 3)	I_O	60	mA
	Emitter-Base Reverse Voltage		V_{EB}	0.5	V
	Supply Voltage		V_{CC}*3	-0.5~18	V
	Output Voltage		V_O*3	-0.5~18	V
	Output Power Dissipation	(Note 4)	P_O	100	mW
Operating Temperature Range			T_{opr}	-0~70	°C
Storage Temperature Range			T_{stg}	-55~125	°C
Lead Solder Temperature (10 sec.)		*4	T_{sold}	260	°C
Isolation Voltage (1 min., RH≦60%)			BV_S**	2500	V_{rms}
				3540	V_{dc}

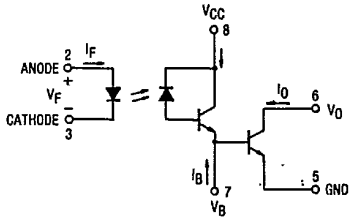
* JEDEC Registered Data.
** Not Registered JEDEC.
*1: 50% duty cycle, 1ms pulse width.
*2: Pulse width 1μs, 300pps.
*3: 6N138 ... -0.5 to 7V.
*4: 1.6mm below seating plane.
A - LED B - DETECTOR

PIN CONFIGURATION (TOP VIEW)



1. NC
2. ANODE
3. CATHODE
4. NC
5. GROUND
6. OUTPUT
7. OUTPUT BASE
8. V_{CC}

SCHEMATIC



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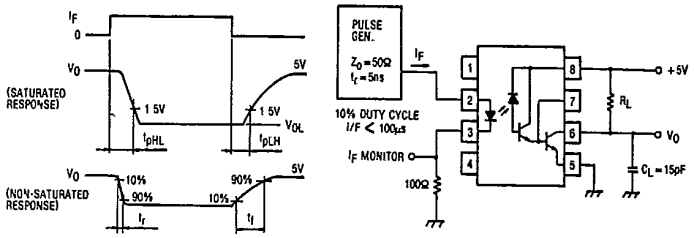
OPTO-ELECTRICAL CHARACTERISTICS OVER RECOMMENDED TEMPERATURE (Ta = 0°C~70°C Unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.*5	MAX.	UNIT
Current Transfer Ratio (Note 5, 6)	6N139	CTR*	I_F=0.5mA, V_O=0.4V, V_{CC}=4.5V	400	800	—	%
	6N138		I_F=1.6mA, V_O=0.4V, V_{CC}=4.5V	500	900	—	
				300	600	—	
Logic Low Output Voltage (Note 6)	6N139	V_{OL}	I_F=1.6mA, I_O=6.4mA, V_{CC}=4.5V	—	0.1	0.4	V
			I_F=5mA, I_O=15mA, V_{CC}=4.5V	—	0.1	0.4	
			I_F=12mA, I_O=24mA, V_{CC}=4.5V	—	0.2	0.4	
	6N138		I_F=1.6mA, I_O=4.8mA, V_{CC}=4.5V	—	0.1	0.4	
Logic High Output Current (Note 6)	6N139	I_{OH}*	I_F=0mA, V_O=V_{CC}=18V	—	0.05	100	μA
	6N138		I_F=0mA, V_O=V_{CC}=7V	—	0.05	250	
Logic Low Supply Current (Note 6)		I_{CCL}	I_F=1.6mA, V_O=Open, V_{CC}=5V	—	0.2	—	mA
Logic High Supply Current (Note 6)		I_{CCH}	I_F=0mA, V_O=Open, V_{CC}=5V	—	10	—	nA
Input Forward Voltage		V_F*	I_F=1.6mA, Ta=25°C	—	1.65	1.7	V
Input Reverse Breakdown Voltage		BV_R*	I_R=10μA, Ta=25°C	5	—	—	V
Temperature Coefficient of Forward Voltage		$\frac{\Delta V_F}{\Delta T_a}$	I_F=1.6mA	—	-1.9	—	mV/°C
Input Capacitance		C_{IN}	f=1MHz, V_F=0	—	60	—	pF
Input-Output Isolation Leakage Current		I_{I-O}*	45% Relative Humidity, t=5s, V_{I-O}=3000Vdc, Ta=25°C (Note 7)	—	—	1.0	μA
Resistance (Input-Output)		R_{I-O}	V_{I-O}=500Vdc (Note 7)	—	10^{12}	—	Ω
Capacitance (Input-Output)		C_{I-O}	f=1MHz (Note 7)	—	0.6	—	pF

** JEDEC Registered Data.
*5 All typicals at Ta=25°C and V_{CC}=5V, Unless otherwise noted..

TEST CIRCUIT 1.



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SWITCHING CHARACTERISTICS (Ta = 25°C, V_{CC} = 5V, Unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time to Logic Low at Output (Note 6, 8)	6N139	t_{pHL}*	1	I_F=0.5mA, R_L=4.7kΩ	—	5	25.0	μs
				I_F=12mA, R_L=270Ω	—	0.2	1	μs
	6N138			I_F=1.6mA, R_L=2.2kΩ	—	1	10	μs
Propagation Delay Time to Logic High at Output (Note 6, 8)	6N139	t_{pLH}*	1	I_F=0.5mA, R_L=4.7kΩ	—	5	60	μs
				I_F=12mA, R_L=270Ω	—	1	7	μs
	6N138			I_F=1.6mA, R_L=2.2kΩ	—	4	35	μs
Common Mode Transient Immunity at Logic High Level Output (Note 9)		CM_H	2	I_F=0mA, R_L=2.2kΩ V_{CM}=400Vp-p	—	500	—	V/μs
Common Mode Transient Immunity at Logic Low Level Output (Note 9)		CM_L	2	I_F=1.6mA, R_L=2.2kΩ V_{CM}=400Vp-p	—	-500	—	V/μs

* JEDEC Registered Data.

Note 1: Derate linearly above 50°C free-air temperature at a rate of 0.4mA/°C.

Note 2: Derate linearly above 50°C free-air temperature at a rate of 0.7mW/°C.

Note 3: Derate linearly above 25°C free-air temperature at a rate of 0.7mW/°C.

Note 4: Derate linearly above 25°C free-air temperature at a rate of 2.0mW/°C.

Note 5: DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.

Note 6: Pin 7 Open.

Note 7: Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7 and 8 shorted together.

Note 8: Use of a resistor between pin 5 and 7 will decrease gain and delay time.

Note 9: Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O>2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O<0.8V).

TEST CIRCUIT 2.