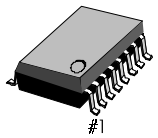
INTRODUCTION

16-SOP-225



The S1T8531 is a wideband FM / FSK receiver designed for wideband FSK data and analog FM applications.
It is fabricated using Samsung's ASP5HB 0.5um advanced BiCMOS process. The S1T8531 contains high gain IF amplifier with received signal strength indicator (RSSI), a wideband FM quadrature demodulator, a baseband filter amplifier and a high speed data slicer with sample & hold function.
The IF amplifier has 100dB small signal gain and 2MHz through 40MHz bandwidth. The wideband FM quadrature demodulator has demodulation bandwidth greater than 1MHz.
The baseband filter amplifier is a wideband buffer and it can be configured as a second-order sallen-key low pass filter. The data slicer is a comparator that is designed to square up the data signal with data rates up to 2Mbps.

FEATURES

- Operating voltage range : 2.2 to 5.5V
- Typical supply current : 5.5mA at 3.6V
- Operating frequency range : 2MHz to 40MHz
- High Gain (100dB) and Wideband (2MHz to 40MHz) IF Amplifier
- Quadrature Demodulator with Greater than 1MHz Bandwidth
- High Speed Data Slicer Operating Upto 2Mbps with Sample & Hold
- RSSI Dynmic range : Typ : 60dB

APPLICATION

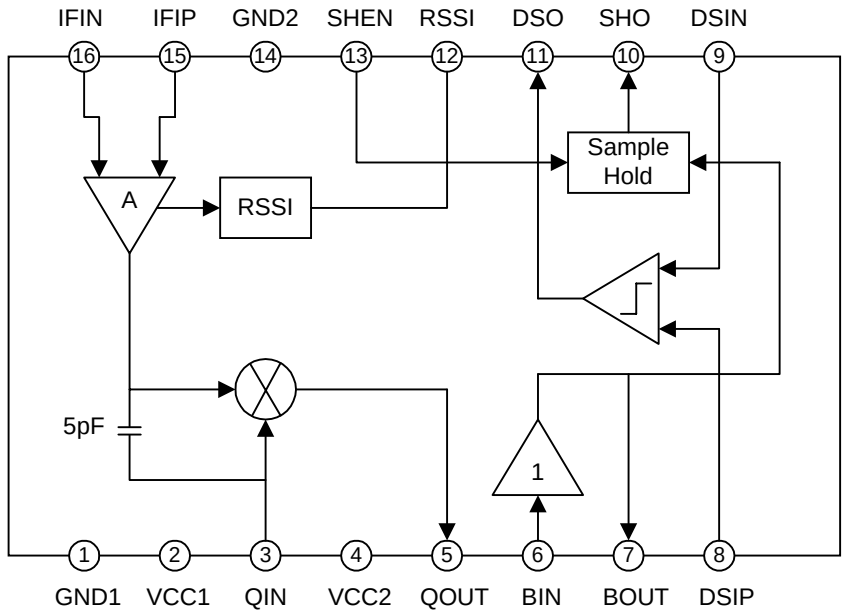
- Wideband FM / FSK Wireless Communication Systems

ORDERING INFORMATION

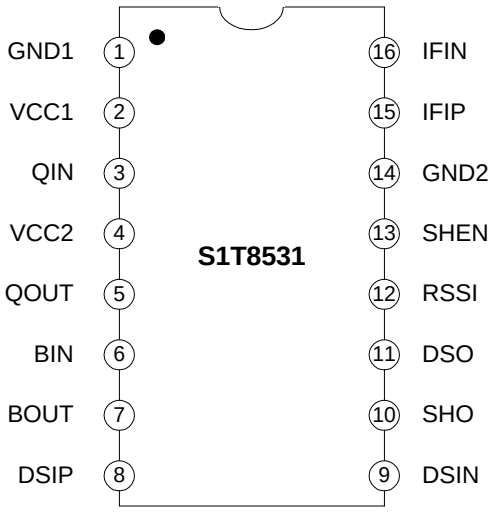
Device	Package	Operating Temperature
+S1T8531X01-S0B0	16-SOP-225	- 10°C to + 70°C

+ : New Product

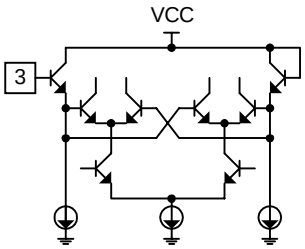
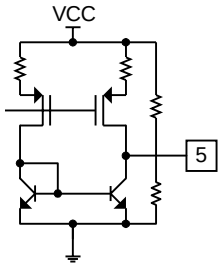
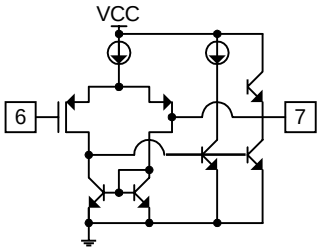
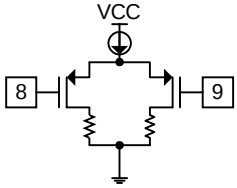
BLOCK DIAGRAM



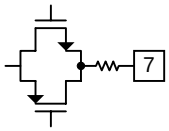
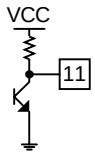
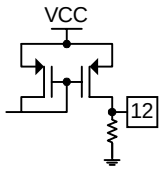
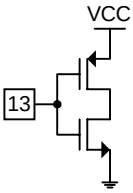
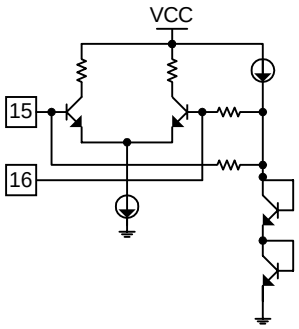
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Schematic	Description
1	GND1		Ground. (Pin1 and Pin14 are connected internally)
2	VCC1		Supply. (Pin2 and Pin4 are connected internally)
3	QIN		Quadrature demodulator tank input.
4	VCC2		Supply. (Pin2 and Pin4 are connected internally)
5	QOUT		Quadrature demodulator output.
6 7	BIN BOUT		Baseband filter buffer amplifier input. Baseband filter buffer amplifier output.
8 9	DSIP DSIN		Data slicer positive input. Data slicer negative input.

PIN DESCRIPTION (Continued)

Pin	Name	Schematic	Description
10	SHO		Sample and hold output.
11	DSO		Data slicer output.
12	RSSI		RSSI output.
13	SHEN		Sample and hold enable input. High signal input enable sample and hold function and low signal input disable sample and hold function .
14	GND2		Ground. (Pin1 and Pin14 are connected internally)
15 16	IFIP IFIN		IF amplifier differential inputs. DC blocking is required.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Maximum Supply Voltage	V_{CC}	6	V
Operating temperature	T_a	-10 to + 70	°C
Storage Temperature	T_{STG}	-55 to + 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	2.2 to 5.5	V
Voltage applied to any pin	V_{IN}	- 0.3 to Vcc + 5.5	V

ELECTRICAL CHARACTERISTICS

(Vcc = 3.6V, IF = 10.7MHz, fdev = ± 75kHz, fmod = 10kHz,Ta = 25°C, IFin = -47dBm unless otherwise noted.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption	Icc	-	-	5.5	7.0	mA
IF Input Frequency	IFfreq	-	2	10.7	40	MHz
20dB SINAD Sensitivity (Note 2)	VSEN	-	-	-95	-81	dBm
IF Amplifire Bandwidth (Note 1)	BWIF	-	2	-	40	MHz
IF Amplifier Voltage Gain (Note 1)	ΔG IF	-	95	101	-	dB
IF Amplifier Input Impedance (Note 1)	RII_{IF}	-	-	1.5	-	kΩ
Quadrature Demodulator Output Voltage	Vo(DEM)	-	100	150	200	mVrms
Demodulator Bandwidth (Notes 1 and 2)	BWDEM	-	0.6	1	-	MHz
Baseband Filter Buffer Amplifier Bandwidth	BWAMP	-	1	2	-	MHz
Baseband Filter Buffer Amplifier Voltage Gain	DG AMP	-	-3	0	+3	dB
Data Slicer Maximum Operating Frequency (Notes 1 and 2)	BWDS	-	1	2	-	Mbps
RSSI Dynamic Range	RSSI	-	50	60	-	dB
RSSI Output Level	Vo(RSSI)	-	0.5	-	2.0	V

NOTES:

1. Not 100% AC tested but guaranteed by design and characterization.
2. Measured result on evaluation board with proper impedance matching.

FUNCTIONAL DESCRIPTION

General

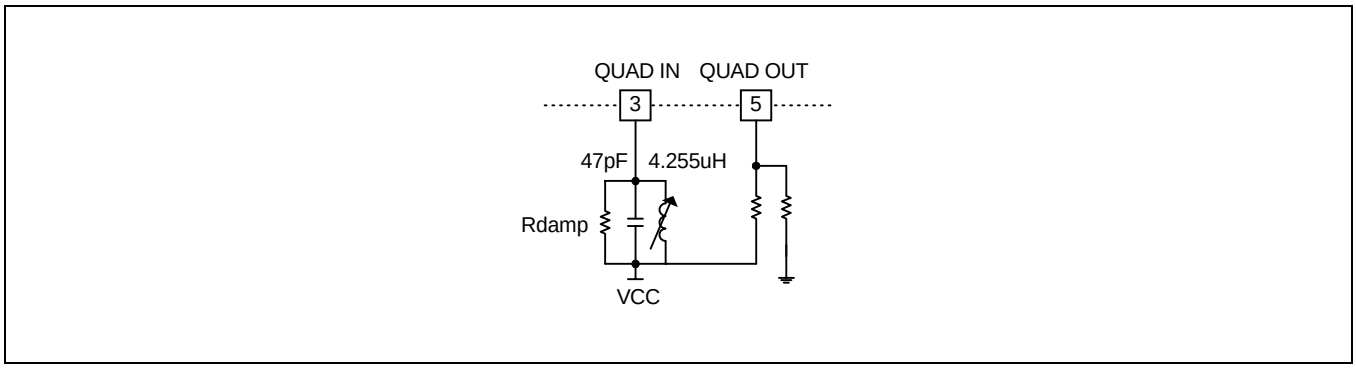
The S1T8531 is a wideband FM / FSK receiver designed for use in analog FM and digital FSK systems such as 900MHz / 2.4GHz ISM band analog / digital cordless phones and wideband data links with data rates up to 2Mbps. It contains IF amplifier, quadrature detector, baseband filter amplifier and data slicer with sample and hold function.

IF Amplifier

The IF amplifier section is composed of seven differential stage with total gain of 100dB at 10.7MHz. The input impedance at 10.7MHz is 1.5kΩ. For 10.7MHz ceramic filter applications, an external 430Ω resistor must be placed between IFP(Pin15) and IFN(pin16) to provide the equivalent load impedance of 330Ω that is required by the filter.

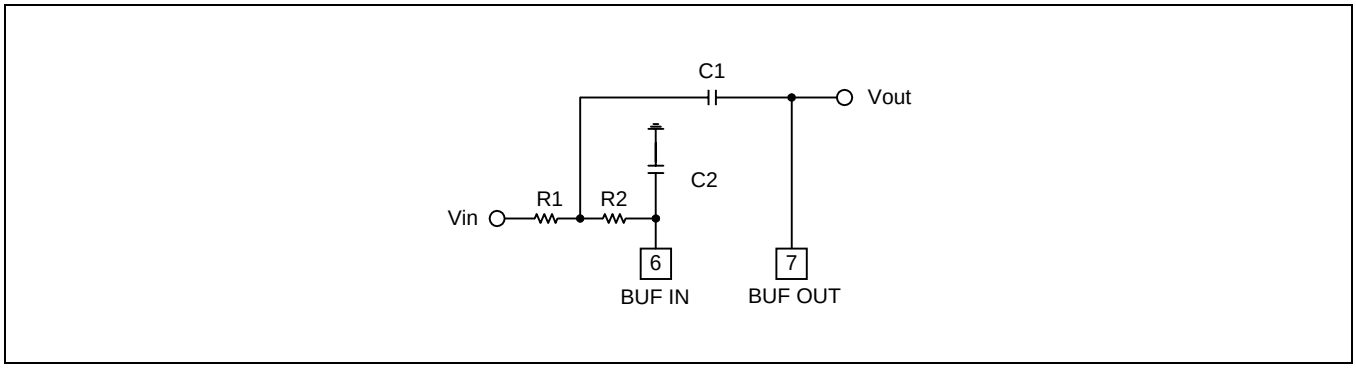
Quadrature Demodulator

The quadrature demodulator requires tank circuit with loaded Q depending on detection bandwidth. Following figure shows external components required for 10.7MHz operation.



Baseband Filter Buffer Amplifier3

Baseband filter amplifier is a wideband buffer and it can be configured as a second-order sallen-key low pass filter. Following figure shows the external components required.
Cutoff frequency = 1 / [2π*SQRT(R1R2C1C2)]
Quality factor = SQRT(R1R2C1C2) / (R1C2 + R2C2)
The component value of R1 should contain the quadrature detector output resistance.



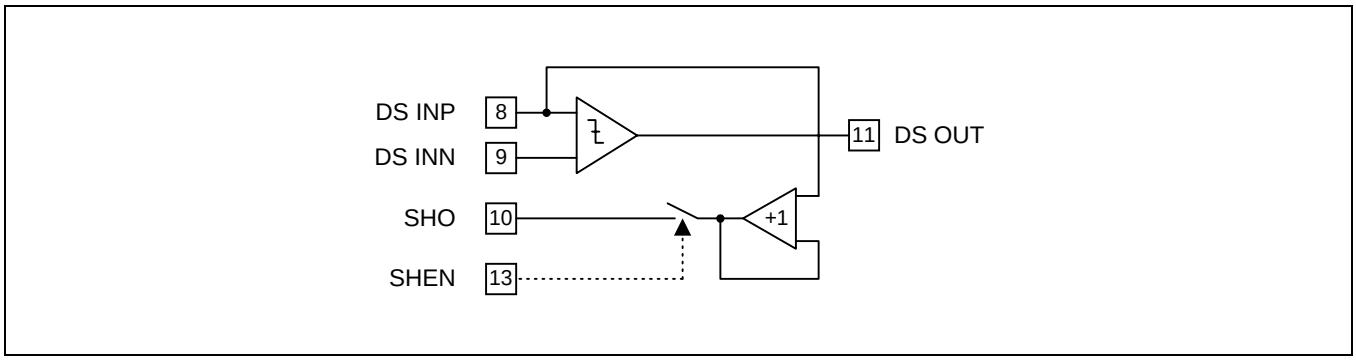
Data Slicer with Sample and Hold

The data slicer is a comparator that is designed to square up the data signal. The recovered data signal from the baseband filter output can be DC coupled to the data slicer DS-INP(Pin 9). The S1T8531's data slicer incorporates an sample and hold used to derive the data slicer reference voltage by means of an external integration circuit. The sample and hold is "ON" during reception of the preamble data pattern, and is otherwise "OFF" in TDD (Time Division Duplex) system. The external integration circuit is formed by an RC low pass circuit placed between SHO (Pin 10) and ground.

The size of this resistor and capacitor and the nature of the data signal determine how faithfully the data slicer shapes up the recovered signal. The time constant is short for large peak to peak voltage swings or when there is a change in DC level at the detector output. For small signal or for continuous bits of the same polarity which drift close to the threshold voltage, the time constant is longer.

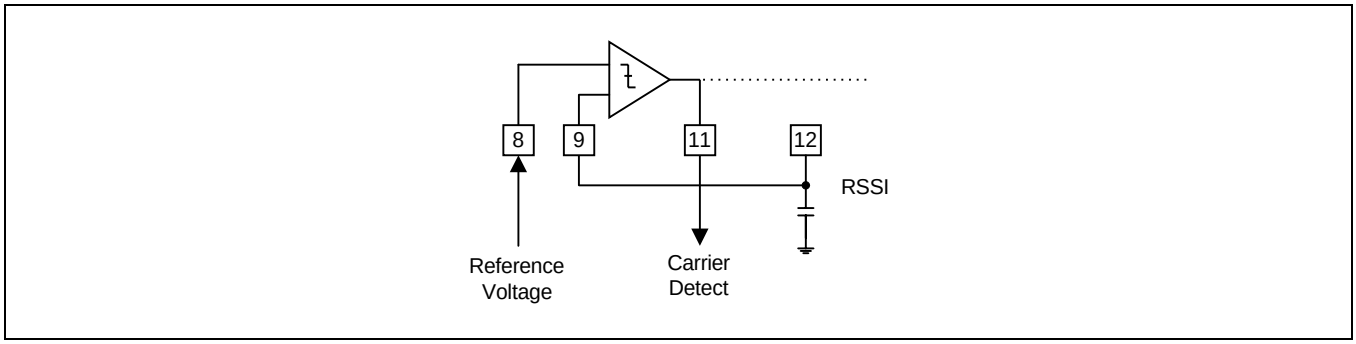
'The sample and hold is able to sink/source 3mA to/from the external integration circuit in order to minimize the settling time. When the sample and hold is "OFF" the output (SHO) is in high impedance state with extremely low leakage current.

'Following figure shows the internal block diagram.

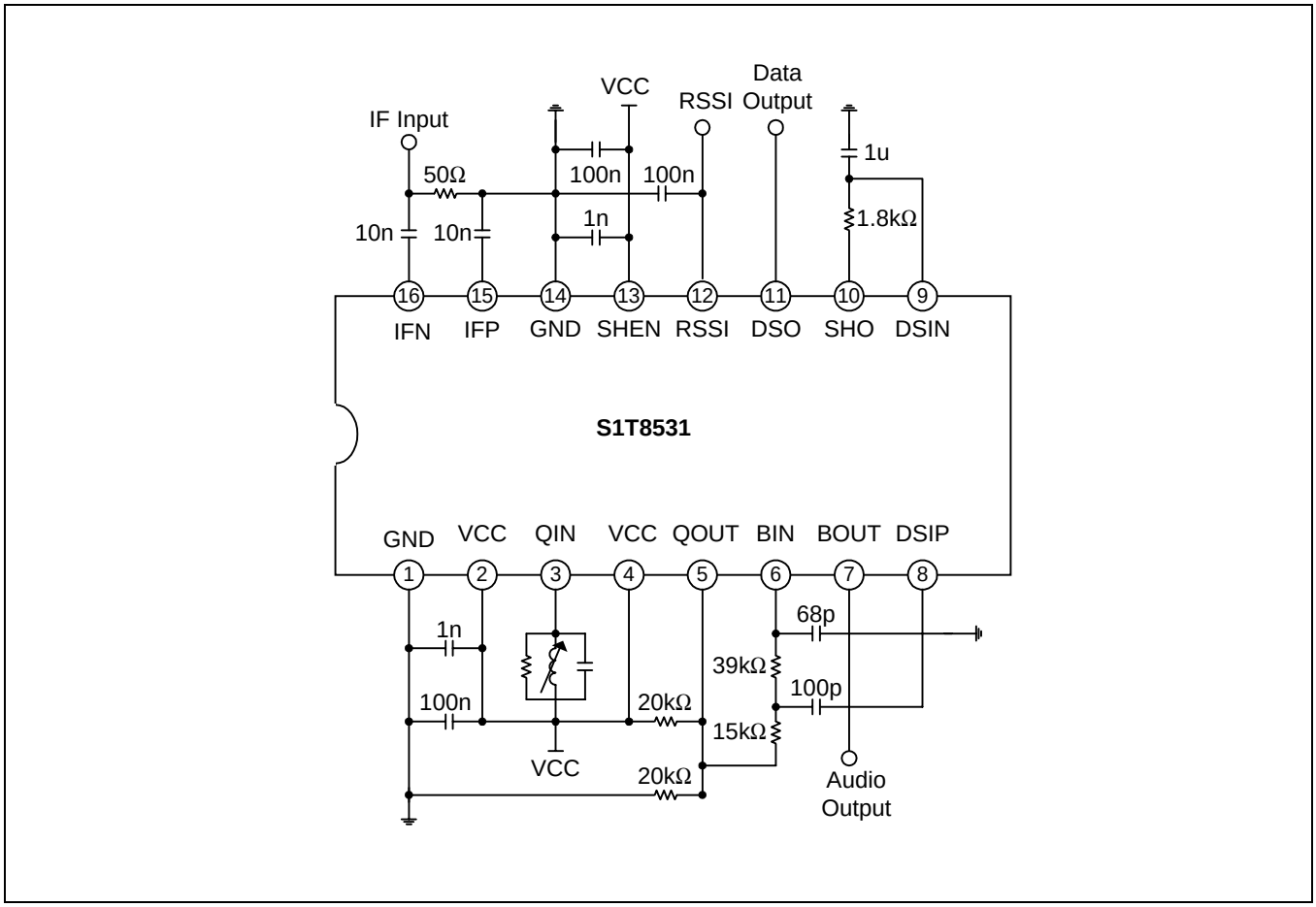


The output of the data slicer (DS-OUT) is a CMOS compatible bitstream. However, it is recommeded that an external NPN amplifier stage be used to drive the CMOS baseband processor, in order to minimize the amount of ground and supply currents in the S1T8531 which might desensitize the chip.

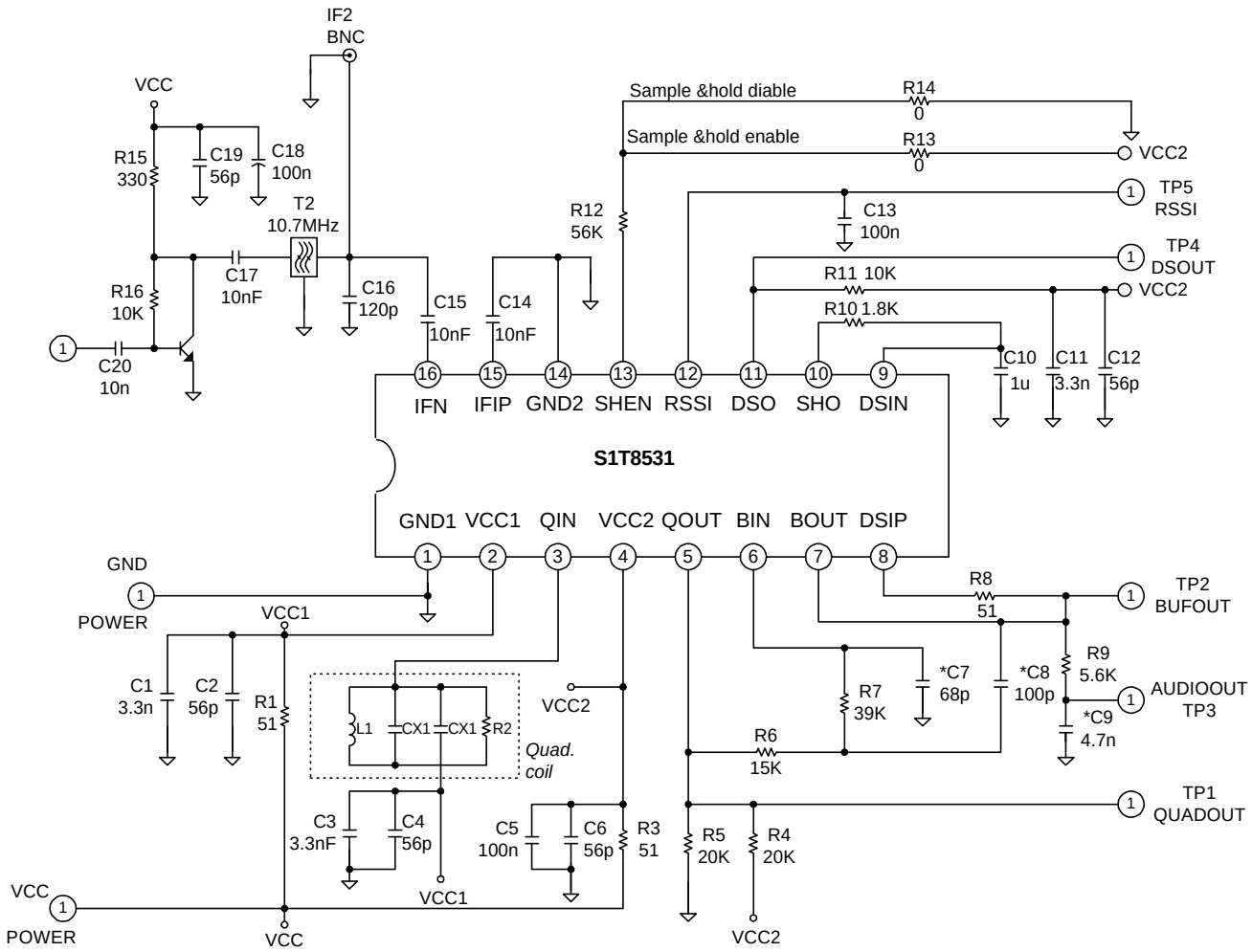
The data slicer can be used as a carrier detector also. Following figure shows application example. In this case, sample and hold should be off.



TEST CIRCUIT



APPLICATION CIRCOUT



* Changable value for each application

	C7	C8	C9
Analog	68p	100p	4.7n
Digital	100p	220p	820p

* Quadrature Coil

	L1	CX1	CV1	R2
Quad. coil	360u	120p	N/A	7.5K
Ext. coil	2.7u	56p	1-3p	2.4K