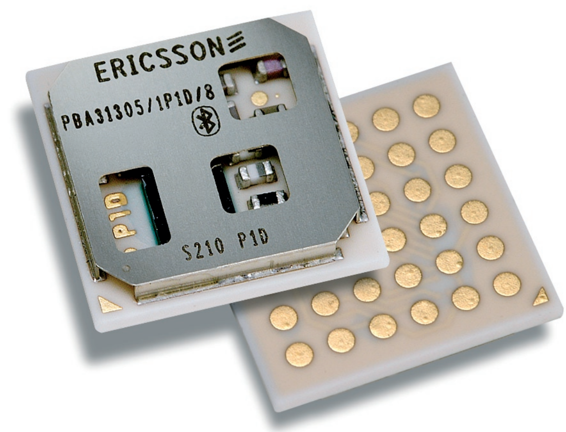
Bluetooth™ Radio

Key features

- A small cost effective class 2 Bluetooth radio
- Forms a complete radio with only an antenna and a reference frequency
- Very high out-band blocking in all GSM bands
- Excellent high signal level performance in-band
- Small LGA package (8.8×8.8×1.6 mm)
- Prequalified for Bluetooth specification 1.1
- Requires no external shielding



Description

The Bluetooth Radio PBA 313 05 from Ericsson Microelectronics is a short-range microwave frequency radio transceiver for Bluetooth communication links. Provided in a compact LGA package. No external shield is required.
The Bluetooth Radio offers a combination of compact size, low power consumption, and cost effective assembly. The PBA 313 05 forms a complete radio with only the addition of an antenna, a 13 MHz reference frequency crystal, and a digital control functionality. As a result, designers can benefit from a pre-tested and ready-to-use device, providing a robust Bluetooth Radio function in the final OEM application.
PBA 313 05 is built around an RFCMOS ASIC. Antenna filter, RX and TX baluns are all integrated into the circuit. The antenna filter is specially designed for application in GSM environment such as inside a mobile phone. The Radio PBA 313 05 also has a very high threshold for high signal levels in-band, which makes it very suitable to be in an IEEE 802.11b environment. Operating from a 2.6 V supply, the module has a typical supply current consumption of only 50 mA (receive mode) or 60 mA (transmit mode), thus helping to extend battery life for portable equipment. Standby mode provides further power savings.

Suggested applications

- Mobile phones
- PDA
- Modems
- Laptop computers
- Handheld equipment

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Block diagram

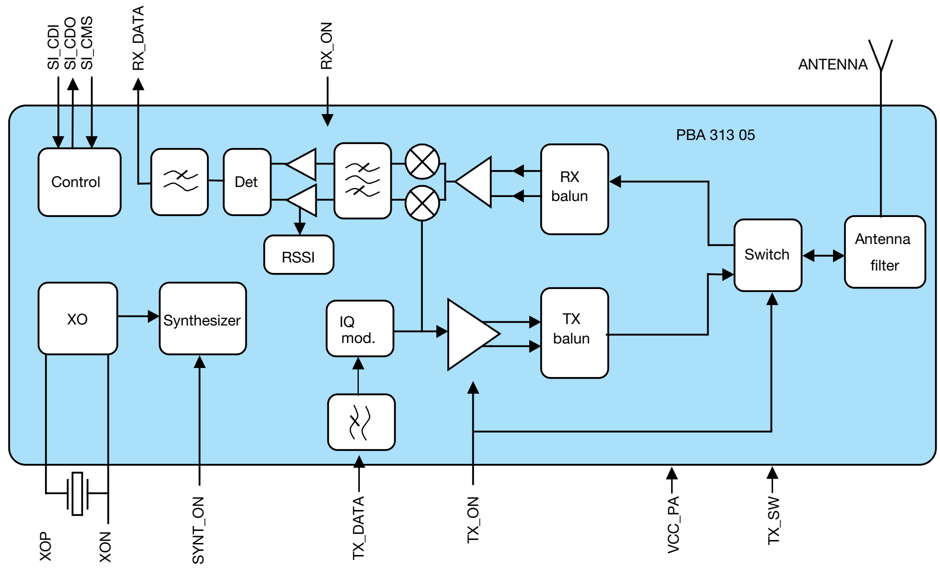


Figure 1. Block diagram.

Absolute maximum ratings

Parameter		Symbol	Min	Typ	Max	Unit
Temperature						
Storage temperature			-40		+100	°C
Operating temperature			-20		+75	°C
Power Supply						
Supply voltage			2.5		2.75	V
Applied voltage of non-supply pins			-0.2		3.3	V
Applied voltage of XO_P			-0.2		2.75	V
Applied voltage of XO_N			-0.2		2.75	V
Input RF power	- In-band				15	dBm
	- Out of band				15	dBm

Electrical characteristics

Unless otherwise noted, the specification applies for $T_{amb} = 25°C$, $V_{DD} = 2.6$ V, $f_{ref} = 13$ MHz ± 10 ppm, $V_{ppref} = 0.8$, VSWR ≤ 2:1

Operating Conditions

Parameter			Min	Typ	Max	Unit
Frequency range			2.400		2.480	GHz
Reference clock frequency (f_{EXT_CLK})			12.99974	13.00000	13.00026	MHz
Reference clock amplitude			0.200		2.0	V_{PP}
Reference clock phase noise	Δf=2.5kHz				-100	dBc/
Hz		Δf ≥ 15kHz				-110
dBc/Hz						
Supply voltage (V_{DD})			2.5		2.75	V
Applied voltage of non-supply pins			0.2		3.3	V
Output matching of ANT pin (VSWR)					2:1	
Logical high input			$0.7*V_{DD}$		3.3	V
Logical low input			-0.2		$0.3*V_{DD}$	V
Rise/fall time of all digital inputs					4	ns
Clock frequency of SI_CLK					4	MHz
Positive period of SI_CLK			76			ns
Ambient temperature (T_{Amb})			-20	+25	+75	°C

DC specifications

Parameter		Min	Typ	Max	Unit
Power Supply					
Supply Current	- Sleep mode [1]		70	TBD	µA
	- Synt mode		35	TBD	mA
	- Transmit mode		60	TBD	mA
	- Receive mode		50	TBD	mA
Capacitance of digital inputs			10		pF
XO_N input capacitance			3		pF
XO_P input capacitance			3		pF
Input leakage current			5		µA
Rise/fall time of all digital outputs [2]			40		ns
Logical high output			V_{DD}		V
Logical low output			0		V
SYS_CLK frequency			13		MHz
TX_CLK frequency			1		MHz
LPO_CLK frequency		3.1992	3.2	3.2008	kHz

1) Average current the first second after shut down.
2) Driving a 10 pF load.

RF specifications

All parameters are guaranteed when measured according to the Bluetooth test specification.

Parameter		Min	Typ	Max	Unit
Receiver performance, BER = 0.1 %,					
Sensitivity level			-80	-75	dBm
Max input level		5	15		dBm
RSSI value	$P_{in} \geq$ -40 dBm	39	43	47	
	$P_{in} \leq$ -60 dBm	16	20	24	
Co-Channel interference, $C/I_{co\text{-}channel}$ [3]				11	dB
Adjacent (1 MHz) interference, C/I_{1MHz} [3]				0	dB
Adjacent (2 MHz) interference, C/I_{2MHz}				-30	dB
Adjacent (3 MHz) interference, $C/I_{\geq 3MHz}$				-40	dB
Image frequency (-4 MHz) interference, C/I_{image}				-9	dB
Adjacent (1 MHz) interference to inband image frequency, $C/I_{image\pm 1MHz}$				-20	dB
Out-of-band blocking	30-880 MHz [4]	4	TBD		dBm
	880-1785 MHz [4]	5			dBm
	1785-1910 MHz [4]	4			dBm
	1910-1980 MHz [4]	3			dBm
	1980-2000 MHz [4]	-10			dBm
	2000-2004 MHz [4]	-27			
	2497-3000 MHz [4]	-27			
	3000-12750 MHz [4]	-10			dBm
Intermodulation rejection [5]		-32	TBD		dBm
Spurious Emissions	30 MHz – 1 GHz			-57	dBm
	1 GHz – 12.75 GHz			-47	dBm

RF specifications continued.

Parameter		Min	Typ	Max	Unit
Transmitter Performance					
Output power		-2		4	dBm
Frequency deviation[6)]		140	159	175	kHz
Initial frequency error		-48	0	48	kHz
TX carrier drift	1 slot	-25		25	kHz
	3 slots	-40		40	kHz
	5 slots	-40		40	kHz
	idle	-40		40	kHz
Drift rate		-20		20	kHz/50µs
20 dB-bandwidth with peak detector				1000	kHz
Adjacent channel power	±2 MHz			-20	dBm
	±3 MHz			-40	dBm
	±4 MHz			-40	dBm
	±13 MHz			-40	dBm
Spurious emission	30 MHz – 1 GHz			-36	dBm
	1 GHz – 12.75 GHz			-30	dBm
	1.8 GHz – 1.9 GHz			-47	dBm
	5.15 GHz – 5.3 GHz			-47	dBm

3) Carrier signal level of -60 dBm, interferer Bluetooth modulated.

4) Carrier signal at 2460 MHz with a level of -67 dBm , Continuous Wave (CW) interferer.

5) Carrier: -64 dBm @ 2441 MHz, 1st interferer: CW @ 2446 MHz, 2nd interferer: BT mod. @ 2451 MHz.

6) Measured differentially.

Pin	x	y	Pin	x	y	Pin	x	y
A1	-3.175	3.175	**C1**	-3.175	0.635	**E1**	-3.175	-1.905
A2	-1.905	3.175	**C2**	-1.905	0.635	**E2**	-1.905	-1.905
A3	-0.635	3.175	**C3**	-0.635	0.635	**E3**	-0.635	-1.905
A4	0.635	3.175	**C4**	0.635	0.635	**E4**	0.635	-1.905
A5	1.905	3.175	**C5**	1.905	0.635	**E5**	1.905	-1.905
A6	3.175	3.175	**C6**	3.175	0.635	**E6**	3.175	-1.905
B1	-3.175	1.905	**D1**	-3.175	-0.635	**F1**	-3.175	-3.175
B2	-1.905	1.905	**D2**	-1.905	-0.635	**F2**	-1.905	-3.175
B3	-0.635	1.905	**D3**	-0.635	-0.635	**F3**	-0.635	-3.175
B4	0.635	1.905	**D4**	0.635	-0.635	**F4**	0.635	-3.175
B5	1.905	1.905	**D5**	1.905	-0.635	**F5**	1.905	-3.175
B6	3.175	1.905	**D6**	3.175	-0.635	**F6**	3.175	-3.175

Table 1.Pad Recommended pad co-ordinates for module PBA 313 05.

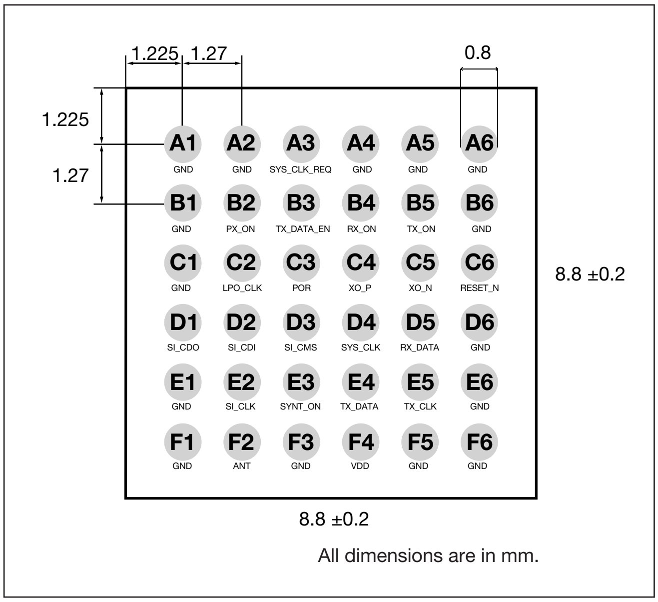


Figure 2. Pin numbering LGA.

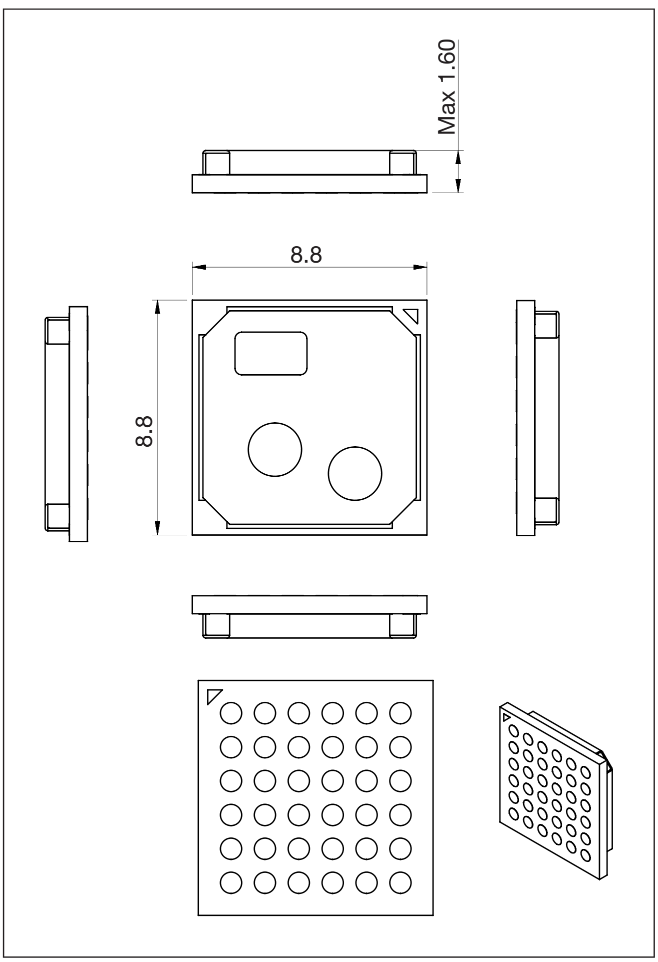


Figure 3. Mechanical dimensions and footprint.

Pin description

Pin No.	Pin name	Type	Description
A1	GND	Ground	Common ground
A2	GND	Ground	Common ground
A3	SYS_CLK_REQ	D in	System clock request
A4	GND	Ground	Common ground
A5	GND	Ground	Common ground
A6	GND	Ground	Common ground
B1	GND	Ground	Common ground
B2	PX_ON	D in	Packet on
B3	TX_DATA_EN	D in	Transmit data enable
B4	RX_ON	D in	Receiver power on
B5	TX_ON	D in	Transmit power on
B6	GND	Ground	Common ground
C1	GND	Ground	Common ground
C2	LPO_CLK	D out	3.2 kHz clock
C3	POR	D out	Power on reset output
C4	XO_P	A in	Crystal positive input
C5	XO_N	A in	Crystal negative input or external clock input
C6	RESET_N	D in	External power on reset input
D1	SI_CDO	D out	Serial data output
D2	SI_CDI	D in	Serial data input
D3	SI_CMS	D in	Serial interface control
D4	SYS_CLK	D out	System clock 13 MHz
D5	RX_DATA	D out	Received data output
D6	GND	Ground	Common ground
E1	GND	Ground	Common ground
E2	SI_CLK	D in	Serial interface clock
E3	SYNT_ON	D in	Synthesizer power on
E4	TX_DATA	D in	Transmit data
E5	TX_CLK	D out	1 MHz clock
E6	GND	Ground	Common ground
F1	GND	Ground	Common ground
F2	ANT	50 Ω	Antenna input/output
F3	GND	Ground	Common ground
F4	VDD	Power	Common power supply
F5	GND	Ground	Common ground
F6	GND	Ground	Common ground

Table 2. Short description of the PBA 313 05 pin-out. In the Type-column "A" denotes Analog bipolar and "D" Digital CMOS.

Functional description

Overview of radio functionality

PBA 313 05 is a radio module requiring minimal external components. The receiver has a heterodyne architecture with low IF. The transmitter utilises an IQ modulation architecture. The block diagram of PBA 313 05 is shown in figure 4.

Radio ASIC

The receiver consists of a LNA followed by I and Q mixers. The I and Q IF signals of these mixers are fed to an image rejecting selectivity filter. The filter is followed by two limiters (I and Q) fixing the amplitude of the received signal to the required level for the demodulator. The limiters generate an RSSI signal, which is converted to a digital word and is available through the serial interface. The demodulator is an IQ quadrature demodulator. A post detection filter and a slicer, which will output the received data to the baseband processor, follow the demodulator.

The local oscillator is an integrated VCO. The VCO frequency is controlled by means of a phase locked loop. The same VCO is used when receiving and transmitting.

The transmitter utilises IQ modulation. The bit stream from the base band radio is digitally processed to generate gaussian shaped I & Q output. A DAC and reconstruction filter is used to generate the IF input to the mixer. The RF input to the mixer comes from the phase locked VCO via phase shifters and buffering. The mixer output is fed to the PA-driver, which will deliver a nominal 0 dBm output power at the antenna.

There are a number of other circuit blocks such as the crystal oscillator, low power oscillator, power on reset circuit, control logic and the serial interface.

Loop filter

Generates the tuning voltage for the VCO.

RX balun

Transformation from unbalanced (single-ended) to balanced (differential) transmission. The balun is integrated in the substrate.

TX balun

Transformation from balanced to unbalanced transmission. The balun is integrated in the substrate.

Antenna switch

Directs the power either from the antenna filter to the receive ports or from the external PA output ports to the antenna filter.

Antenna filter

Front end bandpass filter fully integrated in the ceramic substrate.

I/O Signal Description

Power supply

There is one supply connection, VDD. It's important that this supply is properly decoupled and free from noise and other disturbances.

Oscillator or external clock input (No external load capacitors are required)

XO_N and XO_P connect to the crystal's inputs. The load capacitance to the crystal can be trimmed using the XO-Trim register. If an external clock is used, it should be AC coupled into the XO_N input and the XO_P input shall be left unconnected.

Ground

Ground should be distributed with very low impedance as a ground plane. Connect all GND connections to the ground plane. It is good to have a ground plane underneath the Bluetooth radio in order to shield the module from

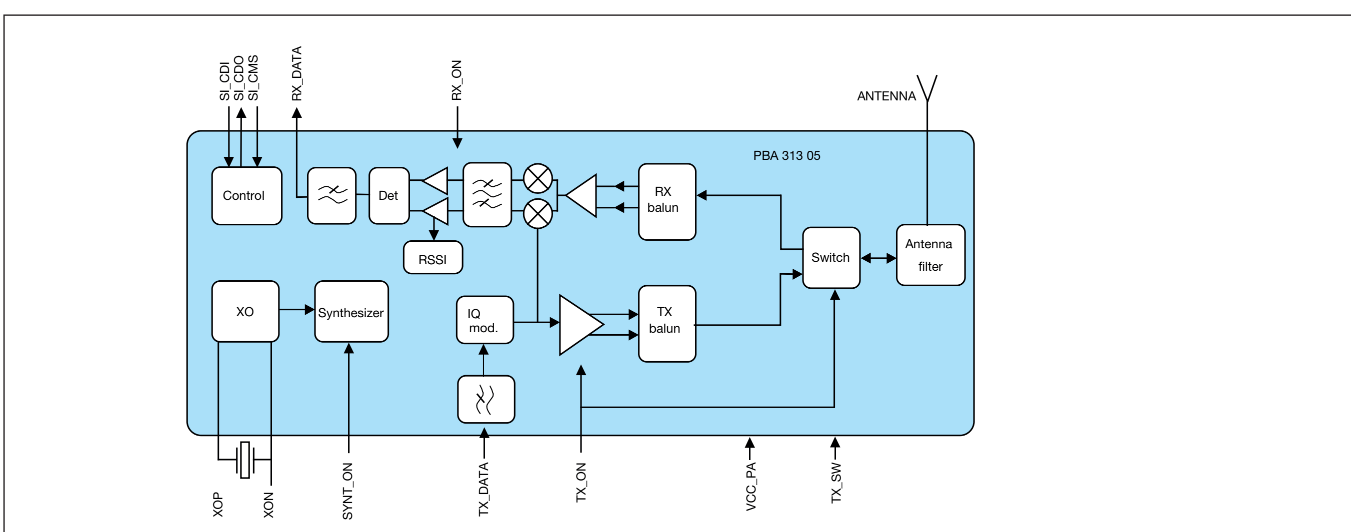


Figure 4. PBA 313 05 block diagram

any electrical noise. The purpose of the ground vias is to connect the local ground plane to the main ground layer. The Bluetooth radio will be self shielding and no additional shields should be necessary for normal operating conditions.

Antenna

The ANT pin should be connected to a 50 Ω antenna interface, thereby supporting the best signal strength performance. Ericsson Microelectronics partners can support application specific antennas.

Input control

There are five digital inputs available for the radio controlling features of the PBA 313 05. The Bluetooth timing requirements for these are described in table 3 and figure 5. In addition, there is a digital input signal for hardware reset of the radio, and a digital input signal for waking up the clock circuitry after a sleep mode period.

Symbol	Parameter	Min	Typical	Max	Unit
t_S	One Slot time			625	µs
t_S	Two Slot times			1875	µs
t_S	Three Slot times			3125	µs
t_{TO}	Transmitter On delay		102		µs
t_{TD}	Delay before transmitting data	203	213 104	223	µs
t_{EN}	Transmit data enable delay after t_{TO}				µs
t_D	Data sending period, one slot			366	µs
t_D	Data sending period, two slots			1598	µs
t_D	Data sending period, three slots			2862	µs
t_{RO}	Receiver On delay		175	213	µs
t_{RD}	Delay before receiving data		213		µs

Table 3. Timing requirements for data transmission.

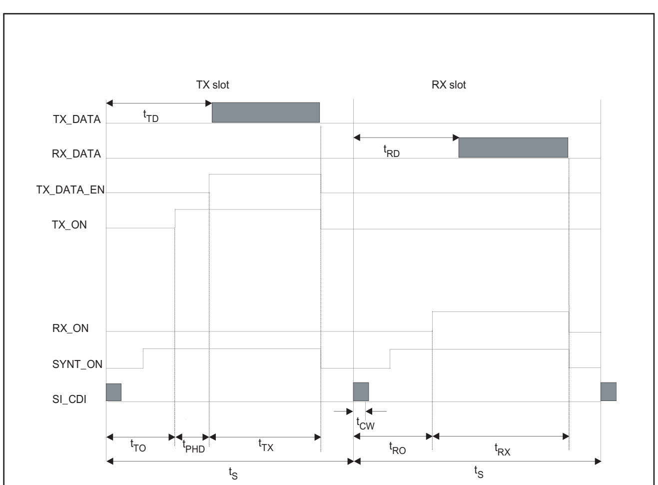


Figure 5. Timing sequence for data transmission.

PX_ON

Packet switch on control is active 'high'. Activate this signal during reception of a Bluetooth payload.

PX_ON is used to control the Slicer of the receiver. Since the General Inquiry Access Code (GIAC), information in a Bluetooth packet header contains an equal number of one's (+F_{MOD}) and zero's (-F_{MOD}), the average frequency will always be centred on the carrier frequency. This provides the Slicer the reference for the fast tuning. If the fast mode is not used during the header then the first bits could be interpreted incorrectly.

The slow mode gives a more accurate FSK compensation of the thresholds for a one and a zero compared to the fast mode; therefore, the BER is less. The fast mode (time constant < 2µs) is used when PX_ON is deactivated and the slow mode (time constant < 50 µs) when it is activated.

SYNT_ON

Synthesiser on control is active 'high'. Activate this signal to power up of the VCO section of the radio. SYNT_ON is used in both transmit and receive mode. This activates the PLL as well as the VCO.

RX_ON

Receive-on control is active 'high'. Activate this signal to enable reception of Bluetooth data on the RX_DATA pin. The transmit-on control (TX_ON) must be deactivated and the synthesiser (SYNT_ON) activated if data is to be received.

TX_ON

Transmit-on control is active 'high'. Activate this signal to enable radio signal output on the ANT pin. The actual transfer of data that exists on the TX_DATA input occurs when TX_DATA_EN goes 'high'. The receive-on control, RX_ON, must also be 'low' and the transmit-switch, TX_SW, be held "high" if data is to be transmitted.

TX_DATA_EN

Enables the modulator thus allowing the input data on TX_DATA to modulate the carrier in transmit mode. TX_DATA_EN is activated after the initialisation of the SYNT_ON signal and the TX_ON signal.

RESET_N

External power on reset is active 'high'. An external power-on-reset digital input signal that will reset the radio controller and its registers. A reset will occur on the positive edge of RESET_N signal. The signal should remain high during operation.

SYS_CLK_REQ

System clock request control is active 'high'. Once the crystal oscillator bit (XO_{CTR}, control register, bit #2) has been set, use this control to switch off (sleep mode) and wake up (idle and operating modes) the reference clock circuitry and corresponding 13 MHz and 1 MHz clock output ports of the module.

Output control

There are four digital output control signals available for controlling external baseband circuitry.

POR

Power-on-reset digital output is activated after the power has been applied to the Bluetooth radio or on a positive edge of the POR_EXT digital input. POR has a transition from 'low' to 'high' after four clock cycles have been delivered to the baseband chip, see figure 6.

SYS_CLK

13 MHz system clock digital output available for the baseband circuitry when the POR_EXT and SYS_CLK_REQ are both 'high'. SYS_CLK will also be available during start-up, independent on the value of SYS_CLK_REQ.

TX_CLK

1 MHz transmit clock digital output available for the baseband circuitry when the POR_EXT and SYS_CLK_REQ (see above) are both 'high'. TX_CLK changes value on rising edges of SYS_CLK.

LPO_CLK

3.2 kHz low power oscillator clock digital output. The clock output is available as soon as the power supply is applied and POR_EXT is 'high'. The LPO is necessary for wake-up timing in the baseband circuitry, if the Ericsson baseband is used.

Data interface

Two digital signals are used for data flow over the air interface.

TX_DATA

Transmit data digital control is active 'high'. The radio module samples Bluetooth data (1 Mbit/s) after a positive edge on TX_CLK, feeds it through a digital filter and on to the radio frequency modulator when TX_DATA_EN is activated. The total delay from the TX_DATA pin to the ANT pin is typically 0.5 µs.

RX_DATA

Receive data digital output is active 'high'. The radio module latches out Bluetooth data (1 Mbit/s) on the RX_DATA pin on falling edges of SYS_CLK when RX_ON is activated. The total delay from the ANT pin to the RX_DATA pin is typically 2.5 µs.

Serial interface

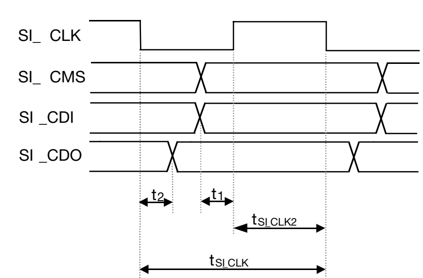
The serial control interface is a JTAG Boundary-Scan Architecture (IEEE Std 1149.1). Interconnection between the serial interface and the external controller (baseband circuit) consists of four 1-bit digital signals; control data input (SI_CDI), control mode select (SI_CMS), control clock (SI_CLK) and control data output (SI_CDO). The timing of these signals is defined in figure 7.

Overview

PBA 313 05 is controlled by programming registers via a 4 pin serial interface and a number of dedicated pins to control the receive and transmit sequences.

The serial interface is accessed using pins SI_CLK, SI_CMS, SI_CDO and SI_CDI. Pins associated with receive and transmit are SYNTH_ON, TX_ON, RX_ON, TX_DATA_EN and PX_ON.

Data to be transmitted is applied to TX_DATA, received data will be available at RX_DATA. The radio relies on an accurate 13 MHz reference signal. This signal can be generated by using a 13 MHz crystal on pins XO_P and XO_N and



	Min	Typ	Max	Unit
t_{SI_CLK}	200	250		ns
t_{SI_CLK2}	76	76		ns
t_1	20			ns
t_2			20	ns

Figure 7. Timing diagram of the serial interface.

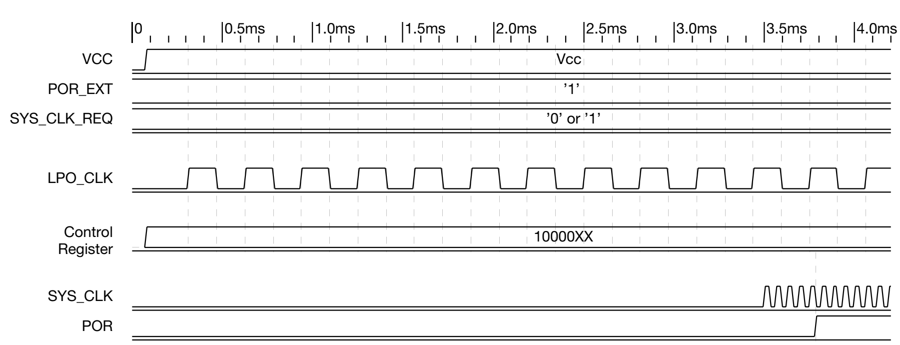


Figure 6. Powering up the module.

trimming to the required frequency via the serial interface. Alternatively an externally generated 13 MHz reference can be applied to the XO_N input, (in this case the oscillator amplifier can be powered down via the serial interface to save power).

A number of clocks are derived from the 13 MHz reference. The LPO output provides a 3.2 kHz reference, which is always available, (this relies either on the use of a crystal or the constant availability of an external 13 MHZ reference). A buffered version of the 13 MHz clock, SYS_CLK and a 1 MHz derived clock, TX_CLK are available when the input pin SYS_CLK_REQ is asserted.

The radio will generate a power on reset signal when powered up. This will reset all on radio registers to a defined state. The signal will also be present on the POR pin so that it can be used as a system reset signal for the base band processor. The radio can be reset to the default state by applying a '0' at the RESET_N pin.

Serial interface

PBA 313 05 contains registers for setting the frequency, storing the value of the signal power etc. The base band processor circuit will read from and write to these registers in PBA 313 05.

The registers are reset to their default values either when EXT_RESET is low or when the supply is first applied (generating a power on reset signal internally). The serial interface is implemented as described in the BlueRF specification.

Additional information for engineers interfacing PBA 313 05 to a baseband can be found in the Programmers Reference and Base Band Interface Guide PBA 313 05/1.

Assembly guidelines

Solder paste

The PBA 313 05 module is made for surface mounting with land grid array (LGA) solder joints. To assemble the module, solder paste (eutectic Tin/Lead) must be printed at the target surface. Preferred solder paste height is 100-127µm (4-5 mil).

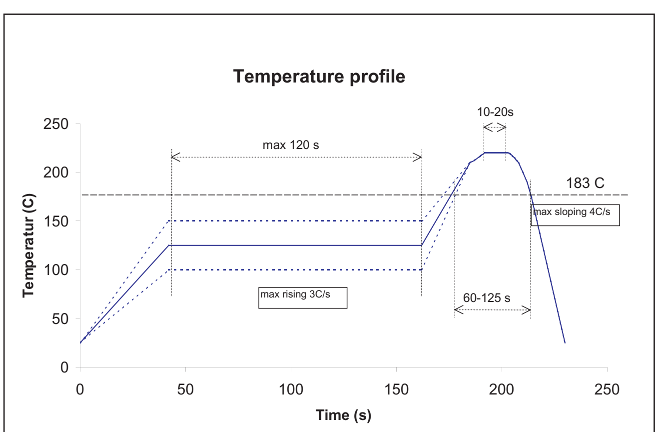


Figure 8. Eutectic SnPb-solder profile.

Soldering profile

It must be noted that the module should not be allowed to be hanging upside down in the reflow operation. This means that the module has to be assembled on the side of the PCB that is soldered last. The reflow process should be a regular surface mount soldering profile (full convection strongly preferred), the ramp-up should not be higher than 3°C/s and with a peak temperature of 210-225°C during 10-20 seconds. Max sloping rate should not be higher than 4°C/s (see example of reflow profile in figure 8).

Placement

The recommended pickup coordinates for the PBA 313 05 shield is based on a nozzle with inner diameter 1.9 mm. From the origin of coordinates, (0,0) for (x,y), the pickup coordinates are (4.4mm,4.4mm) for (x,y).

Control interface

Operation together with a Bluetooth Baseband using the Ericsson Bluetooth Core is recommended.

Antenna interface

50 Ω Bluetooth ISM band antenna (2.4 – 2.5 GHz).

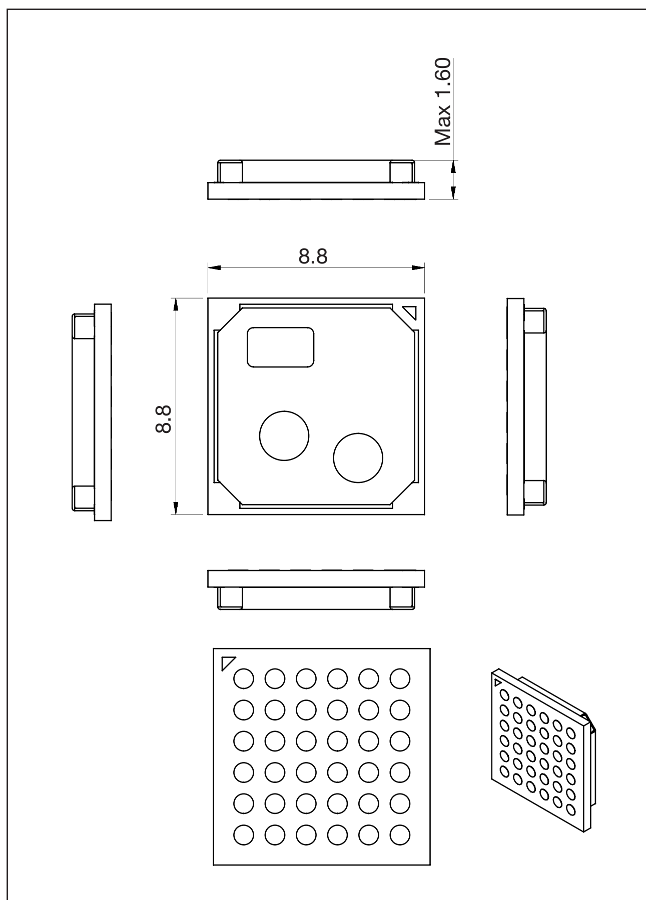


Figure 9. Mechanical dimensions and footprint

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Preliminary Data Sheet

EN/LZT 146 131 R1B