Frame Engine and Datalink Manager

FEATURES

- Single-chip multi-channel packet processor supporting a maximum aggregate bandwidth of 156 Mbit/s for line rate throughput transfers of packet sizes from 40 to 9.6 Kbytes, for up to an aggregate of 84 T1s, 63 E1s, or 3 DS-3s.
- Provides simultaneous support of PPP, Frame Relay, Multilink-PPP and Multilink-Frame Relay protocols. Alternative protocols supported via HDLC termination and full packet store of the data within the HDLC structure.

MULTILINK PPP AND FRAME RELAY BUNDLES

- Capable of supporting fragment sizes from 1 to 9.6 Kbytes.
- Support for 3 egress fragmentation sizes (128, 256, and 512 bytes) configurable on a per multilink bundle. Optionally full packet transfers are supported on a per bundle basis.
- Supports up to 42 multilink bundles with up to 12 member links per bundle. These bundles are composed of independent HDLC channels.
- Support for up to 100ms of intra bundle skew in the receive direction when supporting the minimum fragment size.
- Support for PPP header compression as per RFC 1661.

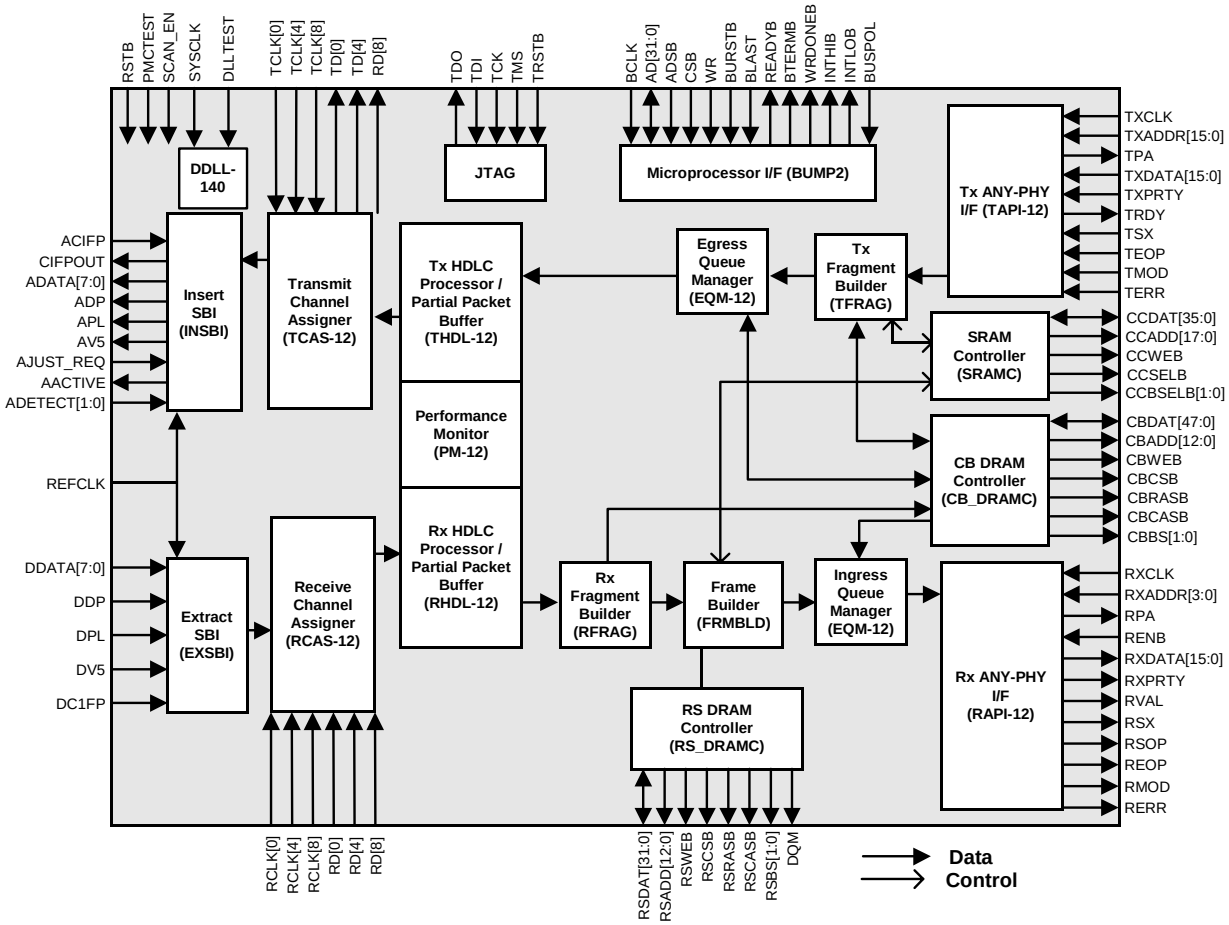
PPP

- Support for 16 COS levels in accordance with RFC 2686.
- Either 12 bit or 24 bit sequence number, with short and long fragment header formats, is supported.
- Link Control protocol packets are identified by the PID as control protocols and will be forwarded to the Any-PHY interface.

FRAME RELAY

- Link layer address lookup can be performed based on HDLC channel and 10 bit DLCI for HDLC channels supporting Frame Relay protocols.
- The lookup algorithm can support a maximum of 16 K connection identifiers (CIs) amongst multilink FR bundles. The connection identifiers are ignored in singlelink FR channels.
- Control frames are identified and forwarded to Any-PHY interface.
- 12 bit sequence numbers supported.
- FECN, BECN, and DE ingress processing as per FRF.12.

BLOCK DIAGRAM



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HDLC

- Support for up to 1024 bidirectional HDLC channels, with individual HDLC channel speeds ranging from 56 Kbit/s to 52 Mbit/s. In a channelized application, the number of time-slots assigned to an HDLC channel is programmable from 1 to 24 (for T1/J1) and from 1 to 31 (for E1).
- The 1024 HDLC channels can be assigned to a mixture of physical links via the 19.44 MHz SBI interface. The SBI transports the equivalent of 3 STS-1 synchronous payload envelopes (SPE). Each STS-1 SPE can be individually configured to carry 28 T1/J1s, 21 E1s or 1 DS3.
- For each channel, supports programmable flag sequence detection and generation, bit stuffing and de-stuffing, and validation and generation of either CRC-CCITT or CRC-32 frame check sequences.
- For each channel, the receiver checks for packet abort sequences, octet aligned packet length and for minimum and maximum packet length.

INTERFACES

- 52 MHz 16 bit Any-PHY Level 2 packet interface for transfer of packet, frame or fragment data using an external controller. The interface is capable of supporting full datagram transfer on a per Any-PHY channel basis, or fragmented packets or frames on a per Any-PHY channel basis.
- A 19.44 MHz SBI bus supporting up to 84 links.
- 3 separate clock and data interfaces to support 3 links of arbitrary data rate up to 52 MHz (e.g., DS3/E3). The device can be configured to process data from either the clock and data interfaces or from the SBI on a per clock-data-link/SPE basis.
- A 100 MHz, 48-bit SDRAM interface for ingress and egress per packet/fragment storage.
- A 100 MHz, 32-bit SDRAM interface for ingress re-sequencing data. structures.
- A 100 MHz, 36-bit SSRAM interface for Ingress/Egress Context storage.
- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan.
- A 32-bit microprocessor interface for configuration and status monitoring.

TECHNOLOGIES

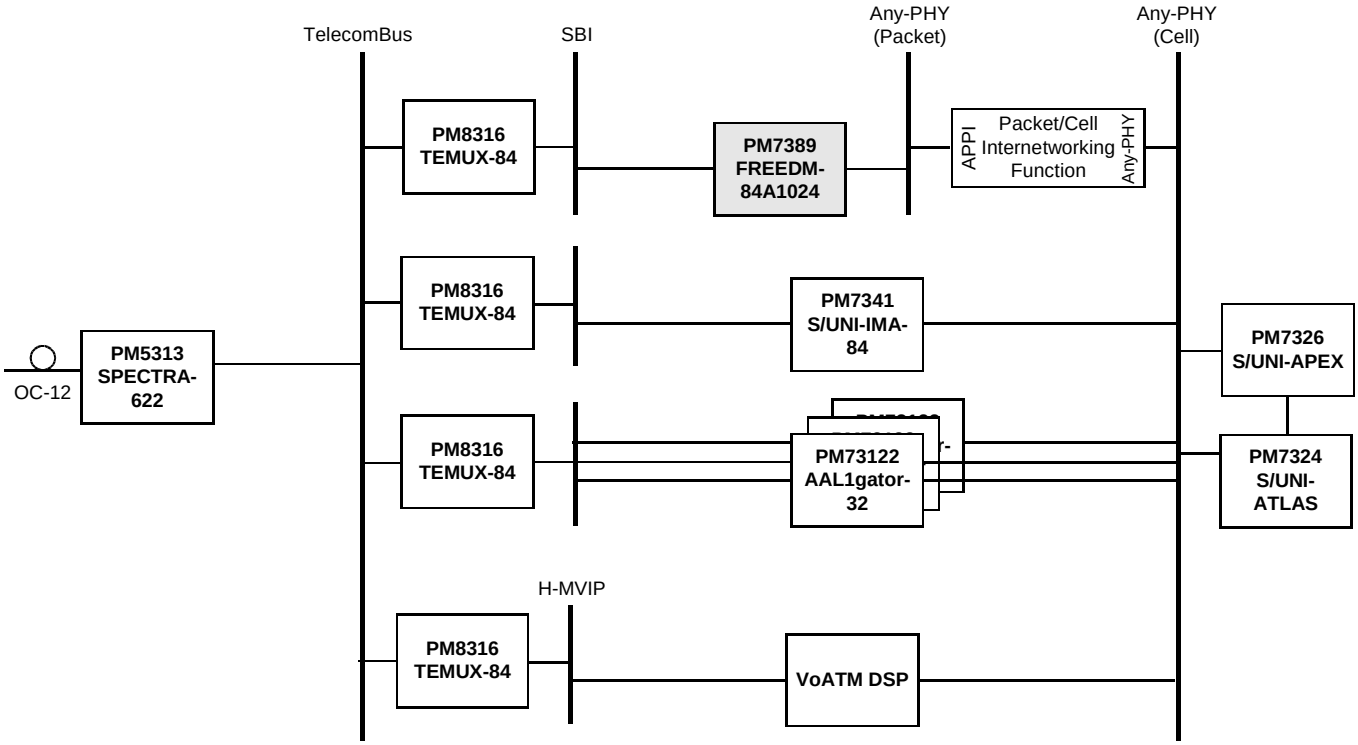
- 40 mm x 40 mm, 520 pin (1.27 mm pitch) enhanced ball grid array (SBGA) package.
- Low power 0.18 mm CMOS technology using 1.8 V core power and 3.3 V I/O.

APPLICATIONS

- IETF PPP interfaces for routers.
- Frame Relay interfaces for ATM or Frame Relay switches and multiplexers.
- Internet/Intranet access equipment.

TYPICAL APPLICATION

OC-12 MULTISERVICE ARCHITECTURE



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