

# Synchronous Buck Converter Controller

## FEATURES

- 6- to 16.5-V Input Range (Si9150CY)
- Voltage-Mode PWM Control
- Low-Current Standby Mode
- Enable Control
- Dual 100-mA Output Drivers
- 2% Band Gap Reference
- Multiple Converters Easily Synchronized
- Over-Current Protection

## DESCRIPTION

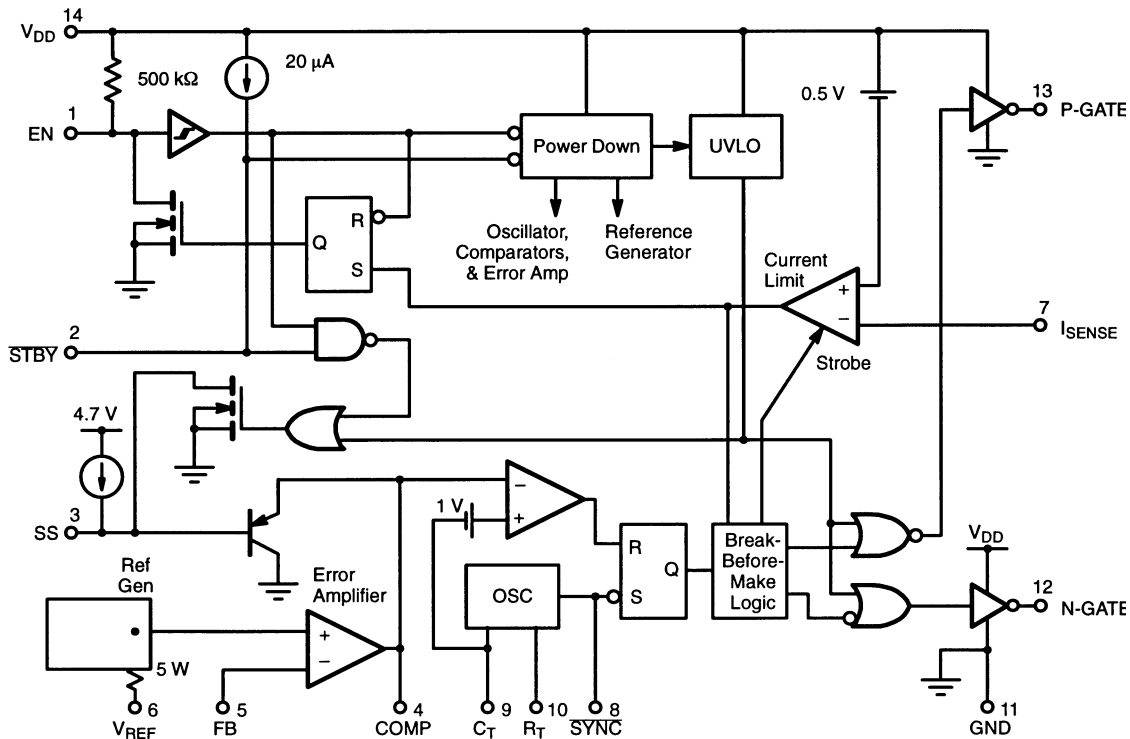
The Si9150 synchronous buck regulator controller is ideally suited for high-efficiency step down converters in battery-powered equipment. Combined with the Si9943DY MOSFET half-bridge, a 90% efficient, 7.5-W, 3.3-V or 5-V power supply can be implemented using standard surface-mount assembly techniques. The wide input range allows operation from NiCd or NiMH battery packs using six to ten cells.

Over-current protection is achieved by sensing the on-state voltage drop across the high side p-channel MOSFET, which eliminates the need for a current sense resistor.

Duty ratios of 0 to 100% and switching frequencies up to 300 kHz are possible. The IC can be disabled by pulling EN low ( $I_{DD} = 100 \mu\text{A}$ ), or the 2.5-V reference can be maintained, with all other functions disabled, by pulling STBY low ( $I_{DD} = 500 \mu\text{A}$ ).

The Si9150 is available in a 14-pin SOIC and rated for the commercial temperature range of 0 to 70°C (C suffix), and the industrial temperature range of -40 to +85°C (D suffix).

## FUNCTIONAL BLOCK DIAGRAM



Synchronous Buck Regulator Controller

**ABSOLUTE MAXIMUM RATINGS**

Voltages Referenced to GND.

$V_{DD}$ .....	18 V
$I_{SENSE}$ Input .....	-2 V to $V_{DD} + 2$ V
All Other Inputs .....	-0.3 to $V_{DD} + 0.3$ V
P-Gate, N-Gate Continuous Source/Sink Current .....	.50 mA
Storage Temperature .....	-65 to 125°C
Operating Junction Temperature .....	150°C

Power Dissipation (Package)<sup>a</sup>14-Pin SOIC (Y Suffix)<sup>b</sup> ..... 900 mWThermal Impedance ( $\Theta_{JA}$ )

14-Pin SOIC ..... 140°C/W

Notes

a. Device mounted with all leads soldered or welded to PC board.

b. Derate 7.2 mW/°C.

**SPECIFICATIONS<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $6.0 \leq V_{DD} \leq 16.5$ V	Limits C Suffix 0 to 70°C			Limits D Suffix -40 to 85°C			Unit
			Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
<b>Reference</b>									
Output Voltage	$V_{REF}$	$T_A = 25^\circ\text{C}$ Measured at Feedback <sup>e</sup> Pin 5	2.45	2.50	2.55	2.45	2.50	2.55	V
		$T_{MIN}$ to $T_{MAX}$ <sup>d</sup>	2.425	2.500	2.575	2.40	2.500	2.60	
<b>Oscillator</b>									
Maximum Frequency	$f_{MAX}$	$C_{OSC} = 94.3$ pF, $R_{OSC} = 28.7$ k $\Omega$ $T_A = 25^\circ\text{C}$	255	300	345	255	300	345	kHz
Initial Accuracy	$f_{OSC}$	$C_{OSC} = 212$ pF, $R_{OSC} = 41.2$ k $\Omega$ $T_A = 25^\circ\text{C}$	85	100	115	85	100	115	
Oscillator Ramp Amplitude	$V_{OSC}$	$T_A = 25^\circ\text{C}$ , 100 kHz	2.05	2.65	2.85	2.05	2.65	2.85	V
Temperature Stability <sup>d</sup>	$f_{TEMP}$	$V_{DD} = 10$ V, $T_{MIN}$ to $T_{MAX}$	-5	$\pm 3$	+5	-6	$\pm 4$	+6	%
<b>Error Amplifier</b>									
Input BIAS Current	$I_B$	$V_{FB} = V_{REF}$		25	500		25	750	nA
Open Loop Voltage Gain <sup>d</sup>	$A_{VOL}$		60	72		58	72		dB
Offset Voltage	$V_{OS}$			10	25		10	30	mV
Unity Gain Bandwidth <sup>d</sup>	BW		1	1.5		1	1.5		MHz
Output Current	$I_{OUT}$	Source, $V_{COMP} = 2.50$ V		-0.30	-0.20		-0.30	-0.15	mA
		Sink, $V_{COMP} = 1.0$ V	1	2.5		0.9	2.5		
Power Supply Rejection	PSRR		50	70		48	70		dB
<b>Protection</b>									
Current Limit Threshold Voltage	$V_{CL}$	$T_A = 25^\circ\text{C}$ , $V_{DD} = 10$ V	0.43	0.49	0.55	0.43	0.49	0.55	V
Current Limit Delay to Output <sup>d</sup>	$t_d$	$T_A = 25^\circ\text{C}$		500	1000		500	1000	ns
Undervoltage Lockout Voltage	$V_{UVLO}$	Upper Threshold	5.4	5.7	6.0	5.38	5.7	6.01	V
Undervoltage Hysteresis	$V_{HYS}$		0.10	0.17	0.25	0.10	0.17	0.26	
Softstart Pull-Up Current	$I_{SS}$			20			20		$\mu\text{A}$
<b>Supply</b>									
Supply Current (Enable Low)	$I_{OFF}$			60	100		60	100	$\mu\text{A}$
Supply Current (Enable High)	$I_{CC}$	$C_L = 0$ pF, $f_{OSC} = 100$ kHz $V_{DD} = 10$ V		2.2	3.0		2.2	3.0	mA
Supply Current ( $\overline{\text{STBY}}$ Low)	$I_{SB}$			300	500		300	550	$\mu\text{A}$

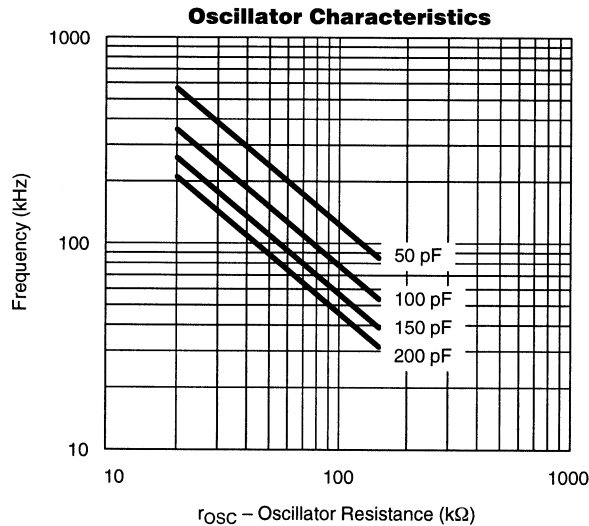


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			Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
<b>Output</b>									
Output High Voltage	V <sub>OH</sub>	I <sub>OUT</sub> = 10 mA, V <sub>DD</sub> = 10 V	9.75			9.7			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OUT</sub> = -10 mA, V <sub>DD</sub> = 10 V			0.25			0.3	
Output Resistance	R <sub>OUT</sub>	I <sub>OUT</sub> = 100 mA, V <sub>DD</sub> = 10 V		10	20		10	25	Ω
Rise Time <sup>d</sup>	t <sub>r</sub>	C <sub>L</sub> = 800 pF, V <sub>DD</sub> = 10 V		30	60		30	70	ns
Fall Time <sup>d</sup>	t <sub>f</sub>			30	60		30	70	
<b>Logic</b>									
Delay to Output	t <sub>d(EN)</sub>	Transition High to Low		0.25	1		0.25	1	μs
Enable Pull-Up Resistance	R <sub>EN</sub>			500			500		kΩ
STBY Pull-Up Current	I <sub>STBY</sub>	T <sub>A</sub> = 25°C, V <sub>STBY</sub> = 0 V V <sub>DD</sub> = 10 V	-25	-20	-15	-28	-20	-12	μA
Turn-On Threshold	V <sub>ENH</sub>	V <sub>DD</sub> = 10 V, Rising Input Voltage	6	6.8	8	6	6.8	8	V
Turn-Off Threshold	V <sub>ENL</sub>	V <sub>DD</sub> = 10 V, Falling Input Voltage	2	3.75	5	2	3.75	5	

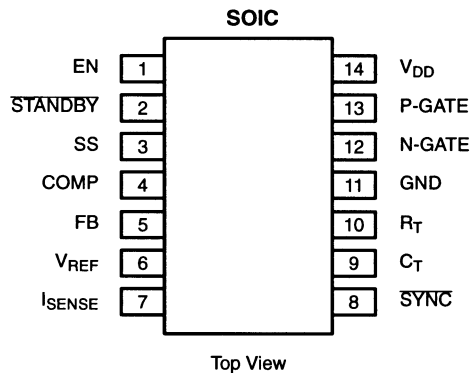
Notes

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. Guaranteed by design, not subject to production test.
- e. The voltage reference is trimmed with the feedback (Pin 5) connected to compensation (Pin 4) so that the effect of the error amplifier's input offset voltage is eliminated.
- f. C<sub>OSC</sub> includes the PC board's parasitic capacitance.

**TYPICAL CHARACTERISTICS**



## PIN CONFIGURATION



## PIN DESCRIPTION

### Pin 1: EN

When this pin is low, the IC is shut down. After a low signal is applied to EN, then COMP, REF,  $R_T$ , and  $C_T$  settle toward ground; N-GATE,  $\overline{STBY}$  and Soft-Start are grounded; and P-GATE is pulled high. The current consumption is no more than 100  $\mu$ A in this state. This input's threshold has substantial hysteresis so that a capacitor to GND can be used to delay restart after the current limit is activated. After  $V_{ENH}$  is exceeded, one clock cycle elapses before N-GATE and P-GATE are enabled. EN is pulled up to  $V_{DD}$  through a 500-k resistor and is pulled down internally when the current limit is triggered.

### Pin 2: $\overline{STBY}$

Has a function similar to EN. The differences are that the EN pin is unaffected, that the reference is still available, that bias currents are still present internally, and that this pin's pull up current is present. This pin should be used to disable an application if the reference voltage is still needed.

### Pin 3: Soft-Start (SS)

This pin limits the maximum voltage that the error amplifier can output. A capacitor between this pin and ground will limit the rate at which the duty factor can increase during initial power up, during a restart when EN or  $\overline{STBY}$  goes high, or after the current limit is triggered. A capacitor here can prevent an application from triggering the Si9150's current limit during startup. Soft-Start is pulled low if either EN or  $\overline{STBY}$  is low.

### Pin 4: Compensation (COMP)

This pin is tied directly to the output of the error amplifier. The feedback network which insures the stability of an application uses this pin. COMP settles low when either EN or  $\overline{STBY}$  is pulled low.

### Pin 5: Feedback (FB)

This pin is attached directly to the inverting input of the error amplifier. This pin is used to regulate the power supply's output voltage.

### Pin 6: Reference ( $V_{REF}$ )

The internal 2.5-V reference generator is attached to this pin through a 5- $\Omega$  resistor. A 0.1- $\mu$ F bypass capacitor is needed to suppress noise. Also note that the generator has an open emitter; it will not pull down. The maximum current that the generator will source before it current limits is about 10 mA. Many parts of the IC use this voltage, so it is important not to overload the reference generator.

### Pin 7: $I_{SENSE}$

This pin should be attached to the switched node (the drains of the application's p-channel and n-channel MOSFETs). If the voltage between  $V_{DD}$  and this pin is more than 0.46 V while the P-GATE is low, the current limit is activated. The current limit is relatively slow to prevent false triggering due to noise. Activating the current limit causes EN to be pulled to GND.  $I_{SENSE}$  may be operated from  $V_{DD} + 2$  V to GND - 2 V. For operation above 13.5  $V_{DD}$  a filter (1 k $\Omega$ , 33 pF) is needed between the MOSFET drains and the  $I_{SENSE}$  pin; refer to Figure 1.

### Pin 8: $\overline{SYNC}$

This pin forces the clock to reset when low, and is also pulled low when the clock resets itself. Thus if several Si9150's have their sync pins shorted together, they will be synchronized; the shortest duration clock will control the other clocks.

**Pin 9:  $C_T$** 

A capacitor from this pin to ground is charged until it reaches 2.5 V, at which point the capacitor is rapidly discharged. The resulting sawtooth with about 1 V added is compared to the input voltage at COMP to determine whether P-GATE and N-GATE should be high or low. The maximum recommended value for  $C_{OSC}$  is 200 pF (See Typical Characteristics). The capacitor's charging current is controlled by Pin 10,  $R_T$ .

**Pin 10:  $R_T$** 

The IC applies 2.5 V to this pin, and the current is mirrored and applied to Pin 9 while charging the capacitor. The minimum recommended value of  $R_{OSC}$  is 20 k $\Omega$  (Figure 1).

**Pin 11: GND**

Since the Si9150 has a high-side current limit, it is important that  $V_{DD}$  track the voltage on the source of the p-channel power MOSFET. For noise immunity, it is best to separate the logic ground from the power ground. The logic ground should be decoupled to  $V_{DD}$  through at least a 1- $\mu$ F capacitor. The two grounds may be connected by a path that is long

compared to the the path from  $V_{DD}$  to the source of the application's p-channel MOSFET.

**Pin 12: N-GATE**

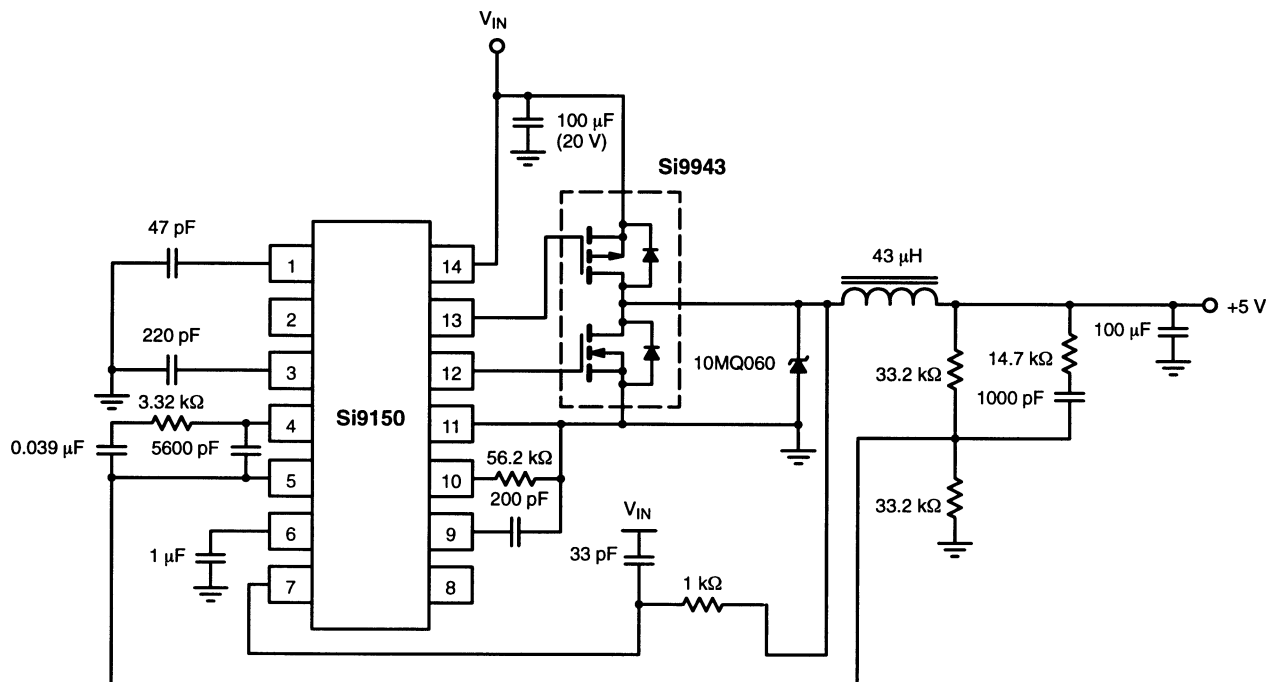
This pin is used to drive the application's n-channel MOSFET. When turning the n-channel MOSFET off, the p-channel MOSFET will not be turned on until N-GATE is within a few volts of ground. This pin is low while either EN or  $\overline{STBY}$  is low.

**Pin 13: P-GATE**

This pin is used to drive the application's p-channel MOSFET. The break before make circuitry for the P-GATE is complimentary to that for the N-GATE. This pin is high while either EN or  $\overline{STBY}$  is low.

**Pin 14:  $V_{DD}$** 

This pin powers the IC. The connection between this pin and the source of the p-channel FET should be as short as practical. Read Pin 11's description for bypassing suggestions.

**APPLICATIONS**

**FIGURE 1.** Typical Application Circuit