CMOS 4-BIT MICROCONTROLLER
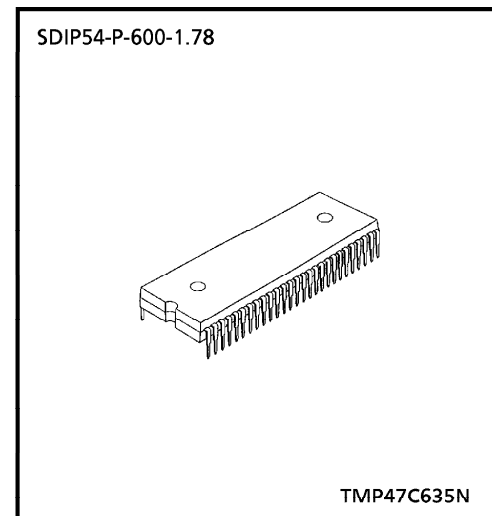
TMP47C635N

The 47C635 is based on the TLCS-470 CMOS series. The 47C635 has on-screen display circuit (OSD) to display characters and marks which indicate channel or time on TV screen, A/D converter (comparator) input, D/A converter output such as TV. The 47C635 is the chip with extension I/O ports for the 47C634.
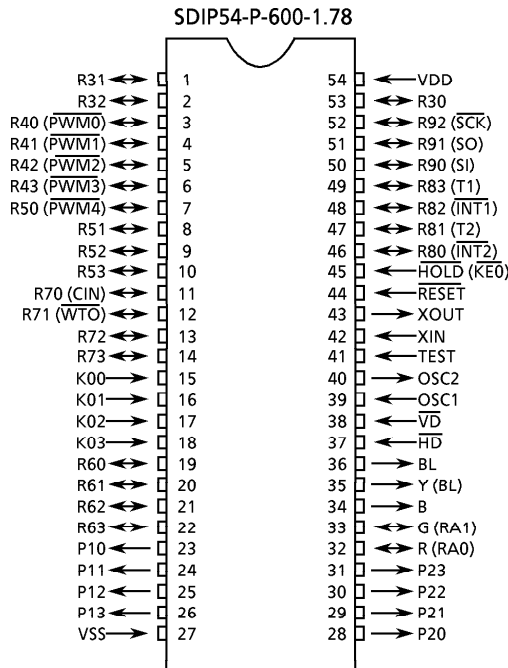
PART No.	ROM	RAM	PACKAGE
TMP47C635N	6144 × 8-bit	384 × 4-bit	SDIP54-P-600-1.78

FEATURES
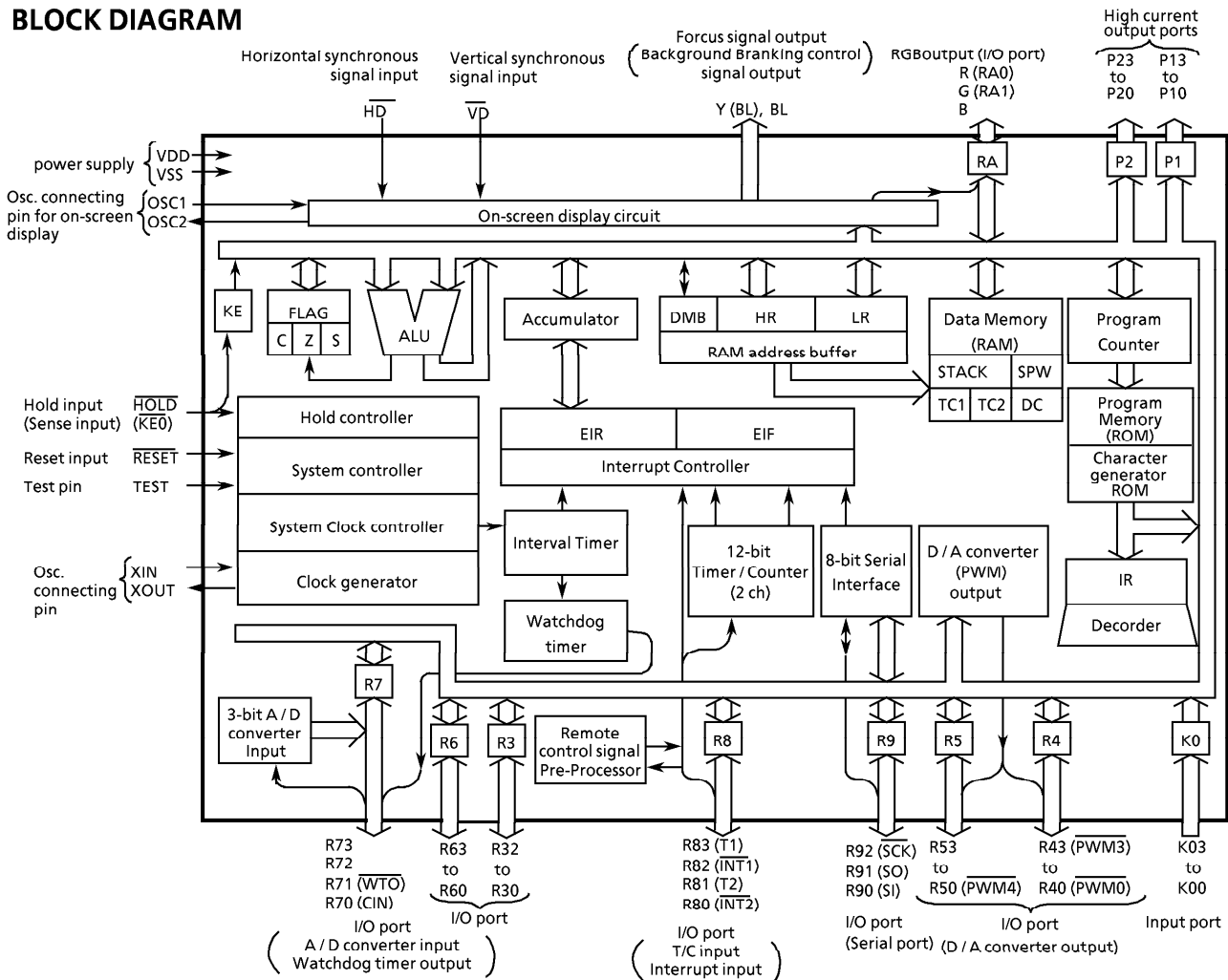
◆4-bit single chip microcomputer
◆Instruction execution time : 1.9 μs (at 4.2 MHz)
◆92 basic instructions
◆Table look-up instructions
◆5-bit to 8-bit data conversion instruction
◆Subroutine nesting : 15 levels max.
◆6 interrupt sources (External : 2, Internal : 4)
　　All sources have independent latches each, and multiple
　　interrupt control is available
◆I/O port (41 pins)
　● Input　　2 ports　　5 pins
　● I/O　　　8 ports　　28 pins
　● Output　2 ports　　8 pins
◆Interval Timer
◆Two 12-bit Timer / Counters
　　Timer, event counter, and pulse width measurement mode
◆Watchdog Timer
◆Serial Interface with 8-bit buffer
　● Simultaneous transmission and reception capability
　● External / internal clock, leading / trailing edge shift, 4/8-bit
◆On-screen display circuit
　● Character patterns :　　48 characters
　● Characters displayed :　16 columns × 2 lines
　● Composition :　　　　　8 × 8 dots (smoothing function)
　● Size of character :　　　2 kinds (line by line)
　● Color of character :　　7 kinds (character by character)
　● Variable display position : Horizontal 64 / Vertical 64 steps
◆D/A converter (Pulse width modulation) outputs
　● 14-bit resolution　　1 channel
　● 6-bit resolution　　4 channels
◆3-bit A/D converter (Comparator) input
　　Auto frequency control signal (S-shaped curve) detection
◆Horizontal synchronous signal is detected by timer/counter
◆Remote control signal preprocessing capability
◆High current outputs
　　LED direct drive capability (typ. 20 mA × 8 bits)
◆Hold function : Battery/Capacitor back-up
◆Real Time Emulator : BM47C834A

SDIP54-P-600-1.78

TMP47C635N

PIN ASSIGNMENT (TOP VIEW)

SDIP54-P-600-1.78

Left pin	#	#	Right pin
R31 ◄►	1	54	◄ VDD
R32 ◄►	2	53	◄► R30
R40 (PWM0) ◄►	3	52	◄► R92 (SCK)
R41 (PWM1) ◄►	4	51	◄► R91 (SO)
R42 (PWM2) ◄►	5	50	◄► R90 (SI)
R43 (PWM3) ◄►	6	49	◄► R83 (T1)
R50 (PWM4) ◄►	7	48	◄► R82 (INT1)
R51 ◄►	8	47	◄► R81 (T2)
R52 ◄►	9	46	◄► R80 (INT2)
R53 ◄►	10	45	◄ HOLD (KE0)
R70 (CIN) ◄►	11	44	◄ RESET
R71 (WTO) ◄►	12	43	► XOUT
R72 ◄►	13	42	◄ XIN
R73 ◄►	14	41	◄ TEST
K00 ►	15	40	► OSC2
K01 ►	16	39	◄ OSC1
K02 ►	17	38	◄ VD
K03 ►	18	37	◄ HD
R60 ◄►	19	36	► BL
R61 ◄►	20	35	► Y (BL)
R62 ◄►	21	34	► B
R63 ◄►	22	33	◄► G (RA1)
P10 ◄	23	32	◄► R (RA0)
P11 ◄	24	31	► P23
P12 ◄	25	30	► P22
P13 ◄	26	29	► P21
VSS ►	27	28	► P20

BLOCK DIAGRAM

Horizontal synchronous signal input — HD
Vertical synchronous signal input — VD
Forcus signal output (Background Branking control) signal output — Y (BL), BL
RGBoutput (I/O port) R (RA0) G (RA1) B
High current output ports P23 to P20, P13 to P10

power supply { VDD, VSS
Osc. connecting pin for on-screen display { OSC1, OSC2

On-screen display circuit

RA, P2, P1

KE
FLAG C Z S
ALU
Accumulator
DMB HR LR
RAM address buffer
Data Memory (RAM)
STACK SPW
TC1 TC2 DC
Program Counter
Program Memory (ROM)
Character generator ROM

Hold input (Sense input) HOLD (KE0) — Hold controller
Reset input RESET — System controller
Test pin TEST — System Clock controller
Osc. connecting pin { XIN, XOUT — Clock generator

EIR EIF
Interrupt Controller
Interval Timer
Watchdog timer

12-bit Timer / Counter (2 ch)
8-bit Serial Interface
D / A converter (PWM) output
IR
Decorder

R7
3-bit A / D converter Input
R6 R3
Remote control signal Pre-Processor
R8
R9 R5 R4
K0

R73 R72 R71 (WTO) R70 (CIN)
I/O port (A / D converter input / Watchdog timer output)

R63 to R60, R32 to R30
I/O port

R83 (T1) R82 (INT1) R81 (T2) R80 (INT2)
I/O port (T/C input / Interrupt input)

R92 (SCK) R91 (SO) R90 (SI)
I/O port (Serial port)

R53 to R50 (PWM4), R43 (PWM3) to R40 (PWM0)
I/O port (D / A converter output)

K03 to K00
Input port

PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS		
K03 to K00	Input	4-bit input port.		
P13 to P10	Output	4-bit output port with latch. 8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL].		
P23 to P20				
R43 (PWM3) to R41 (PWM1)	I/O (Output)	4-bit I/O port with latch. When used as input port or D/A converter outputs pins, the latch must be set to "1".		6-bit D/A converter (PWM) output
R40 (PWM0)				14-bit D/A converter (PWM) output
R53 to R51	I/O			
R50 (PWM4)	I/O (Output)			6-bit D / A converter (PWM) output
R32 to R30	I/O	3-bit I/O port with latch. When used as input port, the latch must be set to "1".		
R63 to R60	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".		
R73 to R72	I/O	4-bit I/O port with latch. When used as input port watchdog, output pin, or A/D converter input pin, the latch must be set to "1".		
R71 (WTO)	I/O (Output)			Watchdog timer output
R70 (CIN)	I/O (Input)			3-bit A/D converter input
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer / counter external input pin, the latch must be set to "1".		Timer / Counter 1 external input
R82 (INT1)				External interrupt 1 input
R81 (T2)				Timer / Counter 2 external input
R80 (INT2)				External interrupt 2 input
R92 (SCK)	I/O(I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".		Serial clock I/O
R91 (SO)	I/O(Output)			Serial data output
R90 (SI)	I/O(Input)			Serial data input
G (RA1)	Output (I/O)	RGB output		2-bit I/O port with latch. When used as input port, the latch must be set to "1".
R (RA0)				
B	Output			
Y (BL), BL	Output (Output)	Forcus signal output		Background branking control signal output
HD, VD	Input	Horizontal synchronous signal input, Vertical synchronous signal output.		
OSC1, OSC2	Input, Output	Resonator connecting pin of on-screen display circuit.		
XIN, XOUT	Input, Output	Resonator connecting pin. For inputting external clock, XIN is used and XOUT is opened.		
RESET	Input	Reset signal input		
HOLD (KE0)	Input (Input)	Hold request / release signal input		Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.		
VDD	Power Supply	+ 5 V		
VSS		0 V (GND)		

OPERATIONAL DESCRIPTION

Concerning the 47C635 the configuration and functions of hardware are described.
As the description has been provided with priority on those parts differing from the 47C660, the technical data sheets for the 47C660 shall all so be referred to.

1. SYSTEM CONFIGURATION

◆ INTERNAL CPU FUNCTION
They are the same as those of the 47C660 except system clock controller.

◆ PERIPHERAL HARDWARE FUNCTION
① Input / Output Ports
② Interval Timer
③ Timer / Counters (TC1, TC2)
④ Watchdot Timer
⑤ Remote Control pulse detector
⑥ On-screen display (OSD) control circuit
⑦ A/D converter (comparator) input
⑧ D/A converter (Pulse Width Modulation) output

The description has been provide with priority on functions (①, ⑥, ⑦ and ⑧) added to and changed from 47C660.

2. INTERNAL CPU FUNCTION

2.1 Operation clock control

On the 47C635 only single clock mode is available. As single clock mode is automatically selected at the initilization, there is no necessary to set system clock control command register (OP16).
After reset, 47C635 is placed in the single-clock mode.
Only the normal 1 operating mode can be active. (Refer to fig 2.1)
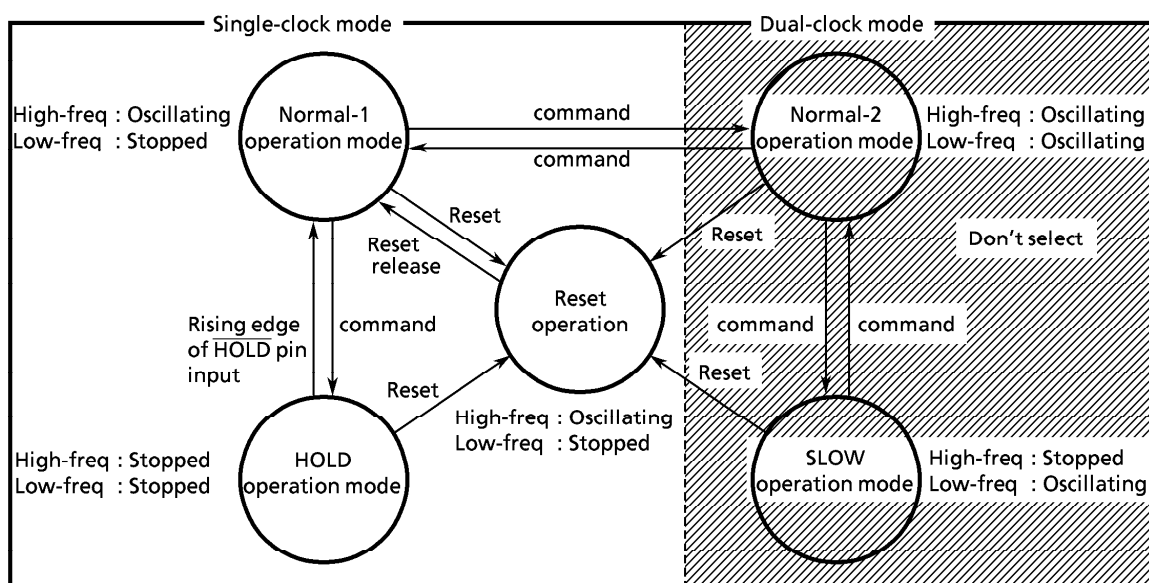
Figure 2-1. Operation Mode Transition Diagram

3. PERIPHERAL HARDWARE FUNCTION

3.1 I/O ports

The 47C635 has 12 I/O ports (41 pins) each as follows.

① K0 ; 4-bit input
② P1 , P2 ; 4-bit output
③ R3 ; 3-bit input / output (shared with the pulse width modulation output)
④ R4 , R5 ; 4-bit input / output (shared with pulse width modulation output)
⑤ R6 ; 4-bit input / output
⑥ R7 ; 4-bit input / output (shared with comparator input and watchdog timer output)
⑦ R8 ; 4-bit input / output (shared with external interrupt input and timer/counter input)
⑧ R9 ; 3-bit input / output (shared with serial port)
⑨ RA ; 2-bit input / output (shared with on-screen display output)
⑩ KE ; 1-bit sense input (shared with hold request / release signal input)

The description has been provide with priority on functions (③, ④ and ⑥) added to and changed from 47C660, and it describes port of ⑦, which item of on-screen display circuit.

(1) Port R3 (R32 to R30)

3-bit I/O port with latch. When used as input port, the latch must be set to "1". The latch is initialized to "1" during reset. There isn't the R33 pin. If it accessed the latch must be set to "1".
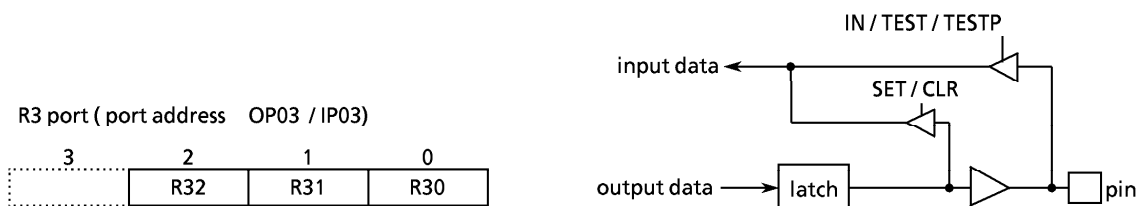
Figure 3-1. R3 port

(2) Port R4 (R43 to R40)

This is a 4-bit I/O port with latch. It is a port common to D/A converter (PWM) output port. R4 port output buffers are Tri-state, and each bit of them can be controled independently by the program. Controling the Tri-state is performed by the command register accessed as port address OP00. When some bit of the OP00 is 0, the corresponding bit of the output buffers becomes high impedance state. The output latch should be set to "1" when the port is used as $\overline{PWM}$ output port,the $\overline{PWM}$ output should be to "H" level (PWM data is all "0") when the port is used as R 4 port. The output buffers should be set to high impedance state,when the port is used as input port. And the R4 output latch be set to "1", $\overline{PWM}$ output be set to "High" level, and the output buffer be set to High-Inpedance state during reset.

R4 (Port Address OP04/IP04)
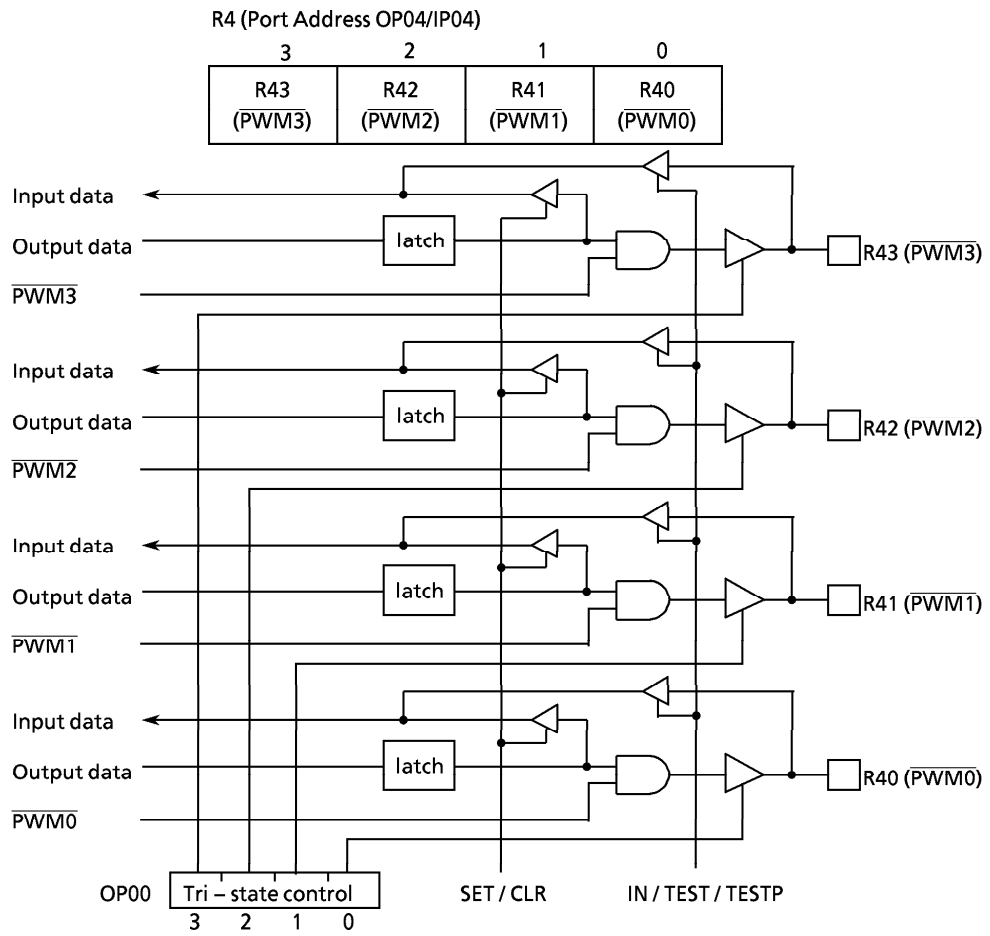
Figure 3-2. Port R4 ($\overline{\text{PWM}}$)

(3) Port R5 (R53 to R50)

The 4-bit I/O port with latch. The only R50 pin share D/A converter (PWM) output. The port output buffers are tri-state, and each bit of them can be controled independently by the program. Controling the tri-state is performed by the command register accessed as port address OP13.

Example : LD   A , #1111$_B$;   OP13←1111$_B$
           OUT   A , %OP13
           OUT   #05H , %OP05   ;   R5 port←5$_H$

R5 Port (Port Address   OP05 / IP05)

3	2	1	0
R53	R52	R51	R50 (PWM4)
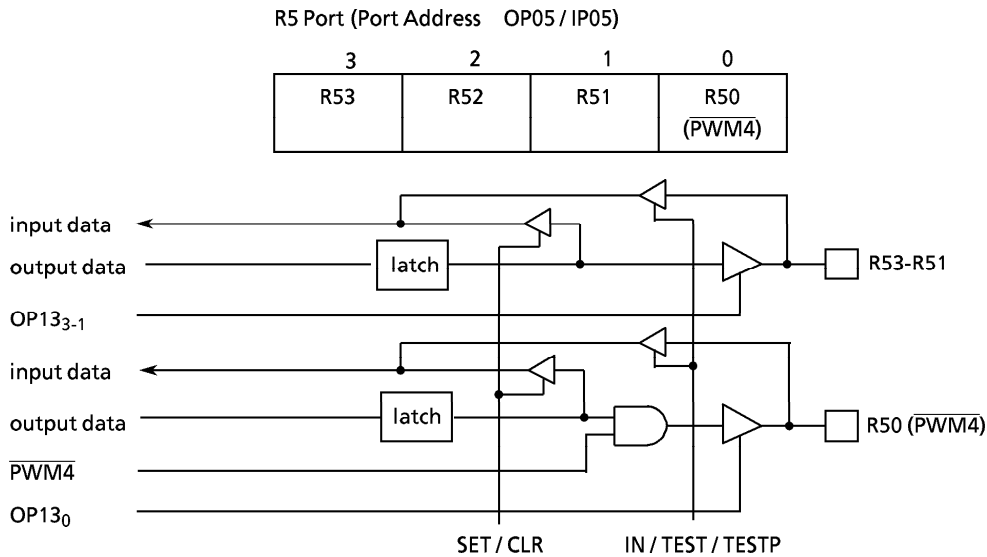
Figure 3-3.   Port R5

(4) Port R7 (R73 to R70)

The 4-bit I/O port with latch. When used as an input port, the latch should be set to "1". The latch is initialized to "1" during reset. R72, R73 pins is I/O port usually.

Pin R70 (CIN) is shared with the digital input usual and the A/D converter (comparator) input for Auto Frequency Control signal detection. CIN input is comparator input and setting of 3-bit D/A convert for reference voltage are performed by the comand register. Pin R71 ($\overline{\text{WTO}}$) is shared with the watchdog timer output. R70, R71 pins latch is initialized to "1" during reset, and they are able to use I/O port usually.

R7 I/O Port (Port address IP07/OP07)

3	2	1	0
R73	R72	R71 ($\overline{\text{WTO}}$)	R70 (CIN)

Figure 3-4.   Port R7

Table 1-1. Port Address Assignments and Available I/O Instructions
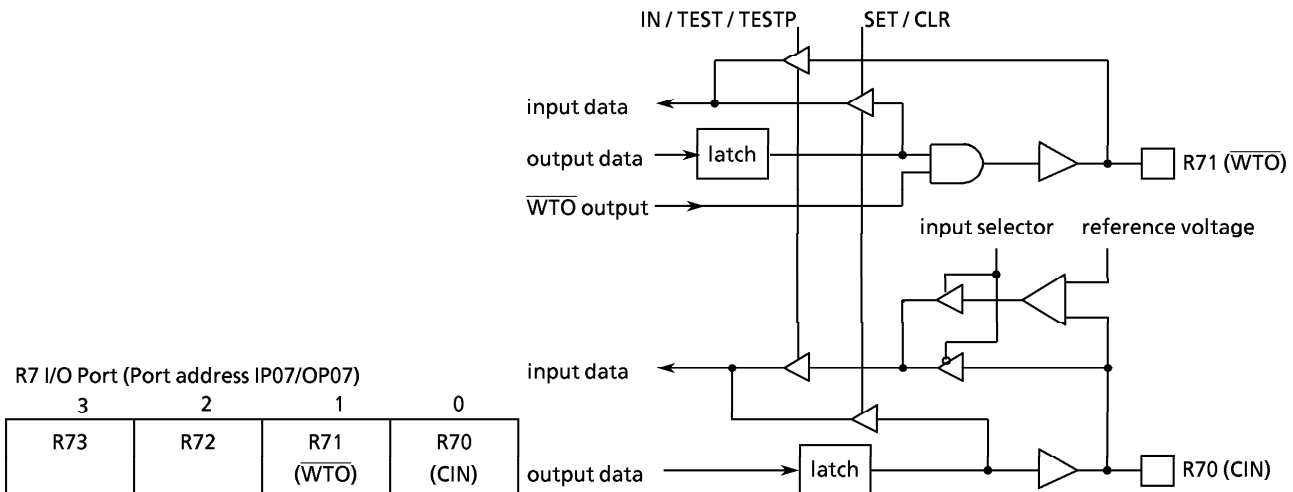
Port Address (**)	Input (IP**)	Output (OP**)	IN %p, A / IN %p, @HL	OUT A, %p / OUT @HL, %p	OUT #k, %p	OUTB @HL	SET %p, b / CLR %p, b	TEST %p, b / TESTP %p, b	SET @L / CLR @L / TEST @L
00H	K0 input port	Tri-state(R4 port) Control	○	○	○	-	-	○	-
01	P1 output port latch	P1 output port	○	○	○	○ (Note 3)	○	○	-
02	P2 output port latch	P2 output port	○	○	○	○	○	○	-
03	R3 input port	R3 output port	○	○	○	-	○	○	-
04	R4 input port	R4 output port	○	○	○	-	○	○	○
05	R5 input port	R5 output port	○	○	○	-	○	○	○
06	R6 input port	R6 output port	○	○	○	-	○	○	○
07	R7 input port	R7 output port	○	○	○	-	○	○	○
08	R8 input port	R8 output port	○	○	○	-	○	○	-
09	R9 input port	R9 output port	○	○	○	-	○	○	-
0A	RA input port	RA output port	○	○	○	-	-	○	-
0B	———	———	-	-	-	-	-	-	-
0C	———	OSD command selector	-	○	○	-	-	-	-
0D	Remote control count value register	Remote control offset value register	○	○	○	-	-	○	-
0E	Status input (Note 2)	Remote control single preprocess circuit control	○	○	○	-	-	○	-
0F	Serial receive buffer	Serial transmit buffer	○	○	○	-	-	-	-
10H	Undefined	Hold operation mode	-	○	-	-	-	-	-
11	Undefined	———	-	-	-	-	-	-	-
12	Undefined	A / D converter input control	-	○	-	-	-	-	-
13	Undefined	Tri-state (R5 port) control	-	○	-	-	-	-	-
14	Undefined	———	-	-	-	-	-	-	-
15	Undefined	Watchdog timer control	-	○	-	-	-	-	-
16	Undefined	———	-	-	-	-	-	-	-
17	Undefined	PWM buffer selector	-	○	-	-	-	-	-
18	Undefined	PWM data transfer buffer	-	○	-	-	-	-	-
19	Undefined	Interval timer interrupt control	-	○	-	-	-	-	-
1A	Undefined	OSD control	-	○	-	-	-	-	-
1B	Undefined	———	-	-	-	-	-	-	-
1C	Undefined	Timer/Counter 1 control	-	○	-	-	-	-	-
1D	Undefined	Timer/Counter 2 control	-	○	-	-	-	-	-
1E	Undefined	SIO control 1	-	○	-	-	-	-	-
1F	Undefined	SIO control 2	-	○	-	-	-	-	-

Note 1 . "———" means the reserved state. Unavailable for the user programs.
Note 2 . The status input of serial interface, clock generator, and $\overline{HOLD}$ ($\overline{KE0}$) pin.
Note 3 . The 5-bit to 8-bit data conversion instruction [OUTB @HL] , automatic access to ports P1 and P2.

3.2 On-screen display (OSD) circuit

An on-screen display (OSD) circuit used to display characters and symbols in built into the TV screen. Amaximum of 32 characters,as 16 columns × 2 lines,out of 48 character patterns can be displayed at a time.

3.2.1 OSD Circuit Function

①	Number of characters	48 kinds
②	Number of characters displayed	32 characters (16 columns × 2 lines)
③	Composition of a character	8 × 8 dots (with smoothing function)
④	Size of character	2 kinds (selectable line by line)
⑤	Color of character	7 kinds (selectable character by character)
⑥	Display position variable	horizontal 64 steps, vertical 64 steps

3.2.2 OSD Circuit Configuration
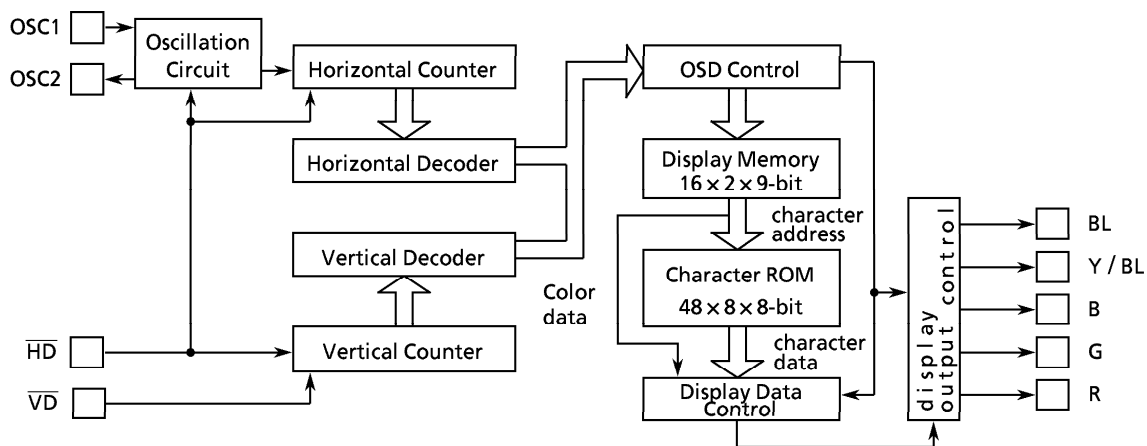
Figure 3-5. OSD Circuit

3.2.3 OSD Circuit Control

The OSD circuit is controlled by the command selector (OP0C) and control register (OP1A). Table 3-2 shows the relationship between OP0C and OP1A. OP1A is multiplexed with the six output control registers which control the display start position, color of character and character size of character, and the two transfer control registers which transter character data to the display memory.

The output control registers consist of 8 bits and all bits can be written by accessing OP1A two times. However, the second access is not required unless the second data are changed. The addressed "0 to 5" are assigned to the six output control registers. OP1A can be accessed by writing the address of the control register where data are to be changed to OP0C. The transfer control registers can be accessed by writing "6" or "7" to OP0C. The transfer control registers have a 12 – bit configuration and can access OP1A three times succession. The first access sets which column is displayed within one line 16 columns. The second and third accesses written 6 bit of character data.

The display memory has a 16-columns × 9-bit × 2 lines configuration with a one-to-one correspondence to the number of columns displayed on the screen. The display data consist of 6 character data bits and 3 color data bits for a total of 9 bits. When "6" is written to OP0C, line 1 is stored to the display memory, when "7" is written to OP0C, line 2 is stored. That is after accessing OP0C, the character data specified the second and third times are written to the display memory area specified in the first OP1A access together with the color data loaded to control register DCR50. Thus color can be specified for each character. After setting of all control registers is completed, the character data read from the character ROM(00 to 2F$_H$)are output to the R, G and B pins together with the color data by setting OP0C to "F".

Note : The writing a data from display memeory is prior than the reading. Therefore, if a data is written to the display memory until the display line is displaying, the display is incorrect.

A data must be written to display memeory when the display is off or when one and two display line are not displayed.

OSD command selector (OP0C)	OSD control register to be accessed through OP1A
0	Control for the horizontal start position of the first display line DCR00: 3=– 2=– 1=HS15 0=HS14 (1st access) DCR01: 3=HS13 2=HS12 1=HS11 0=HS10 (2st access)
1	Control for the vertical start position of the first display line DCR10: 3=– 2=– 1=VS15 0=VS14 (1st access) DCR11: 3=VS13 2=VS12 1=VS11 0=VS10 (2st access)
2	Control for the horizontal start position of the second display line. DCR20: 3=– 2=– 1=HS25 0=HS24 (1st access) DCR21: 3=HS23 2=HS22 1=HS21 0=HS20 (2st access)
3	Control for the vertical start position of the second display line. DCR30: 3=– 2=– 1=VS25 0=VS24 (1st access) DCR31: 3=VS23 2=VS22 1=VS21 0=VS20 (2st access)
4	Control for the character sizes,smoothing switch and OSD output polarities DCR40: 3=CS21 2=CS20 1=CS11 0=CS10 (1st access) DCR41: 3=ESMZ 2=BLIV 1=YIV 0=RGBIV (2st access)
5	Control for the color register and OSD output buffers'tri-state' DCR50: 3=– 2=RDT 1=GDT 0=BDT (1st access) DCR51: 3=EBF3 2=EBF2 1=EBF1 0=EBF0 (2st access)
6	display memory write mode for the first display line(address 00-0F) 3=DMA3 2=DMA2 1=DMA1 0=DMA0 (1st access) 3=– 2=– 1=CRA5 0=CRA4 (2st access) 3=CRA3 2=CRA2 1=CRA1 0=CRA0 (3st access)
7	display memory write mode for the second display line(address 10-1F) 3=DMA3 2=DMA2 1=DMA1 0=DMA0 (1st access) 3=– 2=– 1=CRA5 0=CRA4 (2st access) 3=CRA3 2=CRA2 1=CRA1 0=CRA0 (3st access)
E	display OFF
F	display ON

Table 3-2. OSD control commands and control registers

(1) Composition of character and smoothing function
Each character is compsited by 8×8 dots. Each dot corresponds to a bit in the character ROM. Figure 3-5. (a) shows an example Composition of a character.
Smoothing function is the function to make characters look smooth. In the time the smoothing function is enabled, additional dots are displayed in the middle of the place where two dots contact each other only at a corner. Controlling of the smoothing function is performed by ESMZ in the OSD control register DCR41. Figure 3-6. (b) shows an example of the smoothing function.

(a)   without smoothing   (b)   with smoothing
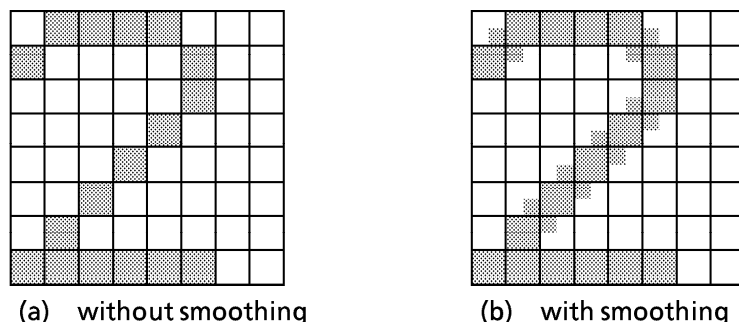
Figure 3-6. Composition of character and smoothing function

(2) Character size and color to display
Size of the characters displayed on screen is selectable line by line from 2 sizes. The size of the first and second display line is disignated by CS11 to CS10 and CS21 to CS20 in the OSD control register DCR40,respectively.
Table 3-3 shows the setting values and character sizes of DCR40.
Table 3-4 shows the display character sizes.
One out of seven colors can be selected for each character to be displayed and are determined by RDT,GDT,and BDT of DCR50. The color data are written to the display memory automatically at the same time as character data are written

Character size (DCR40)	second display line		first display line	
	CS21	CS20	CS11	CS10
small character	1	0	1	0
large character	0	1	0	1
display OFF	0	0	0	0

Table 3-3. Designation of character size

	small character	large character
dot size	$2T_{HD} \times 2T_{OSC}$	$4T_{HD} \times 4T_{OSC}$
character size	$16T_{HD} \times 16T_{OSC}$	$32T_{HD} \times 32T_{OSC}$

Note. T_{HD} :the period of horizontal synchrorous signal
      T_{OSC} :the period of OSD clock oscillation

Table 3-4. character size.

colors displayed on screen	color data(DCR50)		
	RDT	GDT	BDT
Blank	0	0	0
Blue	0	0	1
Green	0	1	0
Sian	0	1	1
Red	1	0	0
Mazenda	1	0	1
Yellow	1	1	0
White	1	1	1

Note. Color to display :   RGB pin uses Red, Green, Blue such as.

Table 3-5.   select of color to display

(3) Display start position
Display start position of each display line on screen can be shifted by software.
The vertical and horizontal display starting position for the first line is determined by HS10 to 15 and VS10 to 15 of DCR00 to 11.
The vertical and horizontal display starting position for the second line is determined by HS20 to25 and VS20 to 25 of DCR20 to 31. Each has a resolution of 64 steps.
The control register and display line on screen are shown in Table 3-6.
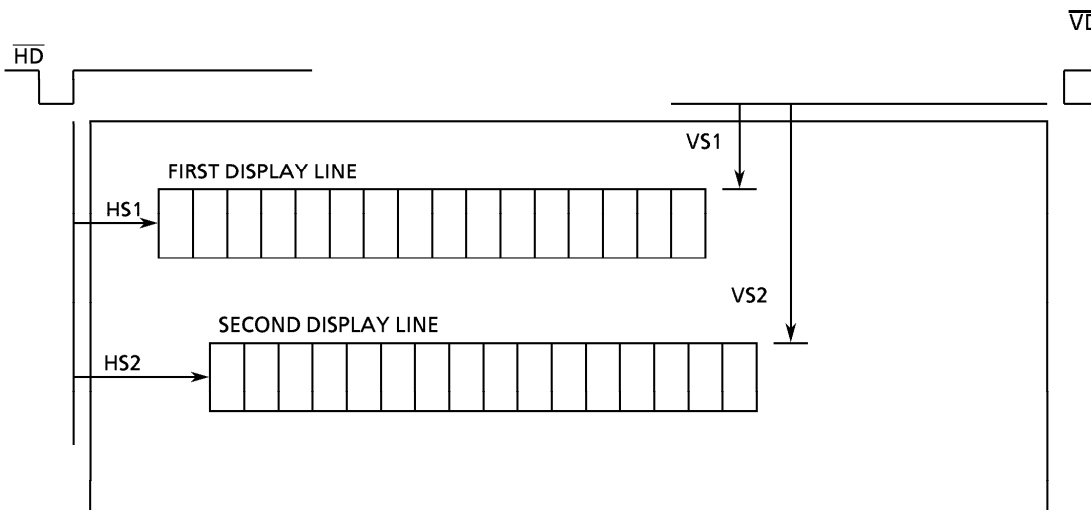
Figure 3-7. TV screen image

SYMBOL	CONTENTS
HS10 to HS15	horizontal start position of the first display line $HS1 = ((32 \times HS15 + 16 \times HS14 + 8 \times HS13 + 4 \times HS12 + 2 \times HS11 + HS10) \times 4 + X) T_{OSC}$
VS10 to VS15	vertical start position of the first display line $VS1 = (32 \times VS15 + 16 \times VS14 + 8 \times VS13 + 4 \times VS12 + 2 \times VS11 + VS10) \times 4T_{HD}$
HS20 to HS25	horizontal start position of the second display line $HS2 = ((32 \times HS25 + 16 \times HS24 + 8 \times HS23 + 4 \times HS22 + 2 \times HS21 + HS20) \times 4 + X) T_{OSC}$
VS20 to VS25	vertical start position of the second display line $VS2 = (32 \times VS25 + 16 \times VS24 + 8 \times VS23 + 4 \times VS22 + 2 \times VS21 + VS20) \times 4T_{HD}$

Note.   X : X is 17 when small character.
X is 34 when large character.

Table 3-6. Display start position

*   The vertical display positions of lines 1 and 2 can be specified independently but,to prevent overlapping of the two lines on the display, the value for the vertical display position of line 2 must satisfy 〔$VS2 > VS1 + CS11 \times 16T_{HD} + CS10 \times 32T_{HD}$〕.

3.2.4 Y/BL signal

The Y signal (the logical or output of the R, G and B signals) makes the display clearer by deleting the background only where characters are displayed. The BL signal deletes the entire background for one character (8 × 8 dots) and is output for all data except that at address $2F_H$ in the character ROM.

The Y/BL pin is used for both Y signal and BL signal output. Which of the two signals is to be output is determined by the upper 2 bits of OP0A. The dotted lines in Figure 3-7 show the Y/BL signal output being scanned.
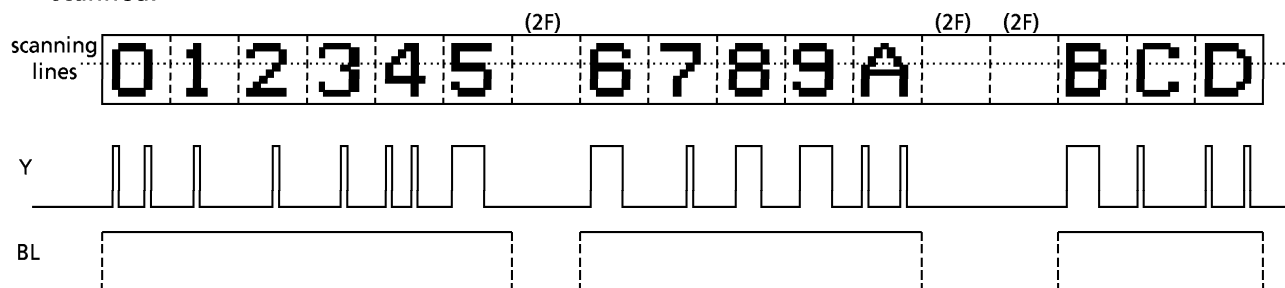
Figure 3-8. Example of Y and BL signal output

3.2.5 Control of OSD outputs buffer

The OSD outputs for Y,BL and RGB use tri-state output buffers for which the respective polarities can be inverted. Polarity is controlled by DRC41 and tri-state is controlled by DRC51.
Bit 3 of DRC41 is used for controlling the smoothing function.

register	bit	symbol	output name	data "0"	data "1"
DRC41	3	ESMZ	——	smoozing OFF	smoozing ON
	2	BLIV	BL	active High	active Low
	1	YIV	Y	active High	active Low
	0	RGBIV	RGB	active High	active Low
DRC51	3	EBF3	Y / BL	output buffer OFF	output buffer ON
	2	EBF2	B	output buffer OFF	output buffer ON
	1	EBF1	G	output buffer OFF	output buffer ON
	0	EBF0	R	output buffer OFF	output buffer ON

Table 3-7. Control of OSD output

3.2.6 RA Port Function

R signal output and G signal output ports are also used as I/O ports. When not used for color signals,use is possible as normal I/O ports. RA port and Y/BL selection is performed by OP0A.
Also,the upper 2 bits of IP0A are used to input the OSD display status.

Port address OP0A

OP0A3	OP0A2	OP0A1	OP0A0

→ RA0 output

→ RA1 output

control of OSD output and RA port

		output pin No.			
OP0A3	OP0A2	22	23	24	25
0	0	R	G	B	Y
0	1	R	G	B	B L
1	0	RA0	G	B	Y
1	1	RA0	RA1	B	B L

port address IP0A

V02	V01	IP0A1	IP0A0

→ RA0 input

→ RA1 input

0 : first display line display ON
1 : first display line display OFF

0 : second display line display ON
1 : second display line display OFF
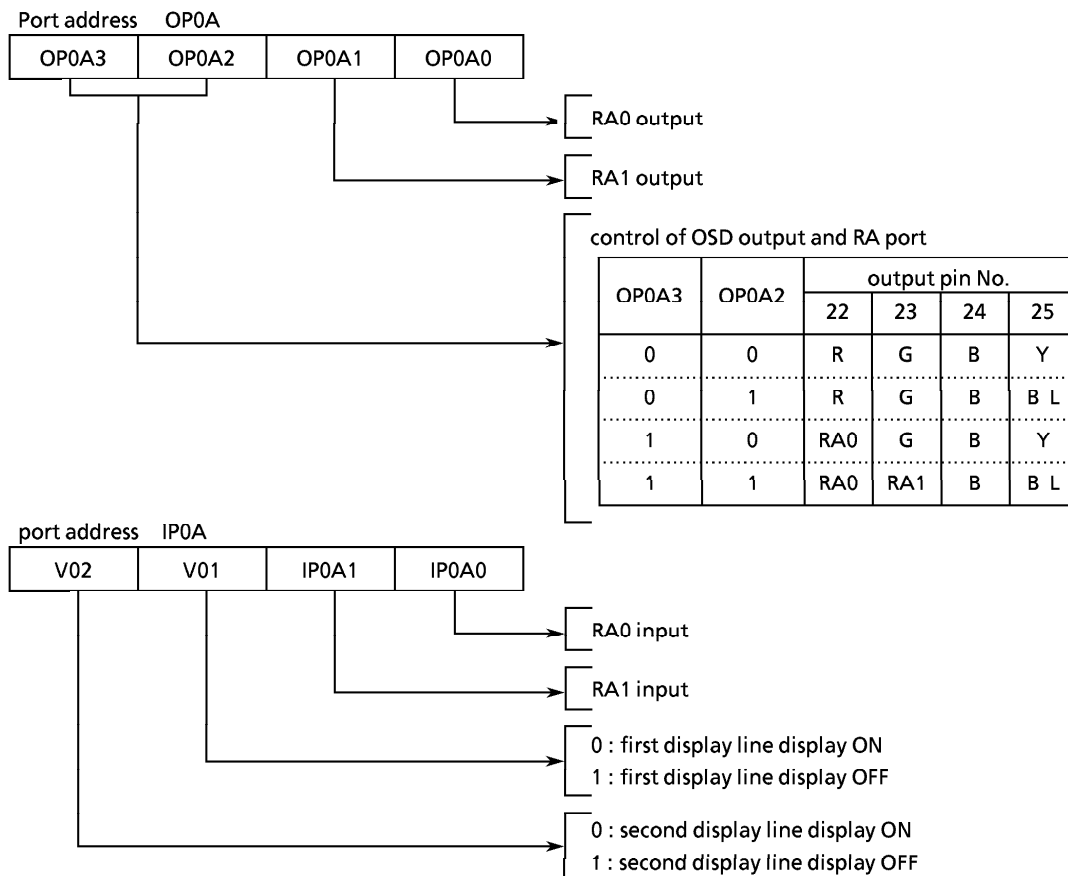
Figure 3-9. Port RA

3.2.7 Character ROM (Standard characters)

Figure 3-10 shows the standard pattern characters and symbols available as character data. Character patterns can also be set by the user.

(Background)
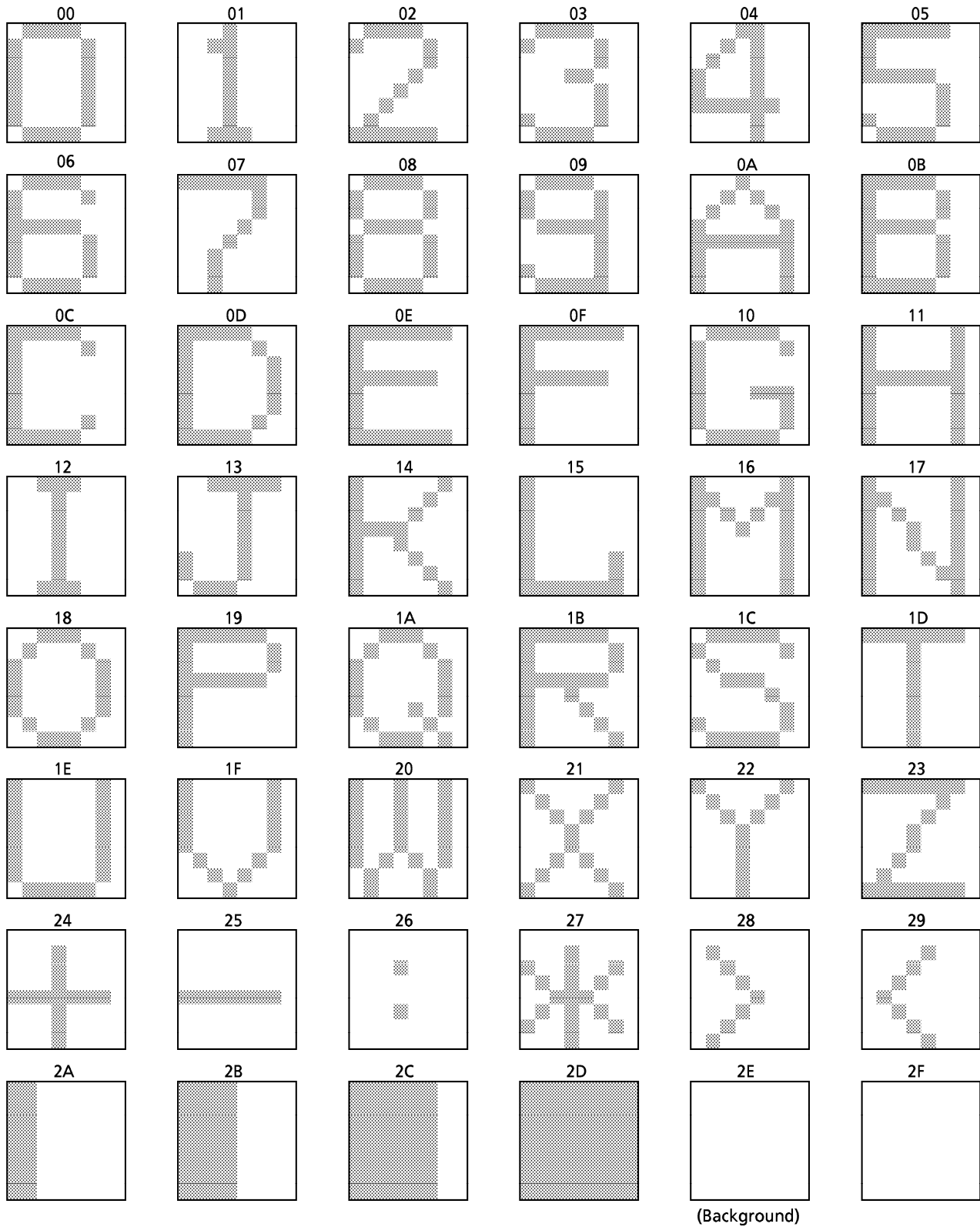
Figure 3-10. Character ROM address and character pattern

Note : *The character data in address 2FH of character ROM must be blank data. (Set character data of the 2FH address to "0".)*
Therefore, the number of character pattern specified by users.

3.3 3-bit A/D converter (Comparator) input

Comparator input consists of a comparator and a 3-bit D/A comvertor. AFC input voltage can be detected in 8 steps by sensing bit 0 of IP07 while cahnging the reference voltage (D/A convertor output voltage) with the command register (OP12).
R70 pin is also used for comparator input. Bit 3 is used to set R70 pin for ordinary digital input.
The comparator is disabled and bit 3 is set to "0" during reset. The latch should be set to "1" when R70 pin is used for comparator input and digital input.

3.3.1 Circuit Configuration
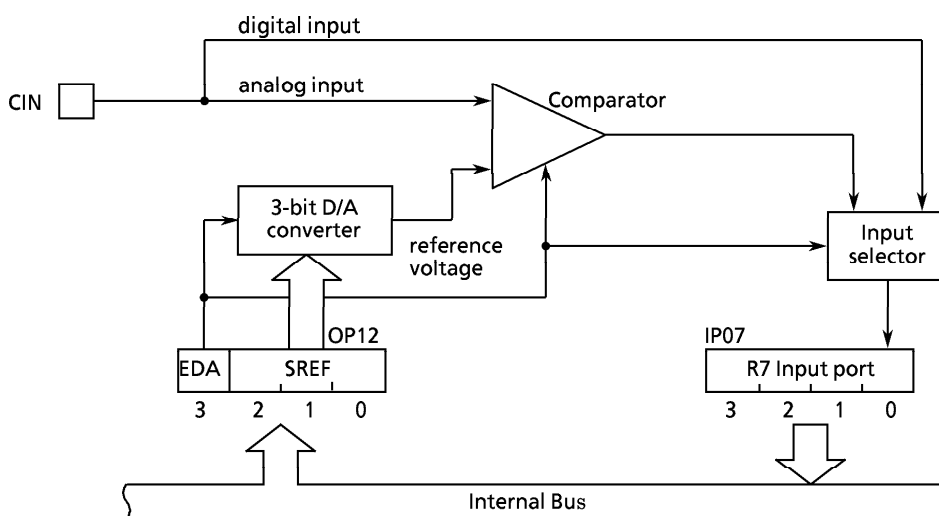
Figure 3-11. Comparator input circuit

3.3.2 Control of Comparator Input

The reference voltage of the comparator is set using the lower 3 bits of the command register. Table 3-8 shows the reference voltage when V_{DD} = 5 V.

Comparator input control command registor (Port address OP12)

OP12			reference
2	1	0	voltage [V]
0	0	0	0.62
0	0	1	1.25
0	1	0	1.87
0	1	1	2.50
1	0	0	3.12
1	0	1	3.75
1	1	0	4.37
1	1	1	5.00
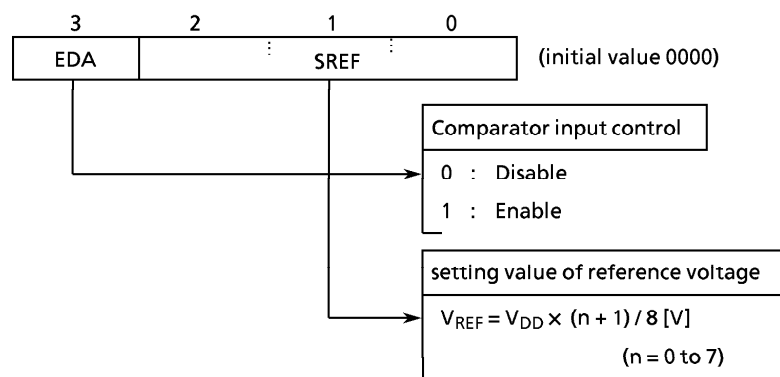
Figure 3-12. Control Command Registor   Table 3-8. Reference Voltage

3.4 D / A converter (PWM) output

The 47C635 have five channels built-in D/A converter (Pulse width Modulation) outputs. $\overline{PWM}$ output can easily be obtained by connecting an external low pass filter.

$\overline{PWM}$ outputs data are multiplex to the R4 port and R50 pin. When the R4 ($\overline{PWM}$) port and R50 pin are used for $\overline{PWM}$ output, the corresponding bits of R4, R50 output latch should be set to "1". The R4, R5 output latch is initialized to "1" during reset.

$\overline{PWM}$ output is controlled by the buffer selector (OP17) and the data transfer buffer (OP18). PWM data written to the data transfer buffer can be sent to the PWM data latch by writing "C_H" to the buffer selector, and $\overline{PWM}$ output $\overline{PWM}$ output. PWM data transferred to the PWM data latch remain intact until overwritten. Resetting and holding clear the buffer selector, data transfer buffer and PWM data latch to "0" ($\overline{PWM}$ output is "H" level).

3.4.1 Configuration of Pulse Width Modulation circuit

Configuration of pulse width modulation circuit shown in Figure 3-14.

3.4.2 Output waveform of PWM circuit

(1) $\overline{PWM0}$ output

$\overline{PWM0}$ is a PWM output controlled by 14 bits data. The basic period of the $\overline{PWM0}$ is $T_M = 2^{15} / fc$.
The higher 8 bits of 14 bits data are used to control the pulse width of the pulse output with the period of $T_S = T_M / 64$, which is the sub - period of the $\overline{PWM0}$. When the 8 bits data are decimal n ($0 \leq n \leq 255$), this pulse width becomes $n \times t_0$, where $t_0 = 2 / fc$.
The lower 6 bits of 14 bits data are used to control the generation of an additional t_0 wide pulse in each T_S period. When the 6 bits data are decimal m ($0 \leq m \leq 63$), the additional pulse is generated in each of m periods out of 64 periods contained in a T_M period. The relationship between the 6 bits data and the position of T_S period where the additional pulse is generated is shown in Table 3-9 (The additional pulse is not generated on $T_{S(0)}$).

(2) $\overline{PWM1}$ to $\overline{PWM4}$ output

Each of $\overline{PWM1}$ to $\overline{PWM4}$ is a PWM output controlled by 6 bits data. The period of them is $T_M = 2^7 / fc$. When the 6 bits data are decimal k ($0 < k < 63$), the pulse width becomes $k \times t_0$. The waveform is also illustrated in Figure 3-13.
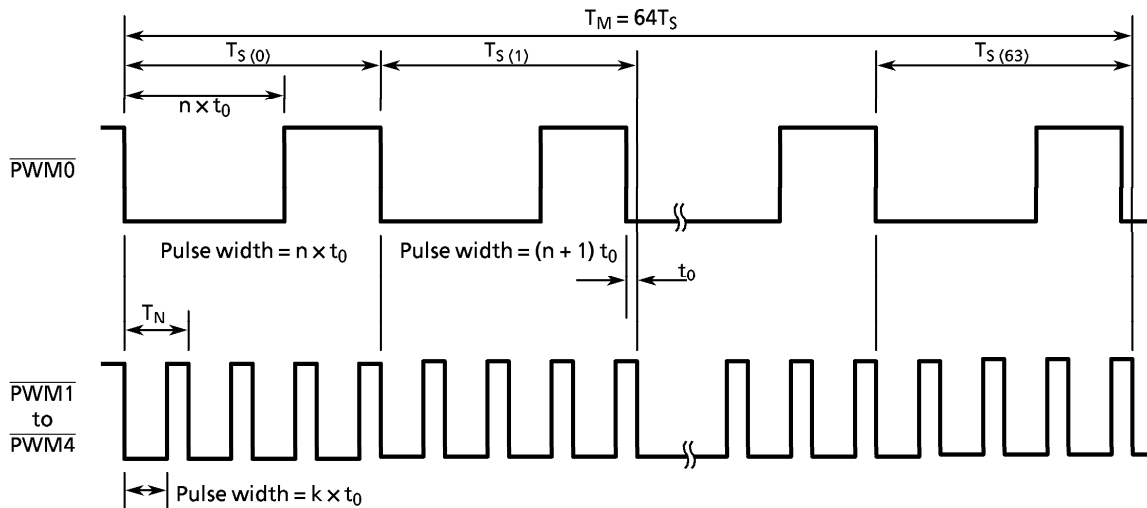
Figure 3-13. $\overline{PWM}$ Output Waveform (It is shown to the additional pulse $T_{S(1)}$ and $T_{S(63)}$ of the $\overline{PWM0}$)
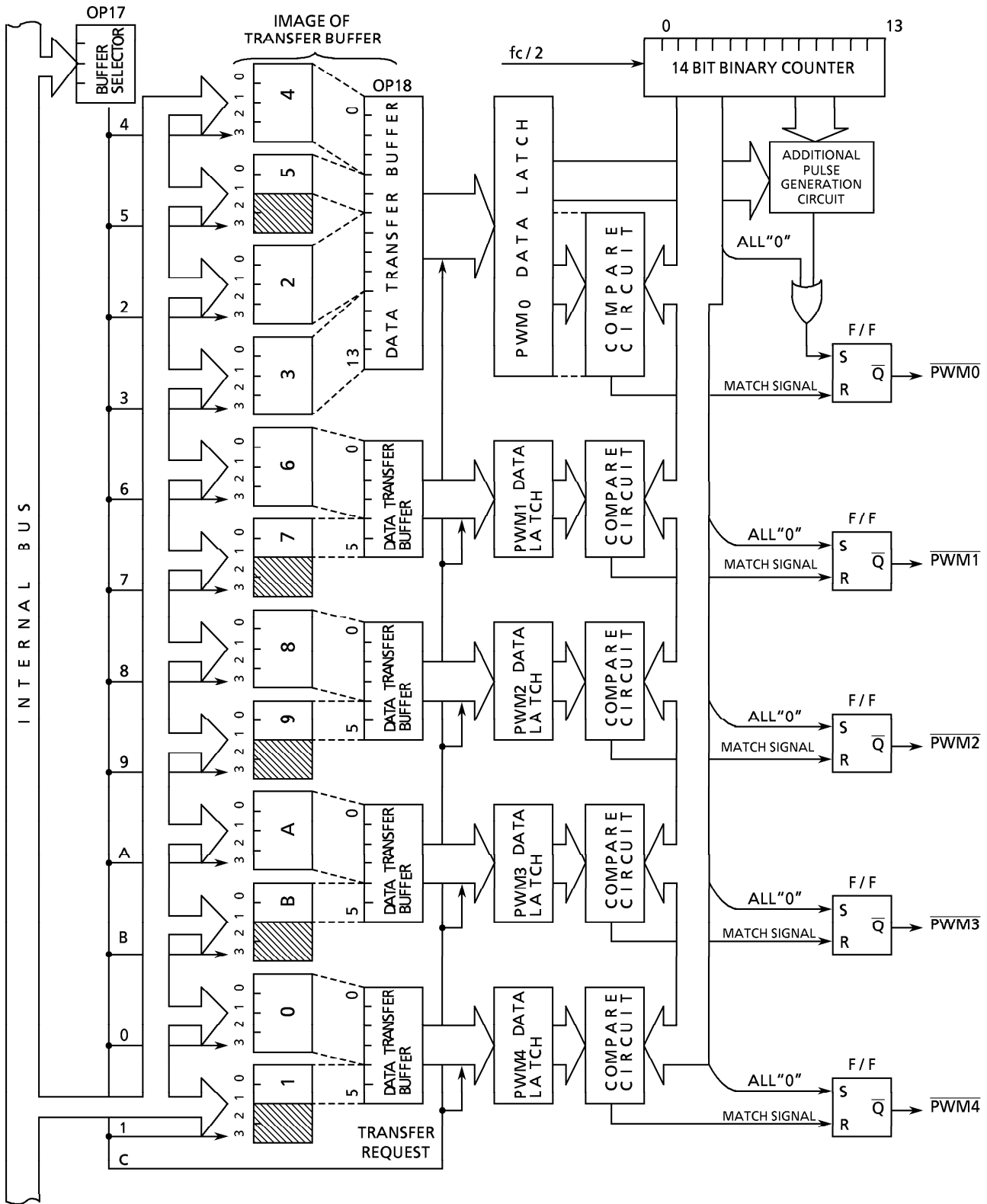
Figure 3-14. Pulse Width Modulation Circuit

Bit position of 6 vits data	Relative position of T_S where the output pulse is generated (No. i of $T_{S(I)}$ is listed)
bit0	32
bit1	16, 48
bit2	8, 24, 40, 56
bit3	4, 12, 20, 28, 36, 44, 52, 60
bit4	2, 6, 10, 14, 18, 22, 26, 30, ..., 58, 62
bit5	1, 3, 5, 7, 9, 11, 13, 15, 17, ..., 59, 61, 63

Note . When the corresponding bit is "1", it is output.

Table 3-9. Correspondence between 6 bits data and the additional pulse generated T_S periods

3.4.3 Control of PWM circuit (Data transfer)

$\overline{PWM}$ output is controlled by writing output data to a data transfer buffer (OP18). For writing, the output data are divided using the buffer selector (OP17). Buffer numbers are assigned to the data transfer buffers for these divided data, after which the data are written as shown in Table 3-10.

① The number of the transfer buffer to which the data are to be written is written to the buffer selector (OP17).
② The corresponding PWM data are written to the selected buffer (OP18).
③ Operations ① and ② are repeated, continuously writing data to the transfer buffer.
④ When all of the output data have been written. "C_H" is written to the buffer selector.

While the output data are being writen to the transfer buffer, the previously written data are being output. For $\overline{PWM0}$ output, switching to $\overline{PWM}$ output occurs at a maximum of 2^{15}/fc [s] (at 4 MHz, 8192fs) after "C_H" is written to the buffer selector. For $\overline{PWM1}$ through $\overline{PWM4}$ output data switching, this requires 2^9/fc [s] (at 4 MHz, 128 μs).

Buffer Number (OP17)	Correspondence to bit (OP18)		Mode	PWM Output
0	Bit of PWM4 transfer buffer	3 to 0	Write	Preceding data
1	Bit of PWM4 transfer buffer	5 to 4	Write	Preceding data
2	Bit of PWM0 transfer buffer	9 to 6	Write	Preceding data
3	Bit of PWM0 transfer buffer	13 to 10	Write	Preceding data
4	Bit of PWM0 transfer buffer	3 to 0	Write	Preceding data
5	Bit of PWM0 transfer buffer	5 to 4	Write	Preceding data
6	Bit of PWM1 transfer buffer	3 to 0	Write	Preceding data
7	Bit of PWM1 transfer buffer	5 to 4	Write	Preceding data
8	Bit of PWM2 transfer buffer	3 to 0	Write	Preceding data
9	Bit of PWM2 transfer buffer	5 to 4	Write	Preceding data
A	Bit of PWM3 transfer buffer	3 to 0	Write	Preceding data
B	Bit of PWM3 transfer buffer	5 to 4	Write	Preceding data
C	None		Transfer	Present data

Table 3-10. The bit and Buffer number of data transfer Buffer

Notice of ROM code release for masked products

When releasing ROM code for mask products, please take notice as follows,

(1) The area of program and program/fixed data

- Fill the data "FF_H" at all addresses of unused area.

(2) The area of character data

- Load the character data at the address 2000_H to $217F_H$.
- Fill the data "FF_H" at all addresses of unused characters.

(3) The area between the end of program/fixed data and the begin of display data table

- Fill the data "FF_H" at all addresses.
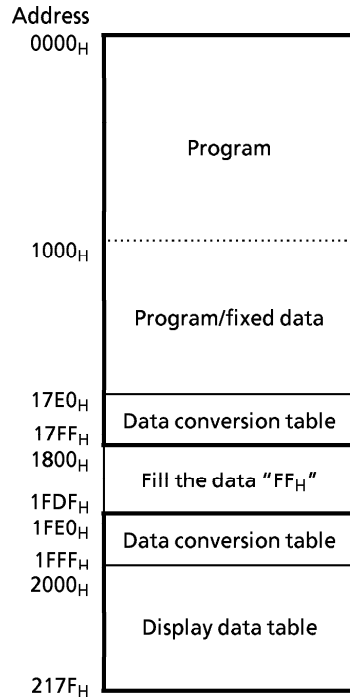
```
           Address
           0000H  ┌─────────────────┐
                  │                 │
                  │                 │
                  │    Program      │
                  │                 │
           1000H  ├ ─ ─ ─ ─ ─ ─ ─ ─ ┤
                  │                 │
                  │ Program/fixed   │
                  │     data        │
                  │                 │
           17E0H  ├─────────────────┤
           17FFH  │Data conversion table│
           1800H  ├─────────────────┤
                  │Fill the data "FFH"│
           1FDFH  ├─────────────────┤
           1FE0H  │Data conversion table│
           1FFFH  ├─────────────────┤
           2000H  │                 │
                  │ Display data table│
                  │                 │
           217FH  └─────────────────┘
                       47C635
```

INPUT / OUTPUT CIRCUITRY

(1) Control pins

Input/output circuitries of the 47C635 control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	Input Output		Resonator connecting pins $R \quad = 1\,k\Omega$ (typ.) $R_f \quad = 1.5\,M\Omega$ (typ.) $R_O \quad = 2\,k\Omega$ (typ.)
$\overline{RESET}$	Input		Hysteresis input Contained pull-up resistor $R_{IN} = 220\,k\Omega$ (typ.) $R \quad = 1\,k\Omega$ (typ.)
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)		Hysteresis input (Sense input) $R = 1\,k\Omega$ (typ.)
TEST	Input		Contained pull-down resistor $R_{IN} = 70\,k\Omega$ (typ.) $R \quad = 1\,k\Omega$ (typ.)
OSC1 OSC2	Input Output		Oscilation terminals for DOS $R \quad = 1\,k\Omega$ (typ.) $R_f \quad = 1.5\,M\Omega$ (typ.) $R_0 \quad = 2\,k\Omega$ (typ.)
$\overline{HD}$ $\overline{VD}$	Input		Synchronous signal input Hysteresis input $R = 1\,k\Omega$ (typ.)

(2) I/O ports

The input/output circuitries of the 47C635 I/O ports are shown below, designated by code (PC).

PORT	I/O	INPUT/OUTPUT CIRCUITRY (code : PC)	REMARKS
K0	Input		Pull-down resistor R_{IN} = 70 kΩ (typ.) R = 1 kΩ (typ.)
P1 P2	Output		Sink open drain Initial "Hi-Z" High drive current I_{OL} = 20 mA (typ.)
R3	I/O		Push-pull output Initial "High" R = 1 kΩ (typ.)
R4 R5 RA	I/O		Tri-state I/O Initial "Hi-Z" R = 1 kΩ (typ.)
R6 R7	I/O		Sink open drain Initial "Hi-Z" and Comparator input (R70 pin) R = 1 kΩ (typ.)
R8 R9	I/O		Sink open drain Initial "Hi-Z" Hysteresis input R = 1 kΩ (typ.)

ELECTRICAL CHARACTERISTICS

| ABSOLUTE MAXIMUM RATINGS | ($V_{SS} = 0$ V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		-0.3 to 7	V
Input Voltage	V_{IN}		-0.3 to $V_{DD} + 0.3$	V
Output Voltage	V_{OUT1}	Except sink open drain pin, but include port R7	-0.3 to $V_{DD} + 0.3$	V
	V_{OUT2}	Sink open drain pin except R7 port	-0.3 to 10	
Output Current (Per 1 pin)	I_{OUT1}	Ports P1, P2	30	mA
	I_{OUT2}	Ports R3, R6, R7, R8, R9	3.2	
Output Current (Total)	ΣI_{OUT1}	Ports P1, P2	120	mA
Power Dissipation	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10 s)	°C
Storage Temperature	T_{stg}		-55 to 125	°C
Operating Temperature	T_{opr}		-30 to 70	°C

| RECOMMENDED OPERATING CONDITIONS | ($V_{SS} = 0$ V, $T_{opr} = -30$ to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITION	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	4.5	6.0	V
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.1$	
Clock Frequency	f_c	XIN, XOUT		0.4	4.2	MHz
	f_{OSD}	OSC1, OSC2		–	6.0	

Note . Input Voltage V_{IH3}, V_{IL3}: in the HOLD operating mode.

D.C. CHARACTERISTICS ($V_{SS} = 0$ V, $T_{opr} = -30$ to $70\,°C$)

PARAMETER	SYMBOL	PINS	CONDITION	Min.	Typ.	Max	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	$V_{DD} = 5.5$ V,	—	—	± 2	μA
	I_{IN2}	Port R (open drain)	$V_{IN} = 5.5$ V / 0 V				
Input Low Current	I_{IL}	Port R (push – pull)	$V_{DD} = 5.5$ V, $V_{IN} = 0.4$ V	—	—	– 2	mA
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Tri-state port Ports R3, R6, R8, R9 (open drain)	$V_{DD} = 5.5$ V, $V_{OUT} = 5.5$ V	—	—	± 2	μA
Output High Voltage	V_{OH1}	Port R (push-pull)	$V_{DD} = 4.5$ V, $I_{OH} = -200\,\mu$A	2.4	—	—	V
	V_{OH2}	Port R (tri-state), OSD outputs	$V_{DD} = 4.5$ V, $I_{OH} = -0.7$ mA	4.1	—	—	
Output Low Voltage	V_{OL1}	Ports R3, R6-R9	$V_{DD} = 4.5$ V, $I_{OL} = 1.6$ mA	—	—	0.4	V
	V_{OL2}	Port R (tri-state), OSD outputs	$V_{DD} = 4.5$ V, $I_{OL} = 0.7$ mA				
Output Low Current	I_{OL}	Ports P1, P2	$V_{DD} = 4.5$ V, $V_{OL} = 1.0$ V	—	20	—	mA
Supply Current (in the Normal mode)	I_{DD}		$V_{DD} = 5.5$ V, fc = 4 MHz	—	3	6	mA
Supply Current (in the HOLD mode)	I_{DDH}		$V_{DD} = 5.5$ V	—	0.5	10	μA

Note 1. Typ. values show those at $T_{opr} = 25\,°C$, $V_{DD} = 5$ V.
Note 2. Input Current I_{IN1} : The current through resistor is not included, when the pull-up/pull-down resistor is contained.
Note 3. Supply Current : $V_{IN} = 5.3$ V / 0.2 V
The K0 port is open when the pull-up / pull-down resistor is contained.
The voltage applied to the R port is within the valid range V_{IL} or V_{IH}.

A / D CONVERTER CHARACTERISTICS

PARAMETER	SYMBOL	PINS	CONDITION	Min.	Typ.	Max.	UNIT
Analog input voltage	V_{AIN}	CIN		V_{SS}	—	V_{DD}	V
A / D conversion error	—			—	—	$\pm \frac{1}{4}$	LSB

A.C. CHARACTERISTICS	$(V_{SS} = 0$ V, $V_{DD} = 4.5$ to 6.0 V, $T_{opr} = -30$ to $70\,°C)$

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		1.9	–	20	μs
High level Clock Pulse Width	t_{WCH}	For external clock operation	80	–	–	ns
Low level Clock Pulse Width	t_{WCL}					
Shift data Hold Time	t_{SDH}		0.5 tcy – 300	–	–	ns

Note.   Shift data Hold Time :

External circuit for $\overline{SCK}$ pin and SO pin.   Serial port (completion of transmission)
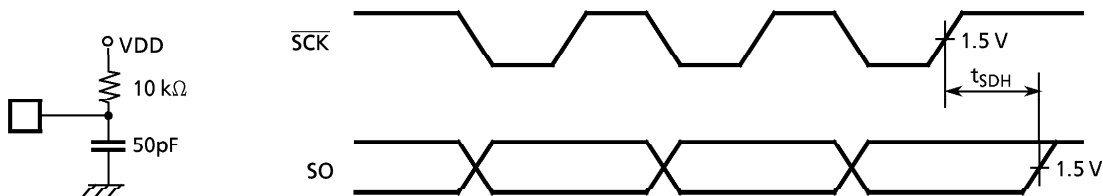
RECOMMENDED OSCILLATING CONDITIONS $(V_{SS} = 0$ V, $V_{DD} = 4.5$ to 6.0 V, $T_{opr} = -30$ to $70\,°C)$

(1) 4 MHz
Ceramic Resonator
        CSA4.00MG   (MURATA) $C_{XIN} = C_{XOUT} = 30$ pF
        KBR-4.00MS   (KYOCERA) $C_{XIN} = C_{XOUT} = 30$ pF
Crystal Oscillator
        204B-6F 4.0000   (TOYOCOM) $C_{XIN} = C_{XOUT} = 20$ pF
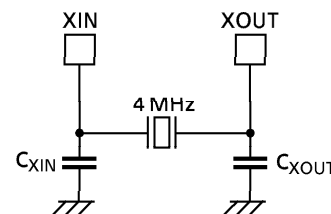
(2) 400 kHz
Ceramic Resonator
        CSB400B   (MURATA) $C_{XIN} = C_{XOUT} = 220$ pF,
                                       $R_{XOUT} = 6.8$ kΩ
        KBR-400B   (KYOCERA) $C_{XIN} = C_{XOUT} = 100$ pF,
                                       $R_{XOUT} = 10$ kΩ
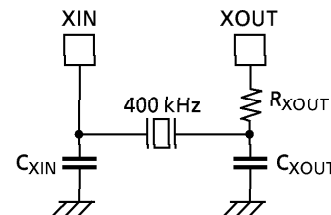
(3) 6 MHz (for DOS)
LC Resonator
        TBEKSES-30361FBY   (TOKO)
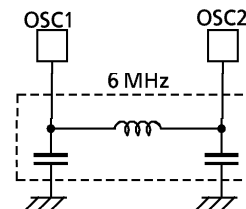
Note :   An electrical shield by metal shield plate on the surface of the IC package should be recommendable in order to prevent the device from the high electric fieldstress applied from CRT (Cathode Ray Tube) for continuous reliable operation.

TYPICAL CHARACTERISTICS

R – Ta K0 port
R (kΩ)
$V_{DD} = 5.5$ V
100
50
0
−40 0 40 80
Ta (°C)

R – Ta $\overline{RESET}$ pin
R (kΩ)
$V_{DD} = 5.5$ V
400
300
200
100
0
−40 0 40 80
Ta (°C)

$I_{OH} – V_{OH}$ CMOS R port
I_{OH} (μA)
$V_{DD} = 4.5$ V
Ta = 25 °C
−400
−300
−200
−100
0
2 4 6
V_{OH} (V)

$I_{IL} – V_{IN}$ CMOS R port
I_{IL} (μA)
$V_{DD} = 5.5$ V
Ta = 25 °C
−800
−600
−400
−200
0
2 4 6
V_{IN} (V)

$I_{OH} – V_{OH}$ TRI-STATE port
I_{OH} (mA)
$V_{DD} = 4.5$ V
Ta = 25 °C
−20
−15
−10
−5
0
2 4 6
V_{OH} (V)

$I_{OL} – V_{OL}$ R port
I_{OL} (mA)
$V_{DD} = 4.5$ V
Ta = 25 °C
8
6
4
2
0
0.4 0.8 1.2
V_{OL} (V)

$I_{OL} – V_{OL}$ P1, P2 port
I_{OL} (mA)
$V_{DD} = 4.5$ V
Ta = 25 °C
40
30
20
10
0
0.4 0.8 1.2
V_{OL} (V)

$I_{OL} – V_{OL}$ TRI-STATE port
I_{OL} (mA)
$V_{DD} = 4.5$ V
Ta = 25 °C
8
6
4
2
0
0.4 0.8 1.2
V_{OL} (V)

$I_{DD} – V_{DD}$
I_{DD} (mA)
Ta = 25 °C
4
3
2
1
0
fc = 4 MHz
fc = 400 kHz
3 5 7
V_{DD} (V)

$I_{DD} – fc$
I_{DD} (mA)
$V_{DD} = 5.5$ V
Ta = 25 °C
4
3
2
1
0
0.1 0.4 1 4 10
fc (MHz)

Operating area
fc (MHz)
Ta = −30 to 70 °C
(Normal mode)
8
6
4
2
0
2 4 6
V_{DD} (V)
(▨ : OSD operation)