CB65000 Series

HCMOS8D 0.18µm Standard Cells Family

FEATURE

- 0.18 micron drawn, six layers of metal connected by fully stackable vias and contacts, Shallow Trench Isolation, low resistance, salicided active areas and gates. Deep UV lithography.
- 1.8 V optimized High Performance and Low Leakage transistors with 3.3 V I/O and supply interface capability.
- Average gate density: 85K/mm^2, plus low power consumption of 30nanoWatt/Gate/MHz/ Stdload.
- Two input NAND delay of 35ps with High Performane transistor and 60ps with Low Leakage transistor.
- Library available in commercial, industrial and military temperature range. Power supply ranging from 1.2V and 1.95V for Core (according to JESD 8-7 specification) and between 3.0V and 3.6V for I/Os (alligned with JESD 8-A specification).
- Broad I/O functionality including:
- Low Voltage CMOS.
- Low Voltage TTL,HSTL, SSTL.
- AGP 2X and 4X, USB, PCI, LVDS I/O interfaces are also available.
- Drive capability up to 8 mA per buffer with slew rate control, current spike suppression impedance matching, and process compensation capability to reduce delay variation.
- Designs easily portable from previous generations of CB55000 with an average factor 2 density increase, 30% speed improvement
- and 2.5 power reduction at respective nominal voltages.
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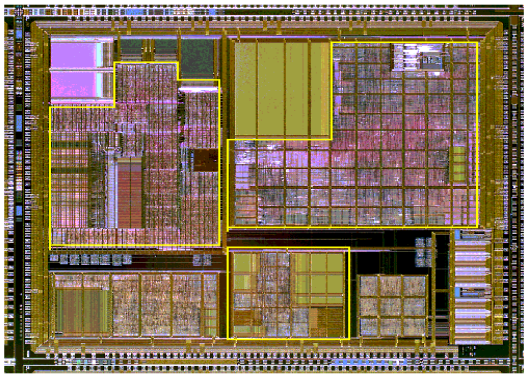
- Generators to support Single Port, Dual port and multiple Port RAM, and ROMs with BIST options.
- Extensive embedded function library including ST DSP and micro-cores, third-party IPs, Synopsys and Mentor Inventra synthetic libraries ideally suited for complete System On Chip fast integration .
- Embedded DRAM Capability



CB65000 Super Integration

Cost Effective Product

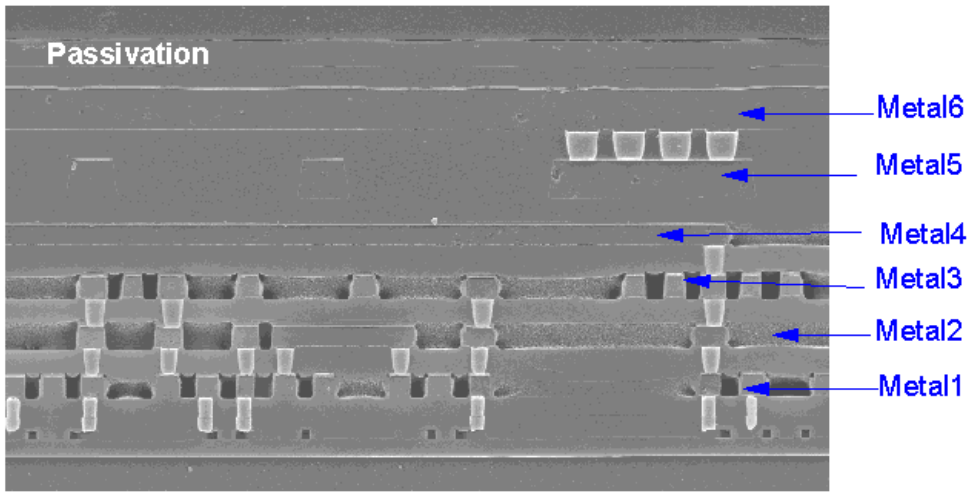
- Architecture partitioning
- Trouble-free integration
- Application-specific

Your Product is Unique

- User specified cell integration
- Design confidentiality
- IP fully re-usable

- 80 µm pitch linear and 50 µm staggered pad libraries.
- Fully independent power and ground configuration for core and I/Os supported.
- I/O ring capability up to 1500 pads.
- Latch-up trigger current > ± 500 mA. ESD protection above 4 kV in H.B.M.
- Oscillators and PLLs for wide frequency spectrum.
- Broad range of more than 600 SSI cells.
- Design for test features including IEEE 1149.1 JTAG Boundary Scan architecture.
- Synopsys, Cadence and Mentor based design systems with interface from multiple workstations.
- Broad range of packaging solutions, including PBGA, LBGA, SBGA, HPBGA, TQFP, PQFP, PLCC up to 1000 pins with enhanced power dissipation options.
- 1.25 GigaHertzGigabit DLL technique.

Figure 1. Process cross section and Interconnect perspective view



1 GENERAL DESCRIPTION

The CB65000 standard cell series uses a high performance, low-voltage, 0.18 µm drawn, six metal levels, high density and high speed HCMOS8D process.

With an average routed gate density of 85,000 gates/mm^2, the CB65000 family allows the integration of up to 30 million equivalent gates and is ideal for high-complexity or high-performance devices for computer, telecommunication and consumer products.

With a gate delay of 35 ps with High Performance transistor and 60 ps with Low Leakage transistor (for a 2-input NAND gate at fan-out 1), the library meets the most demanding speed requirements in telecommunication and computer application designs today.

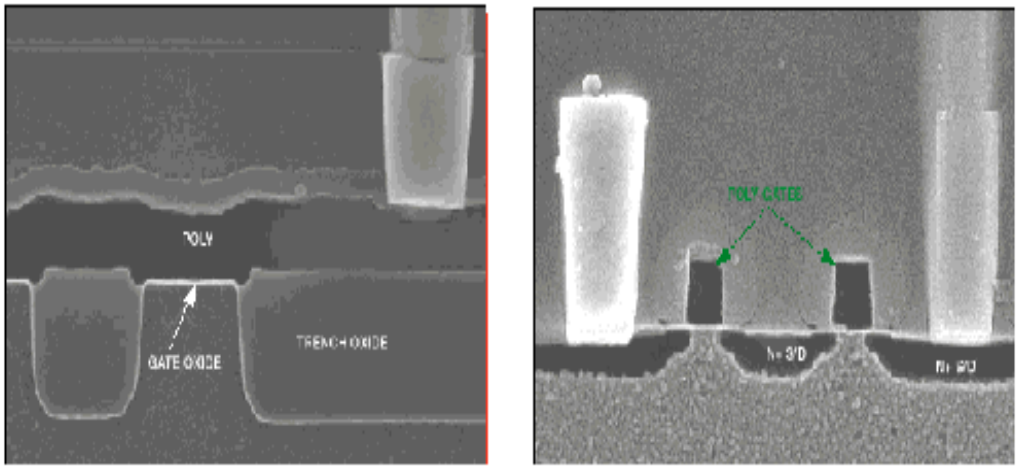
Optimized for 1.8 V operation, the library features a power consumption of less than 35 nW/Gate/MHz (High Performance; fan-out=1) and 25 nW/Gate/MHz (Low Leakage; fan-out=1) at 1.8 V.

The I/O buffers can be fully configured for both 1.8 V and 3.3 V interface options, with several high speed buffer types available. These include: low voltage differential (LVDS) I/Os, PCI, AGP, USB, LVTTL, LVCMOS and SSTL.

The pad pitch down to 50 µm, in a staggered arrangement, meets the requirements of high pin-count devices which tend to become pad-limited at such library densities. For very high pin-count ICs, advanced solutions such as Ball Grid Array packages are available.

New packaging solutions using a flip-chip approach are currently being developed.

Figure 2. HCMOS8D Front end cross section



2 TECHNOLOGY OVERVIEW

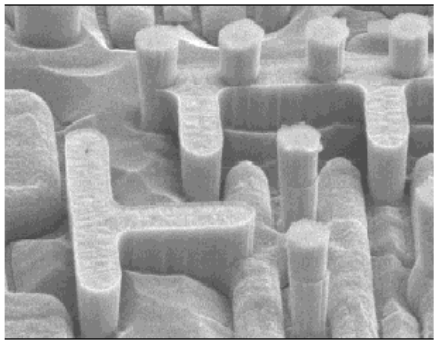
The advanced HCMOS8D transistor architecture: at 0.18 µm, very thin gate oxide: 35 Amstrong, optimized threshold voltages and salicided source, drain, and gate leads to intrinsically high performances in both N channel and P channel driving currents.

The major scaling factor is obtained through deep UV lithography at most masking levels, making sub-micron pitch a reality.

Further integration in the process front-end comes from the use of the Shallow Trench Isolation process between active regions, both improving density and planarity of transistors. In order to allow full utilization of such transistor density, up to 6 levels of metal are made available for routing.

The local interconnection level made in Tungsten, allows short interconnection at silicon layer improving memory and cell density., while all the six metal levels are of low resistivity aluminum for long range interconnection and power distribution.

Figure 3. HCMOS8D Local Interconnect

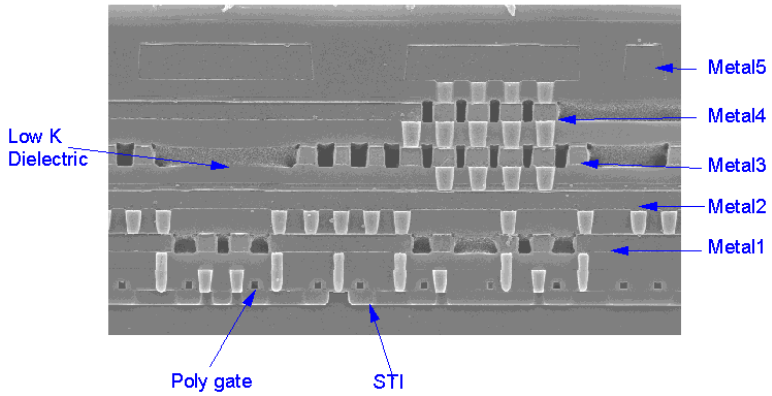


The thick inter-level dielectric is completely planarized by Chemical Mechanical Polishing, which provides defect-free isolation between stripes within the same as well as between different levels.

Usage of Tungsten plugs at contacts and vias allows extremely dense and reliable interconnection between metal layers. These vias and contacts are fully stackable, providing a direct vertical electrical connection from the active level up to the sixth metal level. This efficient interconnect scheme makes routing fast and easy, as well as having a very positive impact on high gate count, random-logic blocks density and routability.

The combination of both high drive and dense transistors, easily interconnected with up to six fine-pitch metal levels and isolated by thick and low K dielectric leads to an optimum gate density, with low parasitic resistance and capacitance. This results in very short interconnected gate delay and minimized power consumption.

Figure 4.



3 LIBRARY

The CB55000 library is organized into three categories:

– SSI cell library
– I/O cell library
– Macrofunctions

3.1 SSI Cell Library Overview

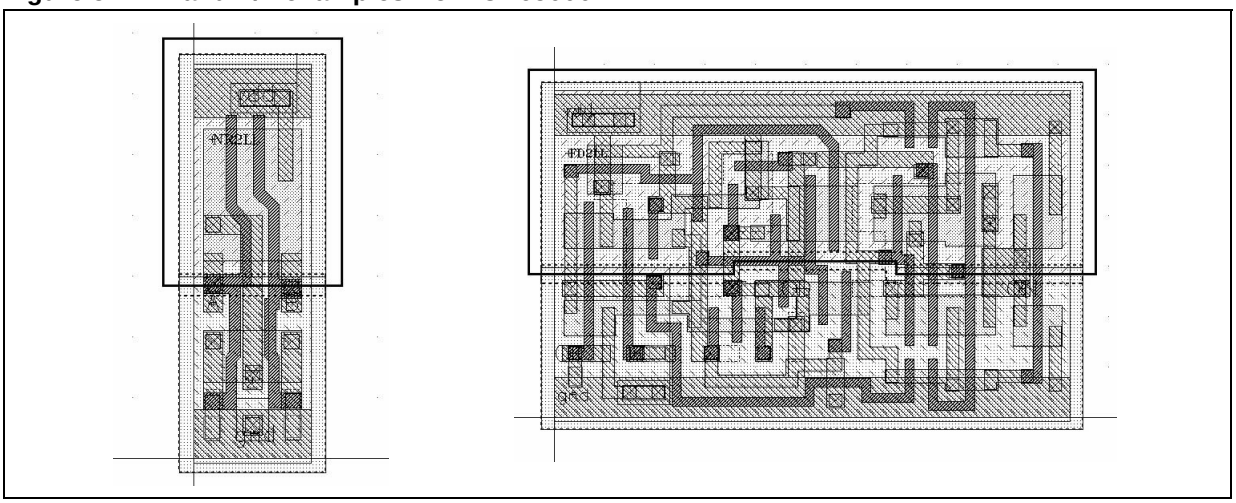
The design of the CB65000 family has been optimized to allow extremely high density, high speed and low power designs. For these reasons, a wide range of cells with different ranges of driving capabilities are available in the library.

The library cells have been optimized in terms of functional and electrical parameters, in order to have:

– Good balancing
– Maximum speed
– Optimum threshold voltage
– Symmetric V_{dd}/V_{ss} noise margins
– Minimum power-speed value

The geometrical aspect of the cells is configured to allow an extremely dense design, fully exploiting the features of the Place and Route tool in terms of horizontal and vertical routing grids. For Place and Route, up to six layers of metal are utilized; the firsts four layers fully available for signal routing, while the fifth and sixth to power distribution, clock bussing and routing.

Figure 5. NR2 and F/F examples from CB65000



3.2 Core Logic

The propagation delays shown in CB65000 data book are given for worst case processing at 1.55V and 125°C and will be provided in the design while power data are referred to a fast process model at 1.95V and -40°C. However, there are additional factors that affect the delay characteristics of the cells. These include: loading due to fanout and interconnect routing, supply voltage, junction temperature of the device, processing tolerance and input signal transition time.

Prior to physical layout, the design system can estimate the delays associated with any critical path. The impact of the placement and routing can be accurately RC back-annotated from the layout for final simulations of critical timing. The median effects on the cells delay of junction temperature (Kt coefficient) and supply voltage (Kv coefficient) are extracted from real Silicon data.

3.3 I/O Buffer Libraries

Two basic buffer libraries are offered with CB65000, one 80 µm pad in line pitch library and one 50 µm staggered pad library to support pad limited designs.

Apart from standard ESD and latch-up protections present in each I/O, a proprietary clamp within each power supply provides proper paths to all types of ESD discharges, efficiently protecting the I/Os. As a result, the buffers withstand more than 4 kV ESD according to Mil 883C Human Body Model specification.

In order to limit switching noise and keep a fixed buffer delay, independent of process, supply voltage and temperature, compensated active slew rate buffers can be selected, providing a fixed and stable dI/dt.

In order to interface with 3.3 V application (from 3.0 up to 3.6 V), a wide range of 3.3 V capable input/output buffers (mixable with standard 1.8V ones) can be chosen. In this case the 3.3 V rail in the chip periphery must be powered through a 3.3 V external supply.

True 5 volt tolerant input buffer is also available to allow different power level managment.

Dedicated I/Os for special applications have developed, like :

– UDMA for Hard Disk Interface
– LVDS and PECL for Telecom Standard
– PCI for PC Peripheral Interface
– USB for Universal Serial Interface

3.4 I/O Test Interface

The I/O cells have a dedicated test interface to facilitate parametric and Iddq testing of devices. This test interface connects standard core signals or dedicated test signals to the I/O cells allowing all output buffers to be driven high, low or put into tri-state regardless of the state of the internal logic.

This greatly simplifies parametric testing of the device and also assisting customers who wish to use this feature during board testing. Note that all output buffers can be tri-stated by this function including buffers that normally do not tri-state.

This test function also turns off all pull down resistors, shuts down all differential receivers and converts them into standard CMOS receivers. This allows Iddq test methodologies to be employed in a very efficient way, avoiding unneeded circuit overhead.

3.5 Macrocells

The CB65000 series has internal macrocells that are robust in variety and performance. The cell selection has been driven by the need of Synthesis and HDL-based design techniques. This offering is rich in buffers, complex combination cells and multi-power drive cells, which allow the Synthesis tool to create a netlist compatible with the requirements of Place and Route tools.

Macrofunctions are a series of soft-macros facilitating quick capture of large functional blocks and are available for such functions as counters, shift registers and adders. Macrofunctions are implemented at layout by utilizing macrocells and interconnecting to create the logic function.

3.5.1 Module generators

A series of module generators using compiled cell generation techniques are available to support a range of megacells. These modules enable the designer to choose individual parameters in order to create a compiled cell, which meets the specific application requirements. These include ROM, single and dual port RAM, multiport RAM and FIFO, some of them specifically optimized for speed and for power. All memories have a complete standby mode where current consumption is limited to process leakage.

High Density Memories are also available to fully exploiting the technology capability.

Table 1. List of module generators

Generator	Description	Bit (Min.)	Kbit (Max)	Word width (Max.)
Romd	High speed Sync. Diffusion ROM	128	2048	64
RO8L	Low Power, High Density Metal ROM (M2 programming)	8	4096	64
SPS2HD	High speed Sync. High Density Single port RAM	64	512	64
SPS4	Small cuts Sync. Low power Single port RAM	2	16	128
SPS5A	Low Power High speed Async. Single port RAM	1000	512	64
SPS6	High Density, Multipage, Low power High speed Single port RAM	1000	4096	128 + byte write
SP8D	Low Power High Density Single Poert RAM	8	2096	64
DPR2	High speed Sync. Dual port RAM	64	256	64
DP8D	Low Power High Density Sync. Dual Port RAM	8	512	64
DP8E	Low Power Async. Register File	8	8	128
FIFO	High speed	8	4	32

– Typical case : 1.8V & 25°C ; Worst case : 1.55V & 125°C .

– 2 Characterization range : [1.55V , 1.95V] & [1.2V , 1.6V]

3.5.2 MicroLibrary & I.P.s

MicroLibrary includes an extensive portfolio of microcores and application specific I.P.s; provided through both internal developments and partners licensing agreements.

A short list of this portfolio consists of:

- General purpose macro functions.
  - Microcores (8,16,32 bits) like:8051,ST10,ST20,SH4,ARM7TDMI,
  - DSP:D950,ST100,
  - PLL, Frequency synthesizer, Comparators,
  - DAC,ADC (8,10,16 bits).
- Application specific I.P.s for:
  - Data communications (10/100 ETH MAC & PHY, Gigabit,..),
  - Telecommunication (622MHz phase aligner, clock recovery),
  - Computer and peripherals (PCI,USB,SSCI,RAMDAC,IEEE1394,FiberChannel),
  - Audio (CODEC,..).

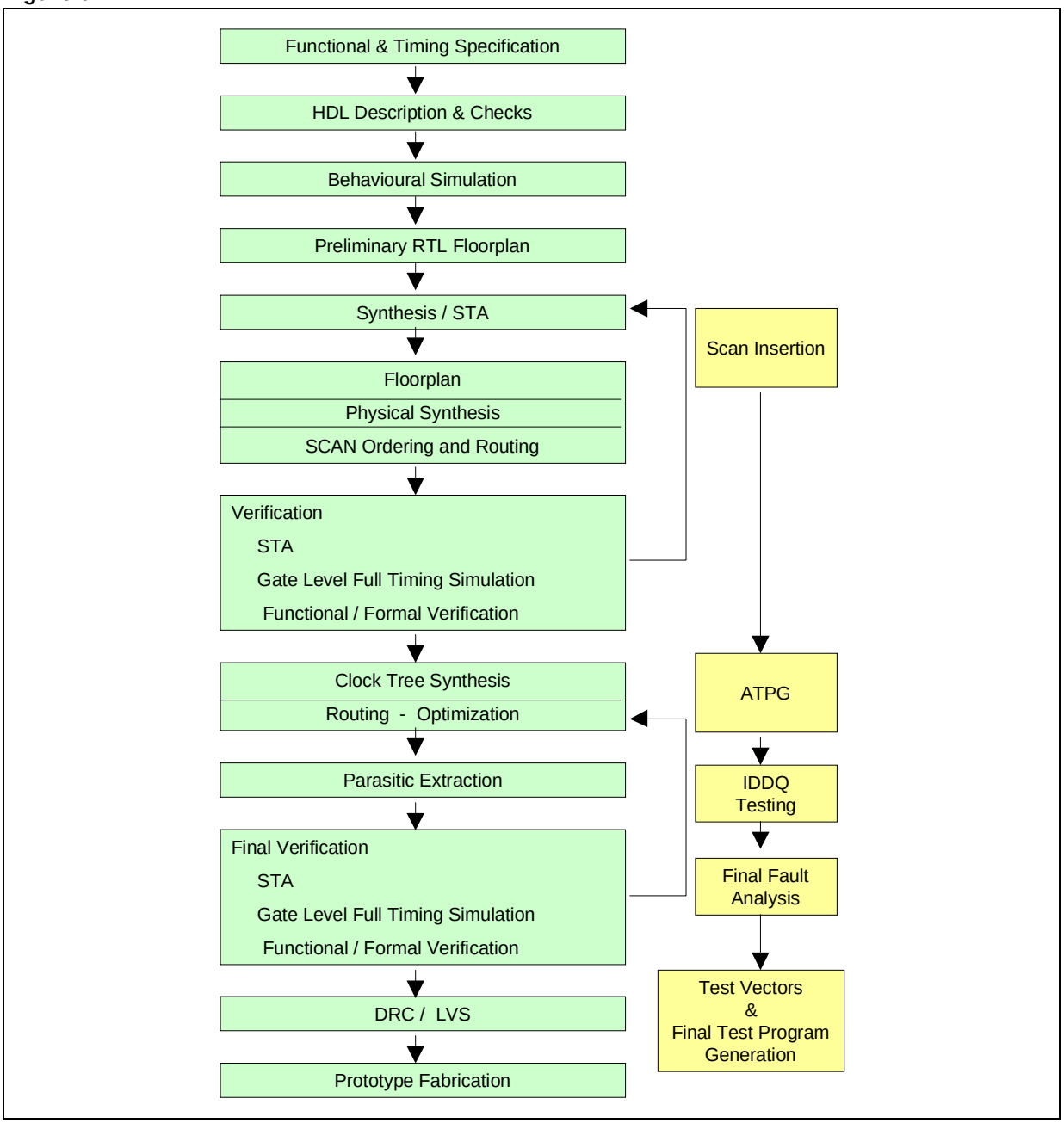
4 DESIGN METHODOLOGY

STMicrolectronics (STM) ASIC design flow is intended for high performance, high complexity submicron ASIC designs. 3rd parties tools from leading EDA vendors such as Synopsys, Cadence, Mentor Graphics and STM proprietary systems are integrated into a framework free design environment that efficiently supports all design phases.

A hierarchical design methodology with a FastLoop, between floorplanning timing-driven placement and synthesis/static timing analysis, guarantees a fast timing prediction and closure after routing.

Other features such as hierarchical Clock tree synthesis, advanced test methodology, formal verification, 3D parasitic extraction, Crosstalk analysis, IP-reuse, qualifies the STM ASIC design flow as one of the industry's leading solutions for today's and tomorrow's complex designs.

Figure 6.



5 DESIGN FOR TESTABILITY

The test time and cost for ASIC testing increases exponentially as the complexity and size of the ASIC grows. Using a *design-for-testability* methodology allows large, more complex ASICs to be efficiently and economically tested.

At system level, STMicroelectronics fully supports IEEE 1149.1; the I/O structure utilized in this family is completely compatible. Several types of core scan cells are provided in the CB55000 Series library. Examples include FDxS/FJKxS edge sensitive and LDxS level sensitive cells. Non-overlapping clock generator macros are also available.

Test coverage and reliability are further supported by IDDQ (quiescent current) testing; all blocks are designed to be “IDDQable” so that anomalous leakage due to metal bridging and dielectric defects can be screened using proper set of vectors extracted from the test patterns.

For parametric and Iddq testing, the I/O cells contain a dedicated test interface as described previously (see Section 3.4 ‘I/O Test Interface’ on page 6).

6 ELECTRICAL SPECIFICATION

Table 2. General Interface Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	Note
Vdd	Core Power Supply Voltage		1.55	1.8	1.95	V	
Vdd3	I/O Power Supply Voltage		3	3.3	3.6	V	
Tj	Operating Junction Temperature		-40	25	125	°C	
I latchup	I/O Latch-Up Current		200			mA	
Vesd	Electrostatic Protection	Leakage < 1u	4000			V	1

Note 1: Human Body Model

6.1 3.3V I/O specifications

Table 3. LVTTL DC Input Specification (3V < vdd3 < 3.6V)

	Parameter	Test Conditions	Min	Typ	Max	Unit
Vil	Low Level Input Voltage				0.8	V
Vih	High Level Input Voltage		2			V
Vhyst	Schmitt Trigger Hysteresis		0.4			V

Table 4. LVTTL DC Output Specification (3V < vdd3 < 3.6V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	Note
Vol	Low Level Output Voltage	Iol = XmA			0.2	V	1
Voh	High Level Output Voltage	Ioh = -XmA	2.8			V	1

Note 1: X is source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.

Table 5. Pullup & Pulldown Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	Note
Ipu	Pullul current	Vi = 0V	40	60	110	uA	1
Ipd	Pulldown current	Vi = vdd3	30	60	110	uA	1
Rup	Equivalent pull-up resistance	Vi = 0V		50		Kohm	
Rpd	Equivalent pull-down resistance	Vi = vdd3		50		Kohm	

Note 1 : Min condition: vdd3 = 3V, 125°C, min process. Max condition : vdd3 = 3.6V, -40°C, fast process.

Table 6. IDDQ Current

OUTPUT

		Typ/25°C/vdd3=3.3V Vdd=1.8V		Fast/25°C/vdd3=3.6V Vdd=1.95V		Fast/125°C/ vdd3=3.6V Vdd=1.95V			Note
	VA	0	1.8	0	1.95	0	1.95	V	
bt2trp_tc	I(vdd3)	0.3	0.4	2.2	3.3	30	40	nA	
	I(vdd)	0.3	0.3	2	1.5	170	140	nA	
bt4trp_tc	I(vdd3)	0.3	0.5	2.2	4.8	30	50	nA	
	I(vdd)	0.3	0.3	2	1.5	170	140	nA	
bt8trp_tc	I(vdd3)	0.35	0.9	2.2	8.5	40	90	nA	
	I(vdd)	0.35	0.3	2	1.5	170	140	nA	

INPUT

		Typ/25°C/vdd=1.8		Fast/25°C/vdd=1.95		Fast/125°C/vdd=1.95			
	VA	0	3.3	0	3.6	0	3.6	V	
clthc_tc	I(vdd)	0.1	0.05	0.5	0.2	40	20	nA	1
tlchth_tc	I(vdd)	0.2	0.15	1.3	0.7	110	50	nA	1

Note 1: In all that cases I(vdd3) is lower than 1 nA

6.2 1.8V I/O specification

Table 7. DC Input Specification (1.55V < vdd < 1.95V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Vil	Low level input voltage				0.54	V
Vih	High level input voltage		1.26			V
Vhyst	Schmitt trigger hysteresis		0.4			V

Table 8. DC OutputSpecification (1.55V < vdd < 1.95V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	Note
Vol	Low level output voltage	Iol = XmA			0.11	V	1
Voh	High level output voltage	Ioh = -XmA	1.45			V	1

Note 1 : X is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability

Table 9. Pullup & Pulldown Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	Note
Ipu	Pullul current	Vi = 0V	20	35	60	uA	1
Ipd	Pulldown current	Vi = vdd	15	35	70	uA	1
Rup	Equivalent pull-up resistance	Vi = 0V		50		Kohm	
Rpd	Equivalent pull-down resistance	Vi = vdd		50		Kohm	

Note 1 : Min condition: vdd3 = 3V, 125°C, min process. Max condition : vdd3 = 3.6V, -40°C, fast process

Table 10. IDDQ Current

OUTPUT

		Typ/25C/vdd=1.8V		Fast/25C/vdd=1.95V		Fast/125C/vdd=1.95V		
	VA	**0**	**1.8**	**0**	**1.95**	**0**	**1.95**	**V**
bt2crp	I(vdd)	0.5	0.6	2.2	2.2	225	220	nA
bt4crp	I(vdd)	0.6	0.7	2.5	2.3	280	240	nA
bt8crp	I(vdd)	1	1	3	3	390	290	nA

INPUT

	VA	**0**	**1.8**	**0**	**1.95**	**0**	**1.95**	**V**
ibuf	I(vdd)	0.08	0.07	0.4	0.3	40	30	nA
ibuf	I(vdd)	0.2	0.15	1.1	0.6	110	60	nA