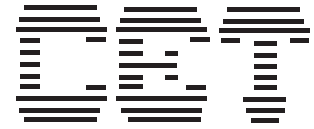


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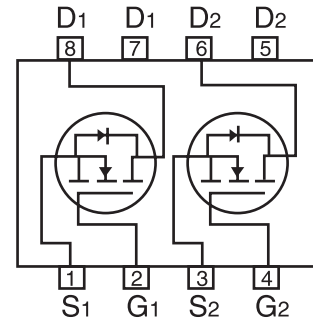
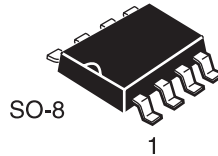
March 1998

## Dual N-Channel Enhancement Mode Field Effect Transistor

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### FEATURES

- 60V , 3.3A ,  $R_{DS(ON)}=100m\Omega$  @  $V_{GS}=10V$ .  
 $R_{DS(ON)}=200m\Omega$  @  $V_{GS}=4.5V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handing capability.
- Surface Mount Package.



### ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	VDS	60	V
Gate-Source Voltage	VGS	$\pm 20$	V
Drain Current-Continuous <sup>a</sup> @ $T_J=125^\circ\text{C}$ -Pulsed <sup>b</sup>	ID	$\pm 3.3$	A
	IDM	$\pm 10$	A
Drain-Source Diode Forward Current <sup>a</sup>	IS	1.7	A
Maximum Power Dissipation <sup>a</sup>	PD	2	W
Operating Junction and Storage Temperature Range	TJ, TSTG	-55 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
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## ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =48V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS<sup>b</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	1.4	3	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =3.3A		0.06	0.1	Ω
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =2.5A		0.08	0.2	Ω
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	10			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =3.3A		7		S
<b>DYNAMIC CHARACTERISTICS<sup>c</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V f=1.0MHz		428	560	pF
Output Capacitance	C <sub>OSS</sub>			128	170	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			28	40	pF
<b>SWITCHING CHARACTERISTICS<sup>c</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =30V, I <sub>D</sub> =1A, R <sub>L</sub> =30Ω V <sub>GEN</sub> =10V, R <sub>GEN</sub> =6Ω		7	25	ns
Rise Time	t <sub>r</sub>			3	30	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			22	50	ns
Fall Time	t <sub>f</sub>			6	40	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =30V, I <sub>D</sub> =3.3A, V <sub>GS</sub> =10V		9	30	nC
Gate-Source Charge	Q <sub>gs</sub>			2		nC
Gate-Drain Charge	Q <sub>gd</sub>			4		nC

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## ELECTRICAL CHARACTERISTICS ( $T_A=25^\circ\text{C}$ unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>b</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0\text{V}, I_S = 1.7\text{A}$		0.8	1.2	V

### Notes

- a. Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$ .
- b. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- c. Guaranteed by design, not subject to production testing.

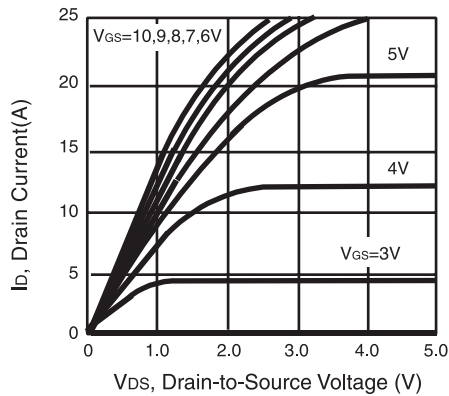


Figure 1. Output Characteristics

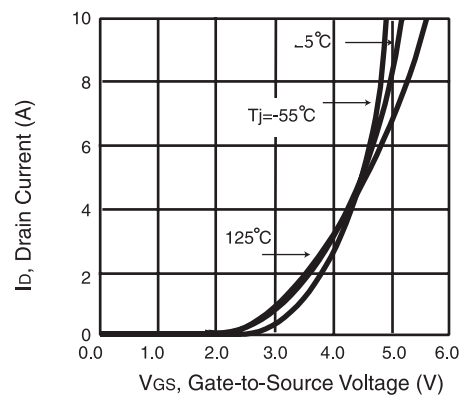


Figure 2. Transfer Characteristics

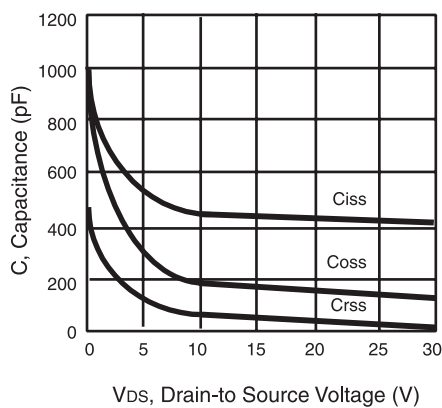


Figure 3. Capacitance

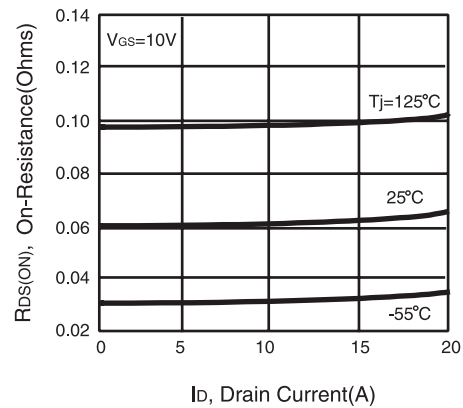
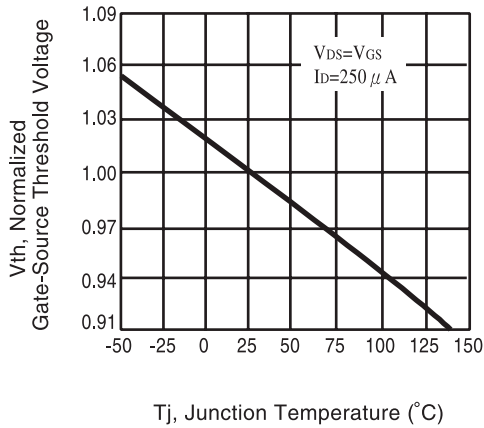
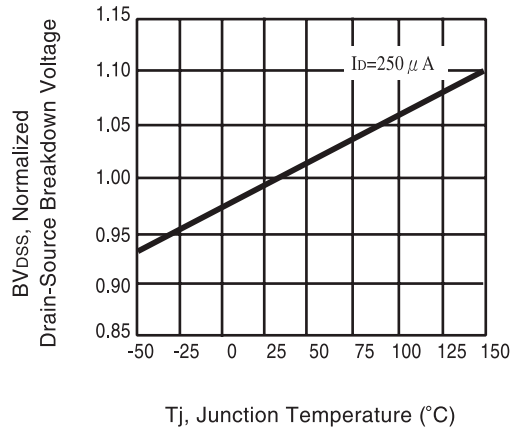


Figure 4. On-Resistance Variation with Drain Current and Temperature

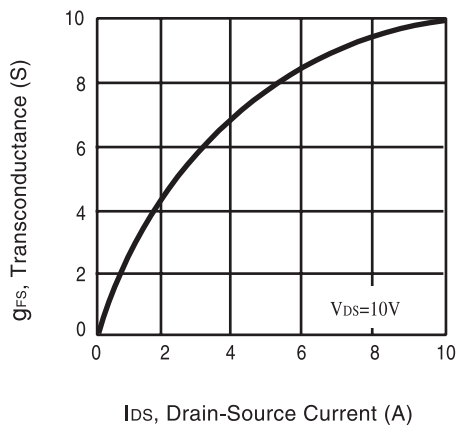
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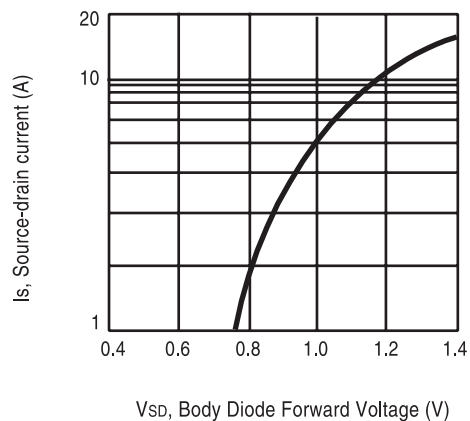
**Figure 5. Gate Threshold Variation with Temperature**



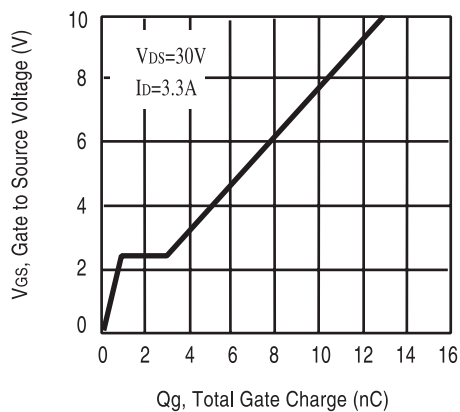
**Figure 6. Breakdown Voltage Variation with Temperature**



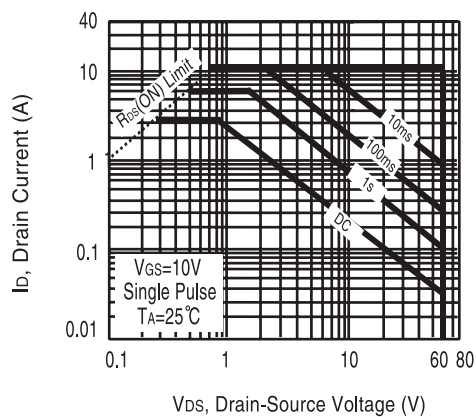
**Figure 7. Transconductance Variation with Drain Current**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**



**Figure 9. Gate Charge**



**Figure 10. Maximum Safe Operating Area**

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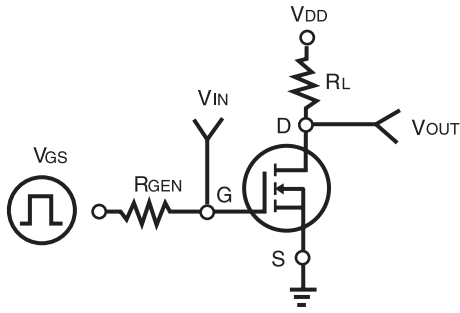


Figure 11. Switching Test Circuit

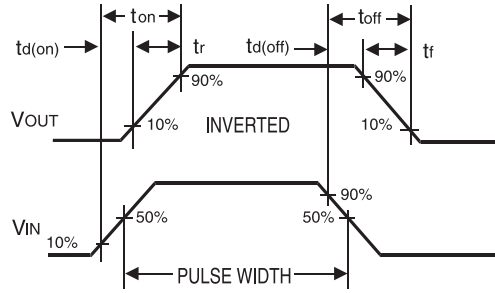


Figure 12. Switching Waveforms

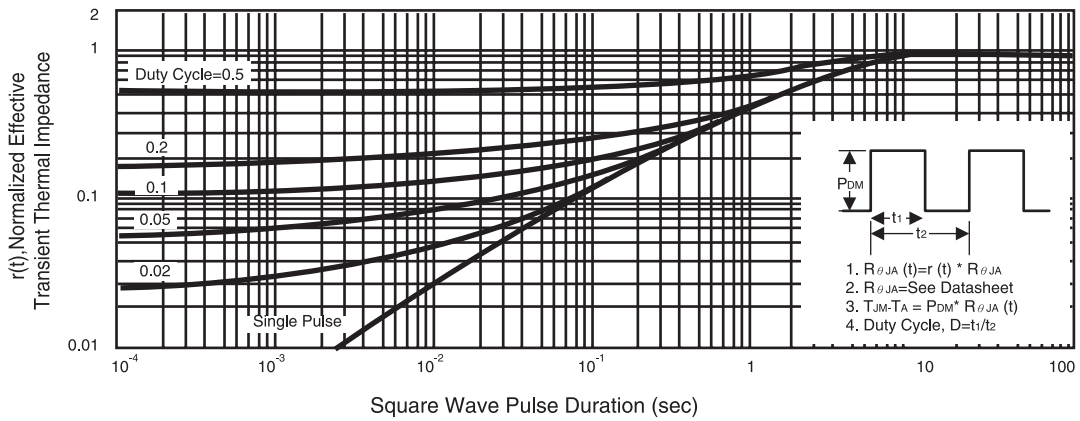


Figure 13. Normalized Thermal Transient Impedance Curve