PM8315, PM5365, PM4328

TEMUX™

TEMUX, TEMAP, TECT3

HIGH DENSITY T1/E1 FRAMER WITH INTEGRATED VT/TU MAPPER AND M13 MULTIPLEXER

Programmer's Guide

Proprietary and Confidential

Release

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Revision History

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4	November 2001	Updated to include TEMAP and TECT3 devices. Removed IIDLE bit. This bit does not exist anymore. Added note to TXGAPEN description for SBI mode.
3	October 2001	Updated to include Errata from PMC-1990677 Issue 9. (Please note that a new errata was also created on this date, for the Production Released TEMUX.) Enhanced BUSMASTER description. Added note to OPMODE description for Transmux mode.
2	April 2001	Added section on operations, Modified SBI setup, corrected errors in section title, register number, bit clarification Addressed Preps 4758, 4821, 4883, 5454 and 5687
	March 2000	Many formatting and clarification changes
	Nov 1999	Added register table.
1	Oct 1999	Document created.

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1 Introduction

This document introduces the reader to the programmable features of the TEMUX, TEMAP and TECT3 by providing the register accesses necessary to configure the devices. It also provides flow charts, figures and tables for programming the real-time aspects of the devices.

This document is a supplement to the TEMUX/ TEMAP/TECT3 datasheet and register description. Due to the vast number of configurations the devices may have, this document may not cover all possible configurations. Please contact a PMC-Sierra Field Applications or Applications Engineer for specific uses not covered in this document.

The TEMAP and TECT3 are functional subsets of the TEMUX. The TEMAP is a high density VT/TU mapper and M13 multiplexer, the TECT3 is a high density T1/E1 framer and M13 multiplexer and the TEMUX is a high density T1/E1 framer with integrated VT/TU mapper and M13 multiplexer.

Table 1 TEMUX, TEMAP and TECT3 Features

	TEMUX	TEMAP	TECT3
M13 Multiplexer	YES	YES	YES
T1/E1 Framer	YES	NO	YES
VT/TU Mapper	YES	YES	NO

This document will explain the programmable features of the TEMUX and where applicable will indicate which features do not apply to the TEMAP and TECT3.

The TEMUX can be programmed into eleven different interface modes of operation. Included in the eleven TEMUX modes are nine modes that apply to the TEMAP and five modes that apply to the TECT3. On power-up, the default register values must be modified via software to successfully use these devices. The devices interface to software via registers and interrupts. Therefore, this document discusses the register accesses and interrupt processing that are necessary to apply the devices to user applications.

Although every effort has been taken to ensure that this document is consistent with the datasheet, some errors may occur. Where there are discrepancies with this document, the datasheet and datasheet errata (if any) will take precedence.

1.1 Target Audience

This document has been prepared for Engineers that design-in the TEMUX, TEMAP and TECT3, and need a quick reference on how to program these devices. It is assumed the reader is familiar with DS3, SONET, E1 and T1 and framing technologies.

1.2 Numbering Conventions

Binary	0001b, 1110b
Decimal	198, 234, 2
Hexadecimal	2H, 200H

2 Register Description

The TEMUX/TEMAP/TECT3 Registers have the following characteristics:

- All values written into unused register bits should be written with logic 0 unless otherwise stated, ensuring software compatibility with future versions of the product. Reading back unused bits can produce either logic one or a logic zero; hence, unused register bits should be masked off by software during a register read access.
- Certain register bits are reserved. To ensure that the TEMUX/TEMAP/TECT3 operates as intended, reserved register bits must only be written with their default values unless otherwise stated in the datasheet.

The TEMUX/TEMAP/TECT3 has two types of register spaces, the “normal” registers, which are accessed directly by the microprocessor bus interface, and the “Indirect” registers which are internal.

Figure 1 TEMUX Block Diagram

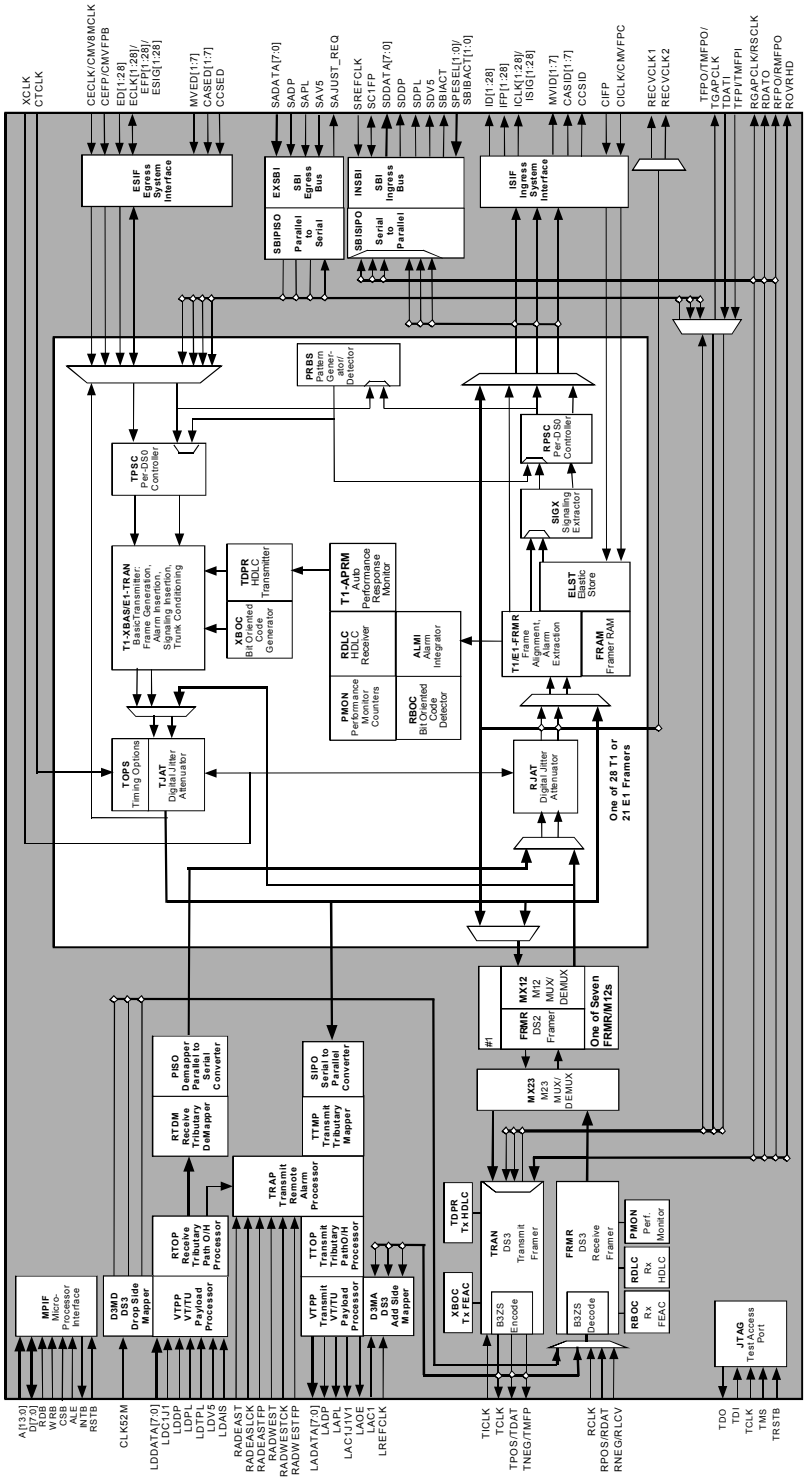


Figure 2 TEMAP Block Diagram

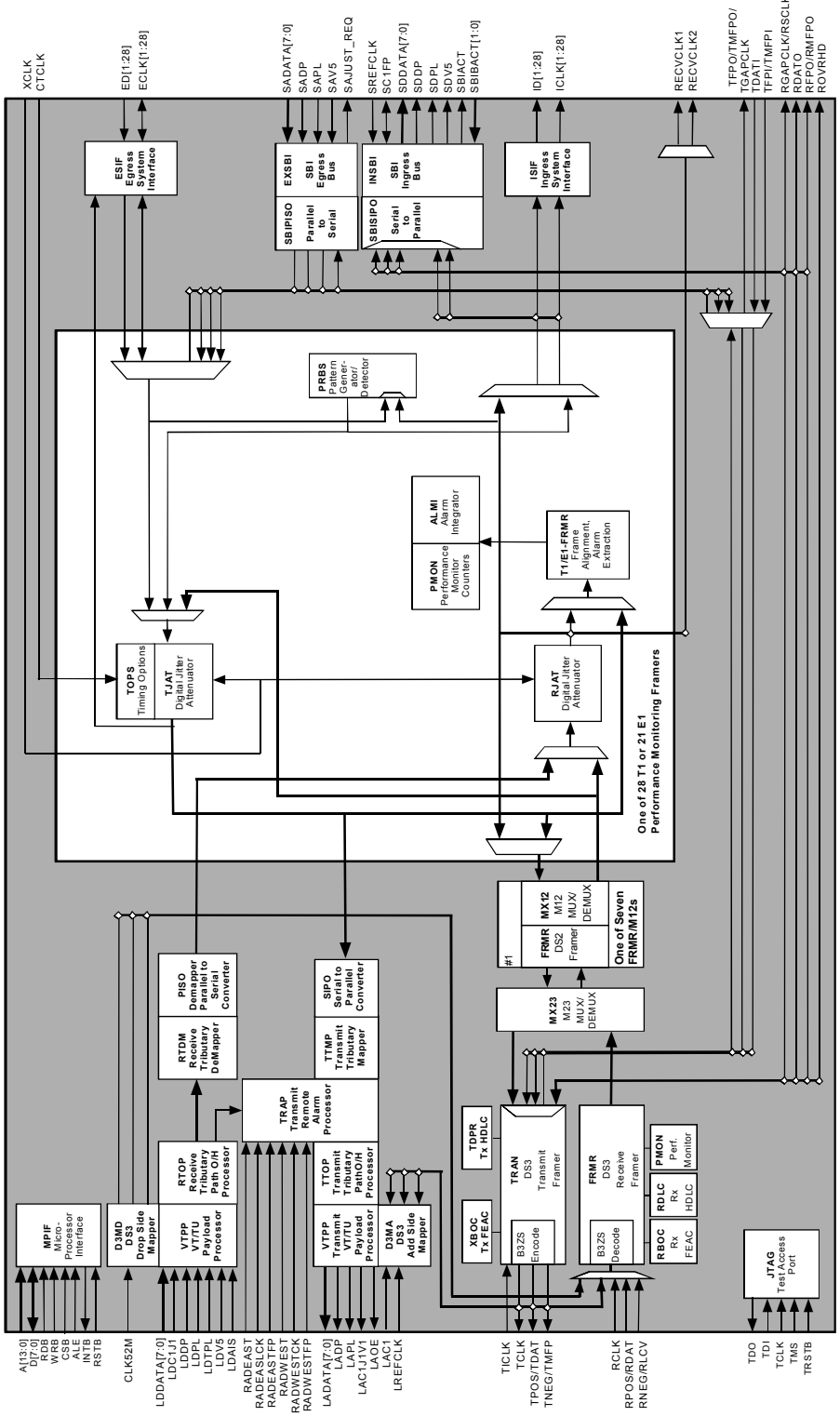
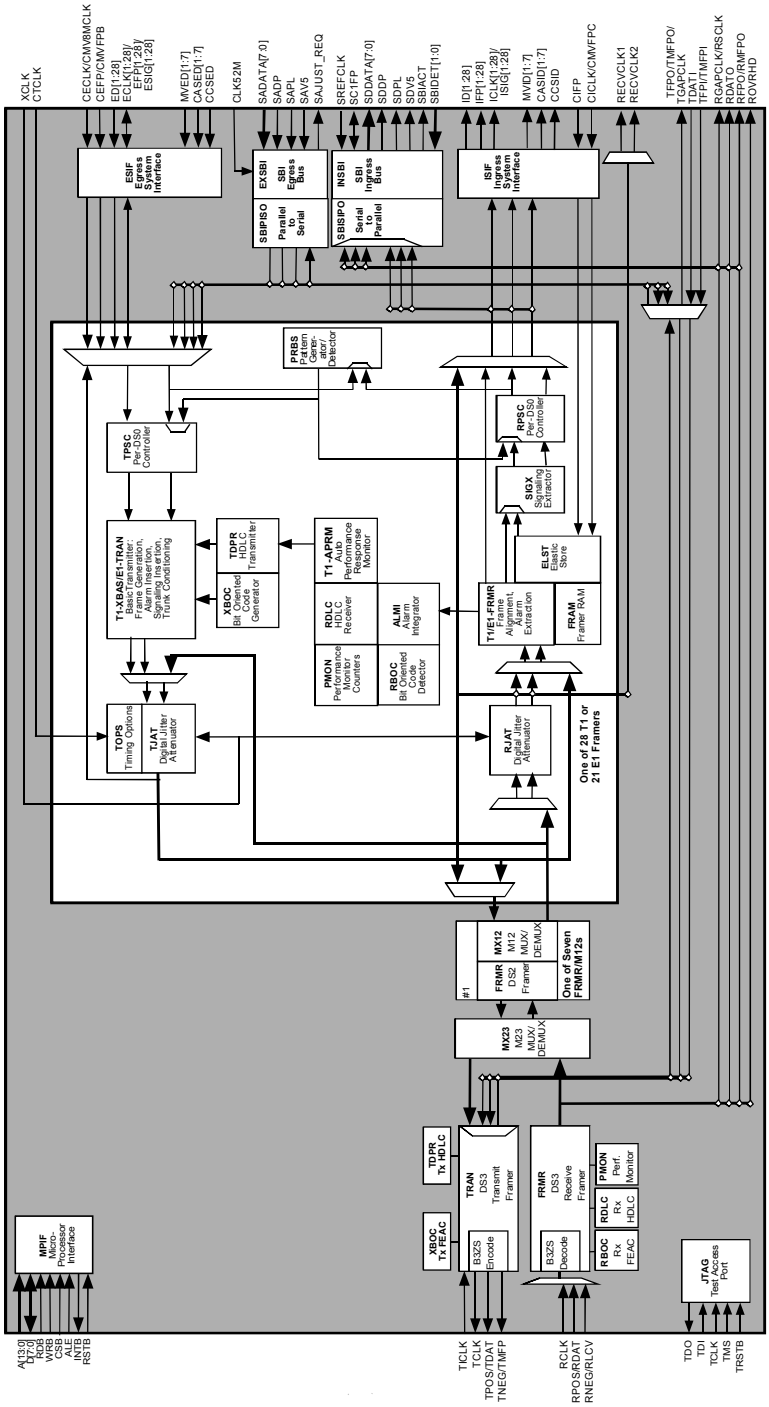


Figure 3 TECT3 Block Diagram



3 TEMUX/TEMAP/TECT3 Mode of Operations

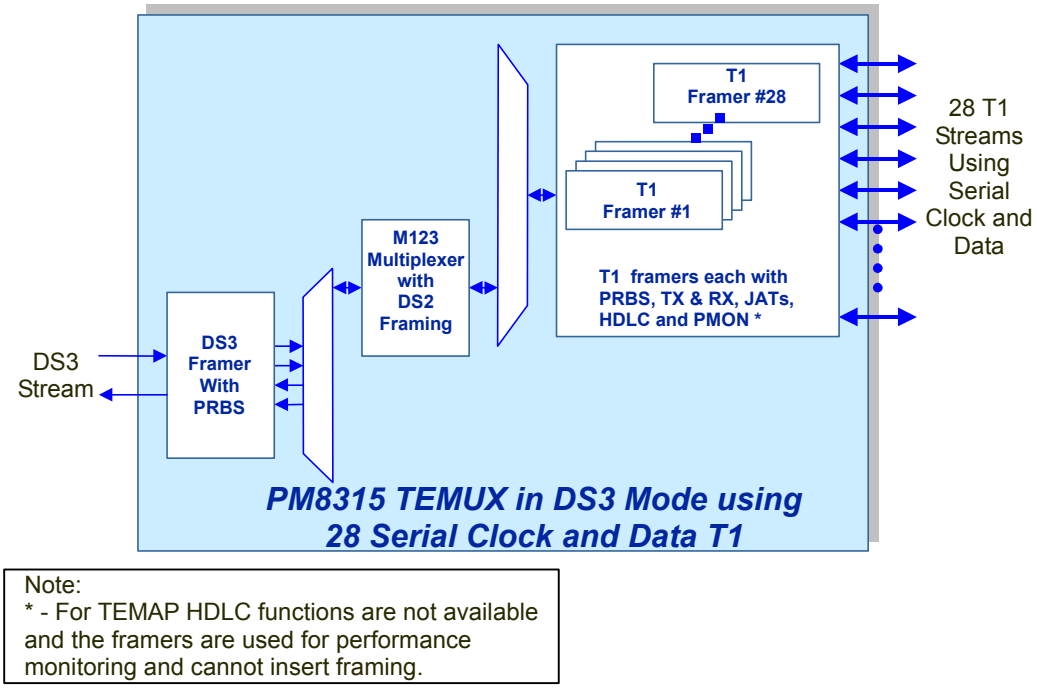
There are eleven interface modes of operation for the TEMUX/TEMAP/TECT3. These are as follows:

Table 2 TEMUX/TEMAP/TECT3 Operation Modes

Line Side Interface	System/Backplane Interface
Serial DS3	28 T1 clock and data
Serial DS3	21 E1 clock and data
Serial DS3	H-MVIP (T1 and E1) (Not Supported for TEMAP)
Serial DS3	Serial DS3
Serial DS3	SBI (Handles DS3 or 28 T1, not E1) with and without CCS.
Telecom Bus (Not Supported for TECT3)	28 T1 clock and data
Telecom Bus (Not Supported for TECT3)	21 E1 clock and data
Telecom Bus (Not Supported for TECT3)	H-MVIP (T1 and E1) (Not Supported for TEMAP)
Telecom Bus (Not Supported for TECT3)	Serial DS3
Telecom Bus (Not Supported for TECT3)	SBI (Handles DS3, 28 T1 or 21 E1) with and without CCS.
Telecom Bus and serial line side DS3 (TRANSMUX MODE) (Not Supported for TECT3)	

3.1 DS3 Line Side Interface 28 Serial Clock/ Data T1 System Interface

Figure 4 DS3 on line side and 28 T1 streams on the system side



Note:
* - For TEMAP HDLC functions are not available and the framers are used for performance monitoring and cannot insert framing.

Figure 4 shows how 28 T1 links are multiplexed into a DS3 stream. The system side access on the T1s is available as serial clock and data. The DS3 line side interface is via the clock and data interface for line interface units. The system side can also be configured for an NxDSO application for a glueless interface to a FREEDM device.

3.2 DS3 Line Side Interface 21 Serial Clock /Data E1 System Interface

Figure 5 DS3 interface on the line side and 21 E1 streams on the system side

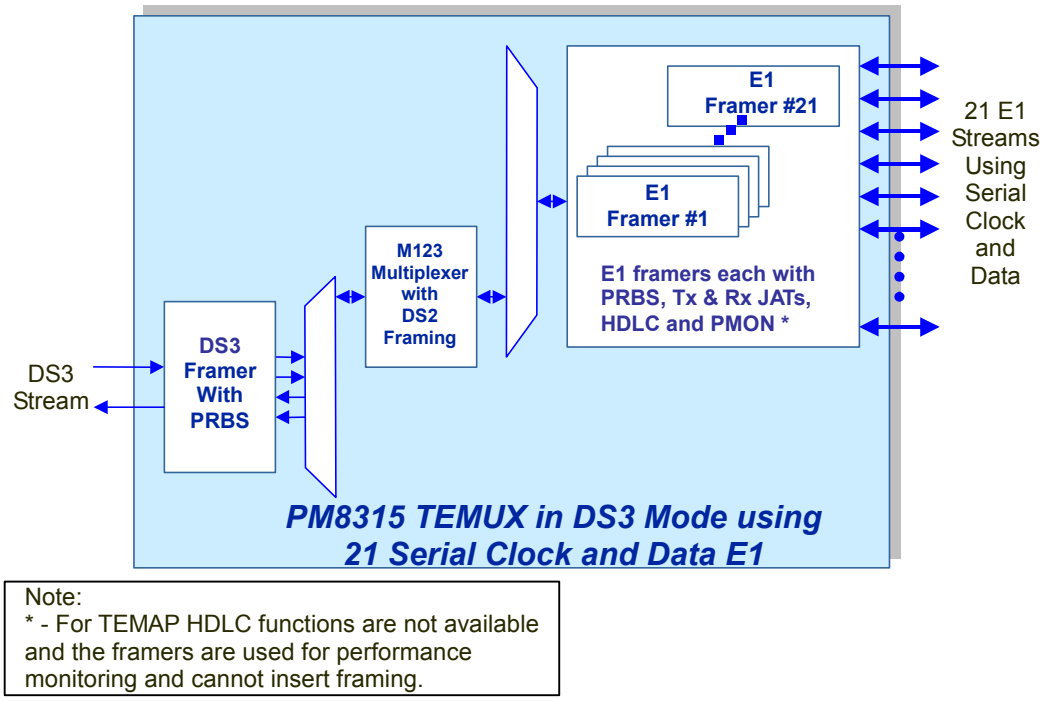


Figure 5 shows how 21 E1 links are multiplexed into a DS3 stream. The system side access on the E1s is available as serial clock and data. The DS3 line side interface is via the clock and data interface for line interface units. The system side can also be configured for an NxDSO application for a glueless interface to a FREEDM device.

3.3 DS3 Line Side Interface H-MVIP System Interface (Not Supported for TEMAP)

Figure 6 DS3 on the line side and an 8.192Mbps H-MVIP interface on the system side

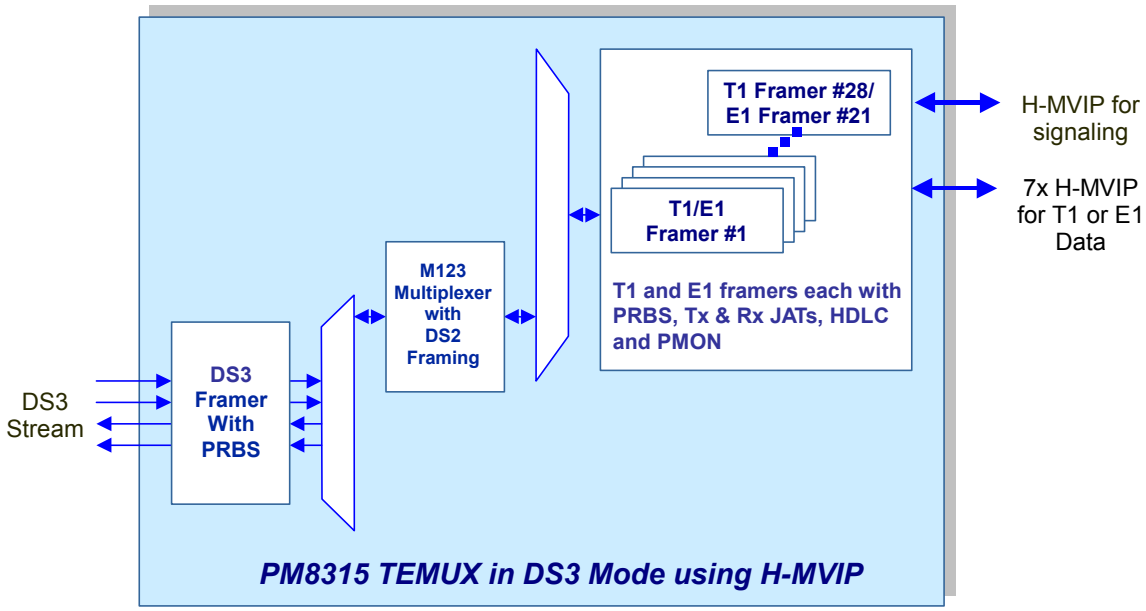


Figure 6 shows T1 and E1 frames from an 8.192MHz H-MVIP link multiplexed into a DS3 stream. The system side access is available via a synchronous H-MVIP Interface. The DS3 line side interface is via the clock and data interface for line interface units. Note that for E1 the seven H-MVIP buses will only contain three E1s each with the fourth empty.

3.4 DS3 Line Side Interface
DS3 System Interface

Figure 7 DS3 on the line side and a DS3 clock and data stream on the system side.

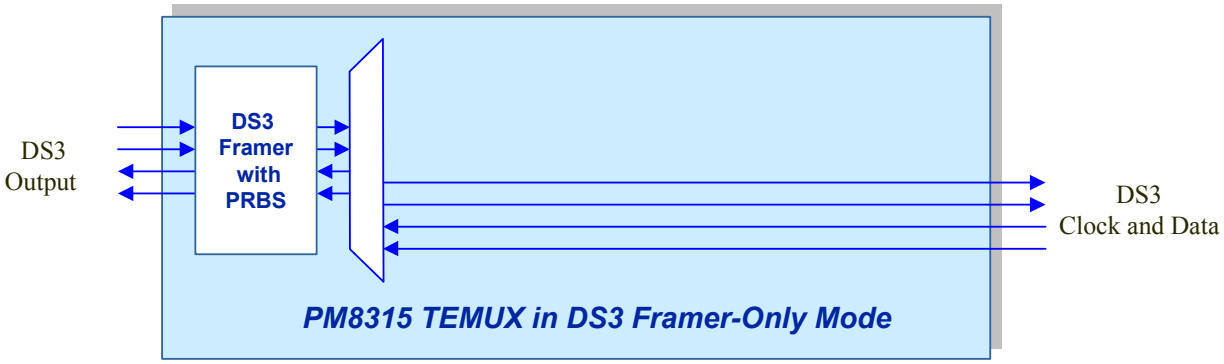


Figure 7 shows an unchannelized DS3 stream on the system side available through a serial clock and data interface and a DS3 line side interface, which connects to a line interface unit. The system side may also be configured for a gapped clock operation making it ideal for a glueless interface to a FREEDM HDLC controller device. This interface can also be used for interfacing to a sub-rate DS3 FPGA.

3.5 DS3 Line Side Interface SBI System Interface

Figure 8 DS3 on line side and SBI on the system side.

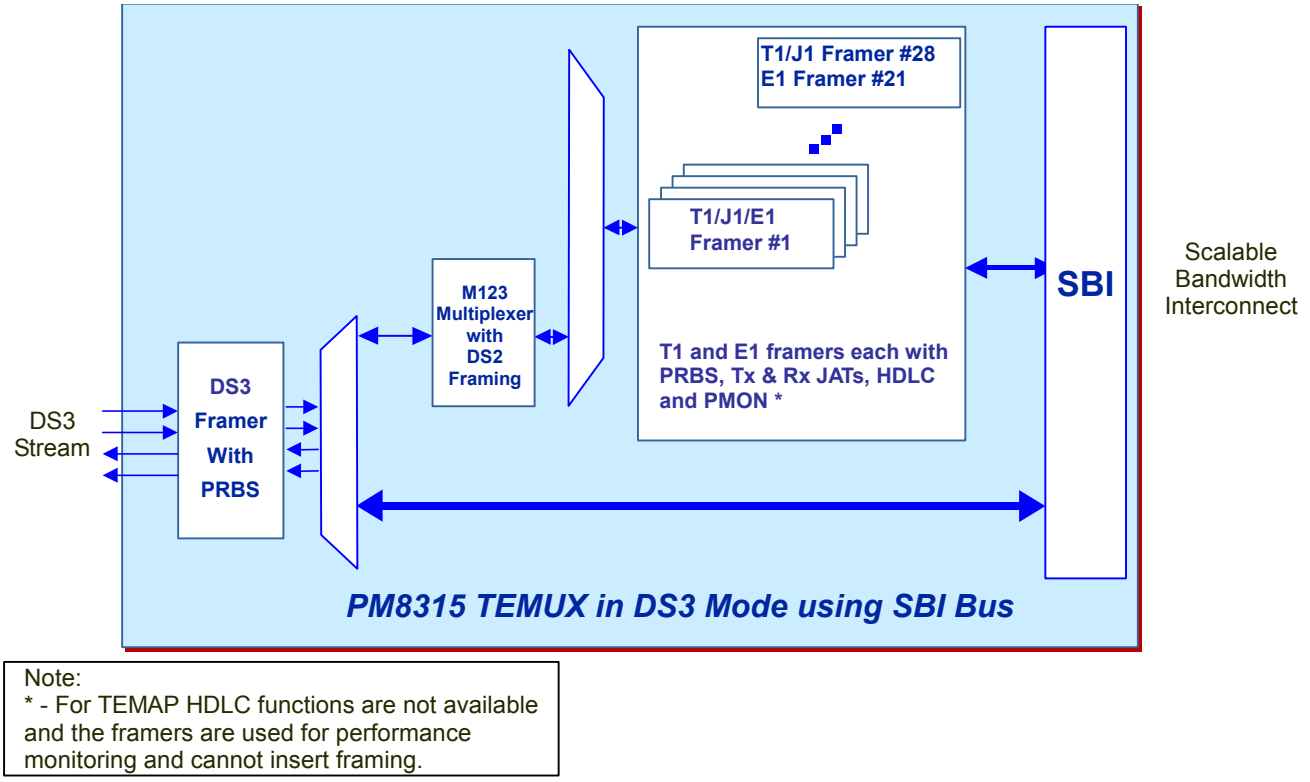


Figure 8 shows 28 T1s or a DS3 link carried over an SBI bus. If this is channelized DS3 then only 28 T1s are multiplexed/ demultiplexed into a DS3 stream. If this is unchannelized DS3 stream the DS3 payload is just framed using a DS3 framer. The system side is referred to as the Scaleable Bandwidth Interconnect and it enables a glueless interface to a FREEDM-84P672 or a FREEDM84A672 device. The DS3 line side interface is via the clock and data interface for line interface units.

3.6 Telecom Bus Line Side 28 Serial Clock/Data T1 Interfaces (Not Supported for TECT3)

Figure 9 Telecom Bus on the line side and 28 T1 streams on the system side

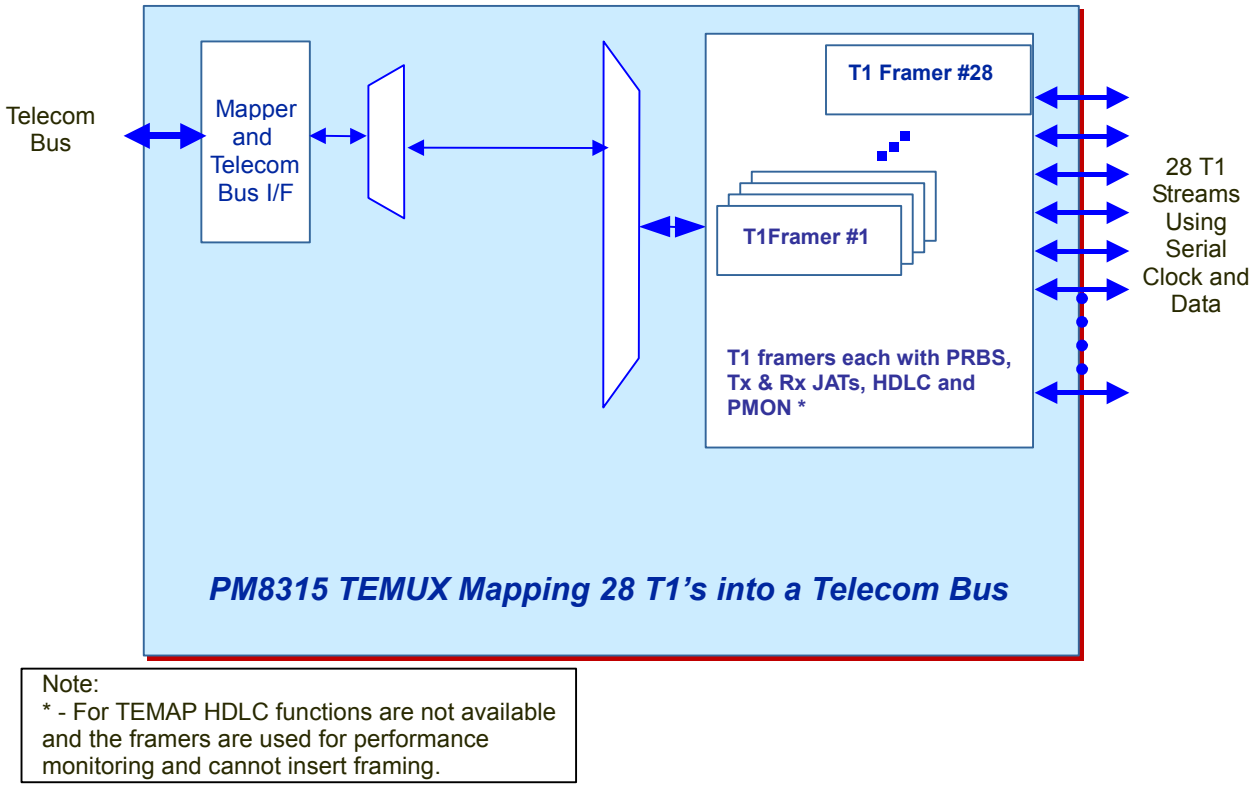
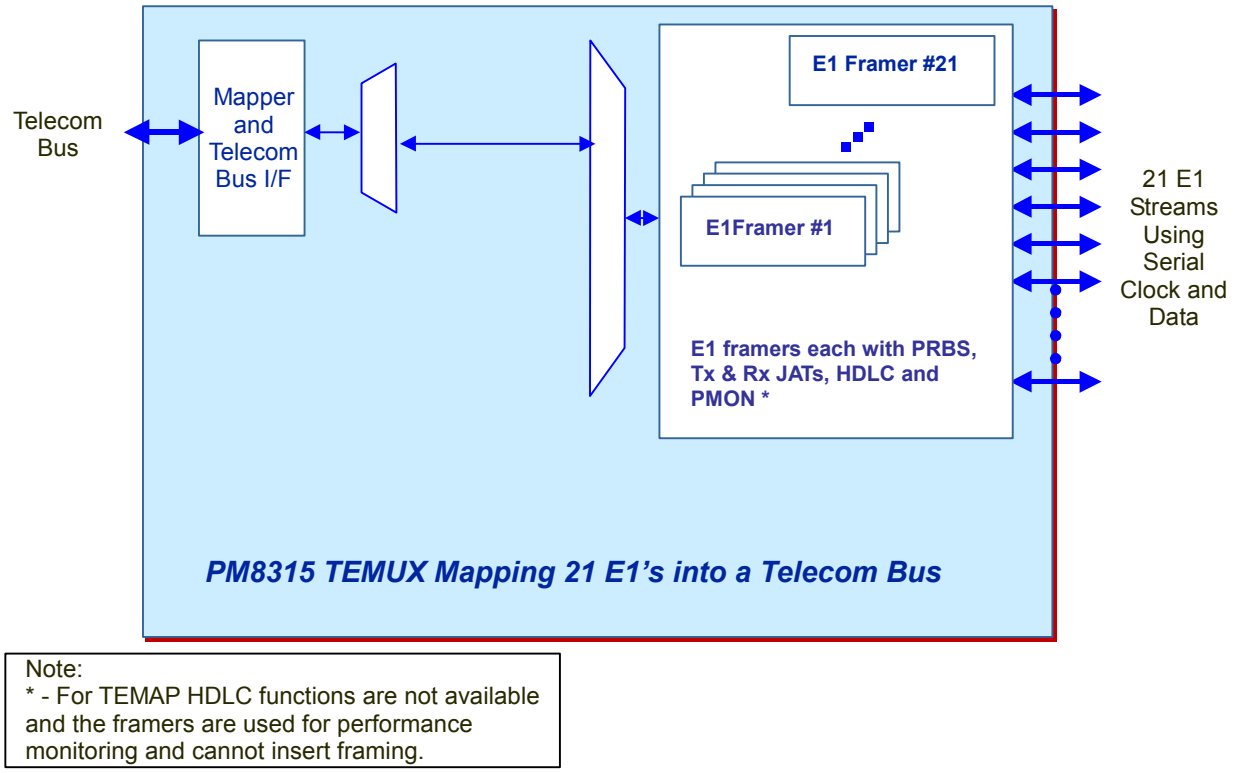


Figure 9 shows 28 T1 streams mapped as bit asynchronous Virtual Tributaries TU-11s/ VT1.5s into a STS-1 SPE or TU-11 tributary unit into an STM-1/VC3 or TUG3 from an STM-1/VC4 using the Telecom Bus.

When adding and dropping T1 tributaries the mapper and demapper blocks allow for up to 28 VT1.5/TU11 tributaries to be processed from any tributary location within the full STS-3/STM-1. On the Telecom DROP bus side this requires that the STS-3/STM-1 be in locked mode such that the J1 bytes immediately follow the C1 bytes.

3.7 Telecom Bus Line Side 21 Serial Clock/Data E1 Interfaces (Not Supported for TECT3)

Figure 10 Telecom Bus interface on the line side and 21 E1 streams on the system side



Note:
* - For TEMAP HDLC functions are not available and the framers are used for performance monitoring and cannot insert framing.

Figure 10 shows 21 E1 streams mapped as bit asynchronous Virtual Tributaries TU-12s /VT2s into a STS-1 SPE or TU-12 tributary unit into an STM-1/VC3 or TUG3 from an STM-1/VC4 using the Telecom Bus.

When adding and dropping E1 tributaries the mapper and demapper blocks allow for up to 21 VT2/TU12 tributaries to be processed from any tributary location within the full STS-3/STM-1. On the Telecom DROP bus side this requires that the STS-3/STM-1 be in locked mode such that the J1 bytes immediately follow the C1 bytes.

3.8 Telecom Bus Line Side H-MVIP Interfaces (Not Supported for TECT3 and TEMAP)

Figure 11 Telecom Bus Interface on the line side and an H-MVIP interface running at 8.192MHz on the system side

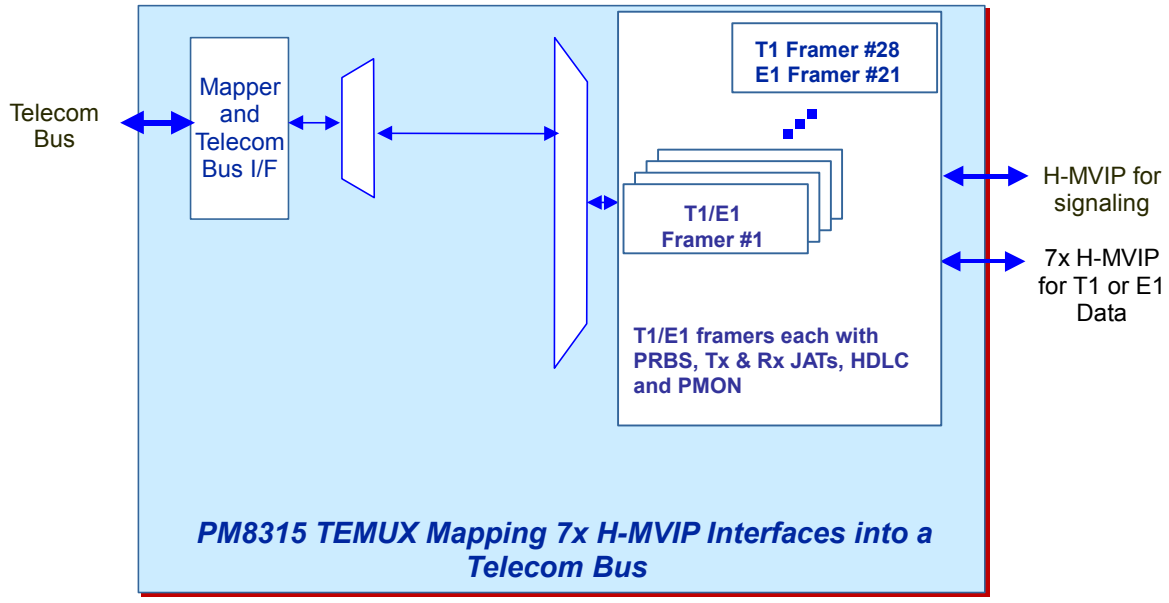


Figure 11 shows 7xH-MVIP interfaces which carry either 21 E1 streams or 28 T1 streams which mapped as bit asynchronous Virtual Tributaries TU-12s /VT2s or TU-11s/VT1.5s into a STS-1 SPE or TU-12, TU-11 tributary units into a STM-1/VC3 or TUG3 from a STM-1/VC4 using the Telecom Bus.

When adding and dropping E1/T1 tributaries the mapper and demapper blocks allow for up to 21 VT2/TU12 or 28 VT1.5/TU11 tributaries to be processed from any tributary location within the full STS-3/STM-1. On the Telecom DROP bus side this requires that the STS-3/STM-1 be in locked mode such that the J1 bytes immediately follow the C1 bytes.

3.9 Telecom Bus Line Side DS3 Interface System Side (Not Supported for TECT3)

Figure 12 Telecom Bus Interface on the line side and a DS3 clock and data stream on the system side.

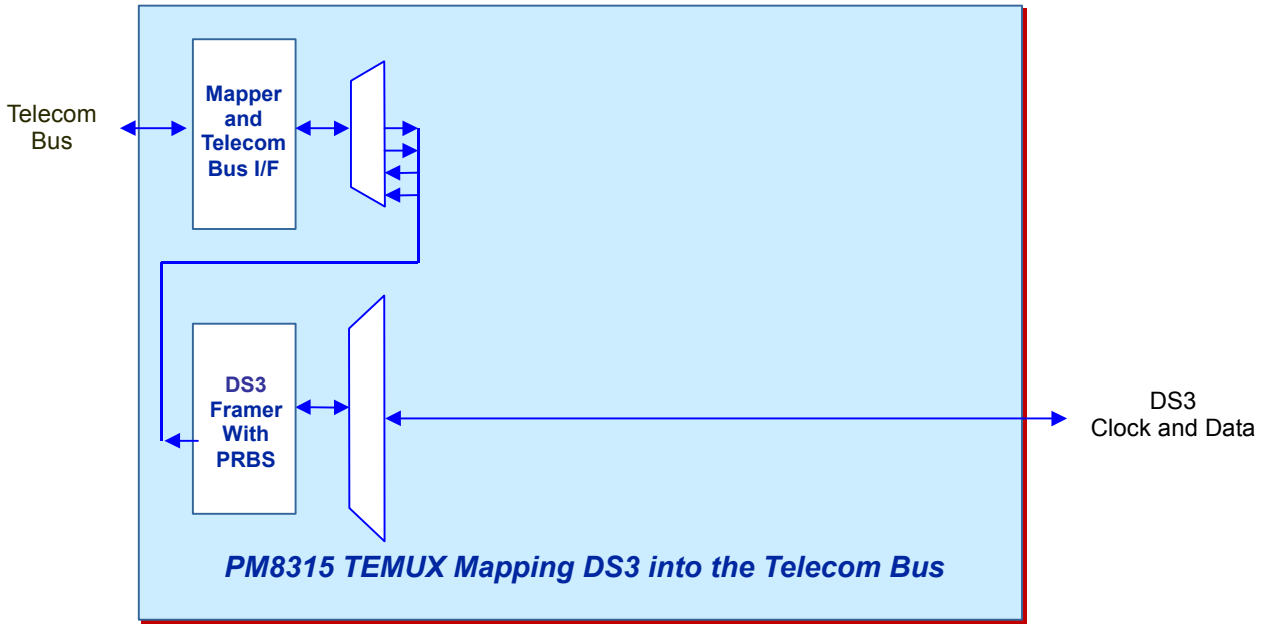


Figure 12 shows a DS3 stream can be mapped or demapped into an STS-1 SPE (AU3).

3.10 Telecom Bus Line Side SBI System Side (Not Supported for TECT3)

Figure 13 Telecom Bus on the line side and an SBI on the system side.

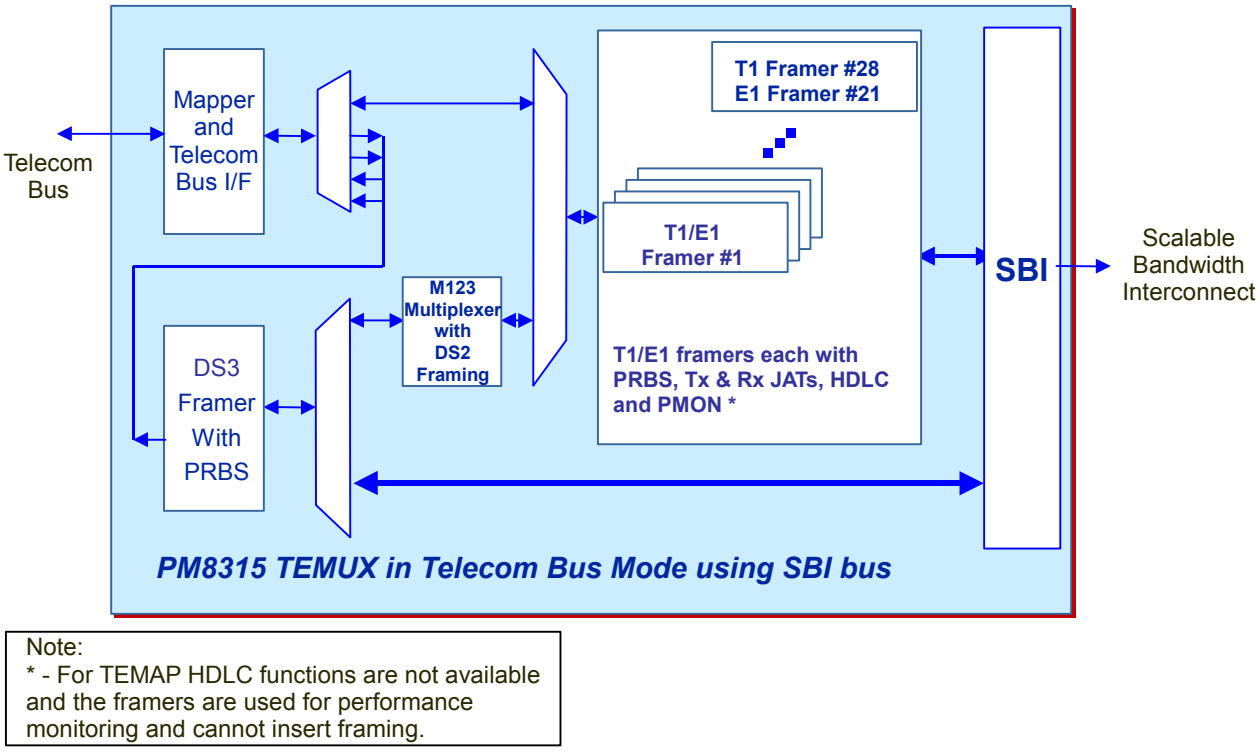


Figure 13 shows how 28 T1 streams, 21 E1 streams or one DS3 stream can be carried over a SBI interface and then mapped via tributaries into VT1.5/TU-11, VT2/TU-12 or TU-3 containers into an STS-1 or VC-3 SPE. The SBI Bus Provides a high-density byte serial interconnect for all TEMUX/TEMAP links. The SBI utilizes an Add/Drop configuration to asynchronously mutliplex up to 84 T1s, 63 E1s or 3 DS3s, equivalent to three TEMUX/TEMAPs, with multiple payload or link layer processors. External devices can access TEMUX/TEMAP unframed DS3, framed unchannelized DS3, unframed (clear channel) T1s, unframed (clear channel) E1s, transparent virtual tributaries or transparent tributary units over this interface, as well as the framed T1s and E1s. Transparent VT/TU access can be selected only when tributaries are mapped into SONET/SDH. Transparent VT1.5s and TU-11s can be selected on a per tributary basis in combination with framed and unframed T1s. Transparent VT2s and TU-12s can be selected on a per tributary basis in combination with framed and unframed E1s. Channel associated signaling bits for channelized T1 and E1 are explicitly identified across the bus. Note if the 21 E1s are multiplexed/demultiplexed to/from a DS3 then they are restricted to serial clock and data mode or H-MVIP mode. H-MVIP mode is not supported for the TEMAP.

3.11 Telecom Bus and DS3 Serial on the Line Side (Not Supported for TECT3)

Figure 14 Telecom Bus Interface on the line side and a DS3 Clock and data bus on the line side

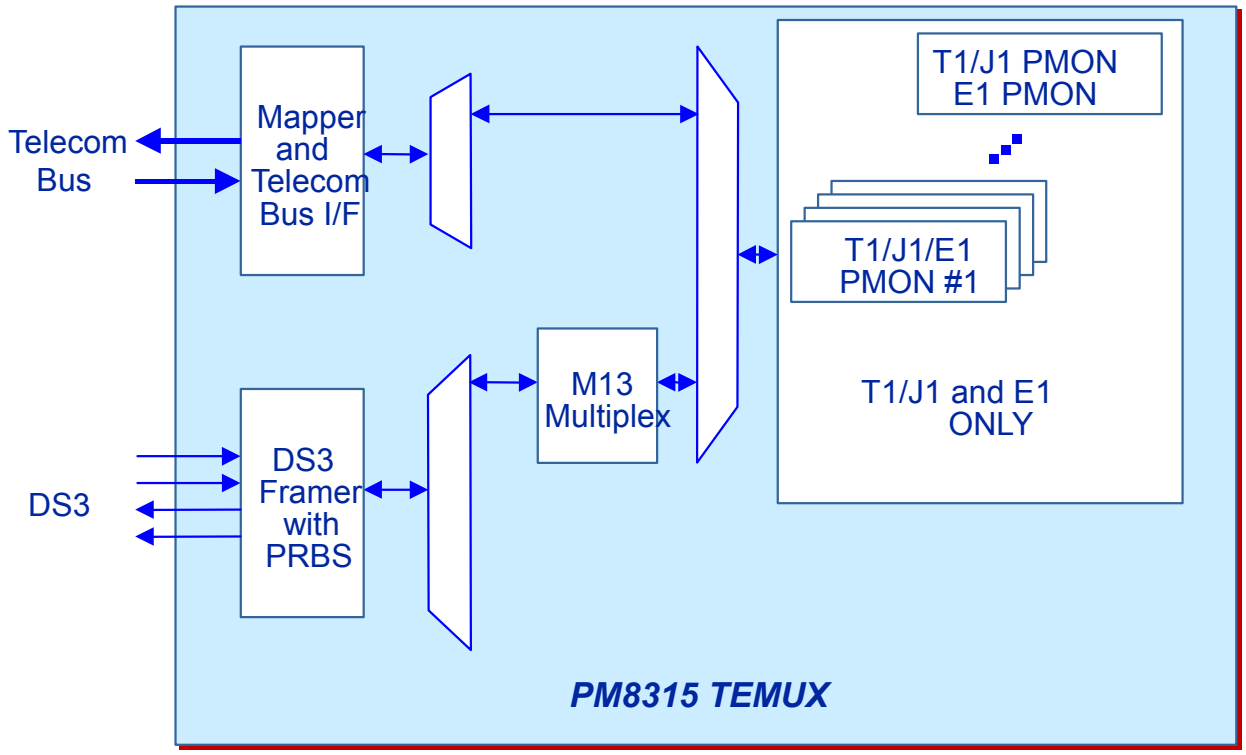


Figure 14 shows an example where the T1s or E1s are demapped from the SONET payload then multiplexed to a DS3, which is sent out to a serial line side interface. A DS3 is received through the serial line interface, demultiplexed then the T1s or E1s are mapped into VTs. This is called Transmux mode.

For each mode of operation the following setups are required. Please refer to the relevant sections within this document and also consult the datasheet to set up the relevant blocks within the device.

Table 3 TEMUX/TEMAP/TECT3 Configuration Requirements

	Line Side	System Side	Mode	Set Up Required
1	DS3	28 T1		DS3 LINE SET UP DS3 MODE SET UP T1/E1 TIMING SET UP T1 MODE SET UP
2	DS3	21 E1		DS3 LINE SET UP DS3 MODE SET UP T1/E1 TIMING SET UP E1 MODE SET UP
3	DS3	H-MVIP	T1 or E1	DS3 LINE SET UP DS3 MODE SET UP H-MVIP SET-UP AND TIMING T1 MODE SET UP Or E1 MODE SET UP
4	DS3	DS3		DS3 LINE SET UP DS3 MODE SET UP DS3 BACKPLANE SET UP
5	DS3	SBI	T1 or DS3	DS3 LINE SET UP DS3 MODE SET UP SBI INTERCONNECT SET UP
6	TelecomBus	28 T1		SETTING UP THE MAPPER T1/E1 TIMING SET UP T1 MODE SET UP
7	TelecomBus	21 E1		SETTING UP THE MAPPER T1/E1 TIMING SET UP E1 MODE SET UP
8	TelecomBus	H-MVIP	T1 or E1	SETTING UP THE MAPPER H-MVIP SET-UP AND TIMING T1 MODE SET UP or E1 MODE SET UP.
9	TelecomBus	DS3		SETTING UP THE MAPPER DS3 MODE SET UP DS3 BACKPLANE SET UP
10	TelecomBus	SBI	E1, T1 or DS3	SETTING UP THE MAPPER T1, E1 or DS3 MODE SETUP SBI INTERCONNECT SET UP
11	TelecomBus DS3 Line I/F			SETTING UP THE MAPPER DS3 LINE SET UP DS3 MODE SET UP Also refer to T1 mode section to set up PMON in channelized DS3 applications.

4 DS3 Set Up

This section describes the registers that need to be configured for using the DS3 LIU, the DS3 backplane, DS3 framing modes and DS3 loopbacks. For DS3 mapping configuration see section 17.

4.1 DS3 Line Side Setup

a) Register 0001H: Global Configuration

LINEOPT[1:0] [1]	'00' DS3 Mux with Serial LIU Interface
Notes: 1. These bits are not supported for the TECT3.	

b) Register 1003H: DS3 Master Transmit Line Options

TICLK	'1' TPOS/ TDAT and TNEG/TMFP updated on the TICLK selected by TRISE bit. '0' TCLK is a buffered version of TICLK (When in looptimed mode when LOOPT bit is set this bit has no effect)
TNEGINV	'0' TNEG/TMFP is not inverted '1' TNEG/TMFP is inverted. (Must be set to '0' when mapping DS3 into SONET/SDH Line Interface)
TPOSINV	'0' TPOS/TDAT is not inverted '1' TPOS/TDAT is inverted (Must be set to '0' when mapping DS3 into SONET/SDH Line Interface)
TRISE	'0' TPOS/TDAT and TNEG/TMFP updated on falling edge. '1' TPOS/TDAT and TNEG/TMFP updated on rising edge.
TUNI	'0' Transmit Interface = TPOS and TNEG (Bipolar Operation) '1' Transmit Interface = TDAT and TMFP (For Unipolar Operation) (TUNI must be set to '1' when mapping DS3 to SONET/SDH Line Interface)

c) Register 1004H: DS3 Master Receive Line Options

RNEGINV	'0' RNEG/RLCV is not inverted '1' RNEG/RLCV is inverted (Must be set to '0' when demapping DS3 from SONET/SDH Line Interface)
RPOSINV	'0' RPOS/RDAT is not inverted '1' RPOS/RDAT is inverted (Must be set to '0' when demapping DS3 from SONET/SDH Line Interface)
RFALL	'0' RPOS/RDAT and RNEG/RLCV sampled on rising edge. '1' RPOS/RDAT and RNEG/RLCV sampled on falling edge.

d) Register 100CH: DS3 FRMR Configuration

UNI	'1' Configures for Single Rail Data Stream on RDAT. RLCV is used for line code violations '0' Configures for Dual Rail Data on RPOS and RNEG. (UNI must be set to '1' when demapping a DS3 signal from the a SONET/SDH interface.)

e) Register 1001H: DS3 Master Data Source

LOOPT	'0' The Transmit Timing (TCLK) is sourced from the TICLK clock input '1' The Transmit Timing (TCLK) is sourced from the Receive Clock (RCLK)
SBICLKMODE	Applicable only when TEMUX/TEMAP/TECT3 is configured for DS3 framer only mode over the SBI System Interface. '0' TEMUX/TEMAP/TECT3 is configured for DS3 framer only mode over the SBI and TEMUX/TEMAP/TECT3 is slave to DS3 clock from SBI Bus. The CLK_MSTR bit for TRIB[1] in the EXSBI Tributary Control Indirect Access Data must be set to match this setting. When connecting to an LIU this mode produces a jitter output clock thus should have external jitter attenuation circuitry available. '1' TEMUX/TEMAP/TECT3 is Egress Clock Master

4.2 DS3 Backplane Set Up

a) Register 0001H: Global Configuration

OPMODE[1:0]	‘11’ DS3 Framer Only Mode

b) Register 1001H: DS3 Master Data Source

RCVCLR	‘1’ Configured for DS3 Framer Only. A clear channel DS3 is passed from the DS3 backplane or SBI Bus. ‘0’ DS3 Payload is accessed from the DS3 backplane or SBI Bus and the TEMUX/TEMAP/TECT3 will insert the framing bits. (This is only applicable when DS3 Framer only mode is set in the Global Configuration Register 0001H).

c) Register 1002: DS3 Master Unchannelized Interface Options

TDATIFALL	‘1’ TDAT, TFPI/TMFPI sampled on falling edge of TICLK or TXGAPEN ‘0’ TDAT, TFPI/TMFPI is sampled on rising edge of TICLK or TXGAPEN
TXGAPEN	‘0’ Either TFPO or TMFPO output is enabled. ‘1’ TGAPCLK is enabled. (Must be set to '0' for SBI mode operation)
TXMFPO	‘0’ TFPO is enabled ‘1’ TMFPO is enabled (Must be set to ‘1’ for SBI mode operation)
TXMFPI	‘0’ TFPI will be expected ‘1’ TMFP will be expected (Must be set to ‘1’ for SBI mode operation)
RXMFPO	‘0’ RFPO will be available ‘1’ RMFPI will be available (Must be set to ‘1’ for SBI mode operation)
RXGAPEN	‘0’ RSCLK output enabled ‘1’ RXGAPCLK output enabled
RSCLKR	‘0’ RDATO, RMFPO and ROVRHD outputs updated on falling edge of RSCLK. ‘1’ RDATO, RMFPO and ROVRHD outputs updated on rising edge of RSCLK.

4.3 DS3 Mode Set Up

4.3.1 Framing Setup

a) Register 1008H: DS3 TRAN Configuration

CBIT	'0' Transmit is set up for M23 mode '1' Transmit is set up for C Bit Parity mode

b) Register 100CH: DS3 FRMR Configuration

CBE	'0' Receive is set up for M23 mode '1' Receive is set up for C Bit Parity mode

c) Register 1040H: MX23 Configuration

CBE	'0' MX23 is set up for M23 mode '1' MX23 is set up for C Bit Parity mode

4.3.2 Unchannelized DS3 Mode with M23 or C Bit Parity Framing

a) Register 0001H: Global Configuration

OPMODE[1:0]	'11' DS3 Framer Only Mode

4.3.3 Channelized DS3 T1 Mode

a) Register 0001H: Global Configuration

OPMODE[1:0]	'00' High Density Framer Mode [1]
E1T1B	'0' T1 Mode
Notes: 1. High Density Framer Mode is not supported in TEMAP.	

4.3.4 Channelized DS3 E1 Mode(G.747)

a) Register 0001H: Global Configuration

OPMODE[1:0]	'00' High Density Framer Mode [1]
E1T1B	'1' E1 Mode
Notes: 1. High Density Framer Mode is not supported in TEMAP.	

b) Register 1040H+20H*N DS2 FRMR #1-#7

G747	'1' enables E1 to be mapped into a DS3 stream

c) Register 1050H+20H*N MX12 Multiplexer #1-#7

G747	'1' enables E1 to be mapped into a DS3 stream

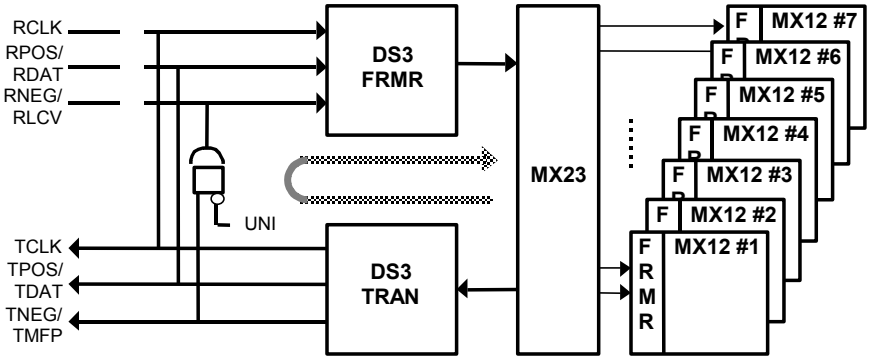
4.4 DS3 LOOPBACK

The TEMUX/TEMAP/TECT3 provides three DS3 M13 multiplexer loopback modes to aid in network and system diagnostics at the DS3 interface. The DS3 loopbacks can be initiated via the µP interface whenever the DS3 framer/M13 multiplexer is enabled. The DS3 Master Data Source register controls the DS3 loopback modes. These loopbacks are also available when the DS3 mux is used with the DS3 mapper via the Telecom bus interface.

4.4.1 DS3 Diagnostic Loopback

DS3 Diagnostic Loopback allows the transmitted DS3 stream to be looped back into the receive DS3 path, overriding the DS3 stream received on the RDAT/RPOS and RNEG/RLCV inputs. The RCLK signal is also substituted with the transmit DS3 clock, TCLK. The configuration of the receive interface determines how the TNEG/TMFP signal is handled during loopback: if the UNI bit in the DS3 FRMR register is set, then the receive interface is configured for RDAT and RLCV, therefore the TNEG/TMFP signal is suppressed during loopback so that transmit MFP indications will not be seen nor accumulated as input LCVs. If the UNI bit is clear, then the interface is configured for bipolar signals RPOS and RNEG, therefore the TNEG is fed directly to the RNEG input. This diagnostic loopback can be used when configured as a multiplexer or as a framer only. The DS3 loopback mode is shown diagrammatically in Figure 15.

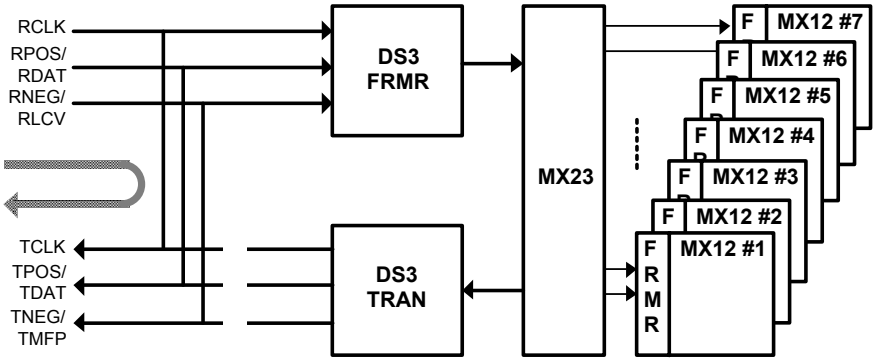
Figure 15 DS3 Diagnostic Loopback Diagram



4.4.2 DS3 Line Loopback

DS3 Line Loopbacks allow the received DS3 streams to be looped back into the transmit DS3 paths, overriding the DS3 streams created internally by the multiplexing of the lower speed tributaries. The transmit signals on TPOS/TDAT and TNEG/TMFP are substituted with the receive signals on RPOS/RDAT and RNEG/RLCV. The TCLK signal is also substituted with the receive DS3 clock, RCLK. Note that the transmit interface must be configured to be the same as the DS3 FRMR receive interface for this mode to work properly. The DS3 line loopback mode is shown diagrammatically in Figure 16. There is a second form of line loopback, which only loops back the DS3 payload. In this mode the DS3 framing overhead is regenerated for the received DS3 stream and then retransmitted. Line loopback is selected with the LLOOP bit in the DS3 Master Data source register and the PLOOP bit in the same register selects payload loopback.

Figure 16 DS3 Line Loopback Diagram



a) Register 1001H:DS3 Master Data Source

LLOOP	'0' Normal operation '1' Line Loopback enabled. RPOS/RDAT and RNEG/RLCV are looped to TPOS/TDAT and TNEG/TMFP. RCLK is used for reference.
DLOOP	'0' Normal operation '1' Transmit Data Stream is looped to the Receive Direction. The TUNI register bit in the TEMUX/TEMAP/TECT3 Transmit Line Options Register must be set the same as the UNI Bit in DS3 frame register.
PLOOP	'0' Normal operation '1' DS3 payload loopback is enabled. The DS3 overhead bits are regenerated. The received data stream is re inserted into the transmit stream. The bit must be set before the TEMUX/TEMAP/TECT3 is configured for DS3 Framer Only mode to operate in DS3 Framer Only mode.

5 T1/E1 Timing Set Up

5.1 Egress Timing Options

The TEMUX/TEMAP/TECT3 supports the following EGRESS Timing Options:

- Clock Master: NxChannel (Not Supported for TEMAP)
- Clock Master: Clear Channel
- Clock Slave: EFP Enabled (Not Supported for TEMAP)
- Clock Slave: External Signaling (Not Supported for TEMAP)
- Clock Slave: Clear Channel
- Clock Slave: H-MVIP *Please refer to H-MVIP section (Not Supported for TEMAP)
- Clock Master: SBI *Please refer to SBI section
- Clock Slave: SBI *Please refer to the SBI section

5.1.1 Egress Clock Master Transmit Clock Source and Options

In all Egress Clock Master Modes the Transmit Clock for each T1 line can be sourced from the following:

- CTCLK
- One of two T1/E1 Receive Recovered clocks REVCLK1 and REVCLK2
- Receive Recovered clock for the individual T1/E1 line.

a) Register 003H: Master Recovered Clock#1/ Reference Clock Select

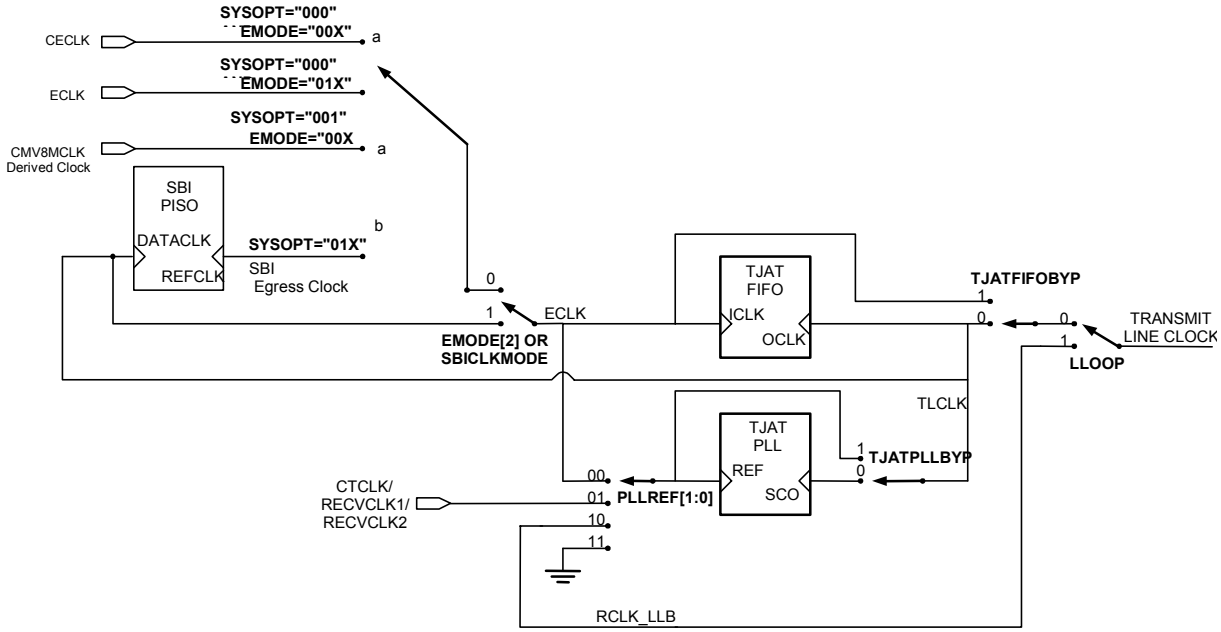
REFCLK[1:0]	'00' Selects CTCLK pin as Transmit Clock for all T1 or E1 lines '01' RECVCLK1 selects one of the 28(T1) or 21(E1) recovered clocks as the Transmit Clock or all T1 or E1 lines. '10' RECVCLK2 selects one of the 28(T1) or 21(E1) recovered clocks as the Transmit Clock for all T1 or E1 lines.
RECV1SEL[4:0]	Select the source of the recovered T1 or E1 clock (RECVCLK1) from one of 28 (T1) or 21(E1) clocks. (When in E1 mode the T1/E1 framers slices from 22 to 28 will result in an invalid recovered clock)

b) Register 0004H: Recovered Clock #2 Select

RECV2SEL[4:0]	Select the source of the recovered T1 or E1 clock (RECVCLK2) from one of 28 (T1) or 21(E1) clocks. (When in E1 mode the T1/E1 framers slices from 22 to 28 will result in an invalid recovered clock)

Figure 17 shows how the transmit jitter attenuator can be configured to be in or out of the transmit path. TxCLK is the TEMUX/TEMAP/TECT3 internal clock that is used for egress timing in Master clock modes and is the data clock to the DS3 M13 Mux or the SONET/SDH Mapper. RCLK is the recovered clock.

Figure 17 Transmit Timing Options Diagram



Notes:
a) This mode is not supported for the TEMAP.
b) SYSOPT = “010” for TEMAP.

c) Register 004H+80H*N: T1/E1 Egress Line Interface Configuration

PLLREL[1:0]	Selects the source of the clock going into the TJAT Digital PLL. '00' Slave Clock (Do not used when in clock master mode) **'01' External Transmit Reference (CTCLK, RECVCLK1 or RECVCLK2)** **'10' Recovered Receive Clock** ('01' and '10' should be used in all clock master modes) '11' Slave Clock (Do not use when on Clock Master mode)
TJATPLLBYP	'0' Jitter Attenuation is done on the Transmit Clock '1' Jitter attenuation on the transmit clock is not done. (This is useful to jitter attenuate an external transmit reference clock. Normally, the JAT will always be used.)
TJATFIFOBYP	'0' TJAT FIFO is used to attenuate jitter on the Transmit data. '1' TJAT FIFO is not active and no Transmit Data Jitter Attenuation is done. This reduces the latency by 40 bits. A jitter free transmit clock source must be available. (Normally, the JAT will always be used.)

d) Register 009H+80H*N: T1/E1 Serial Interface Configuration

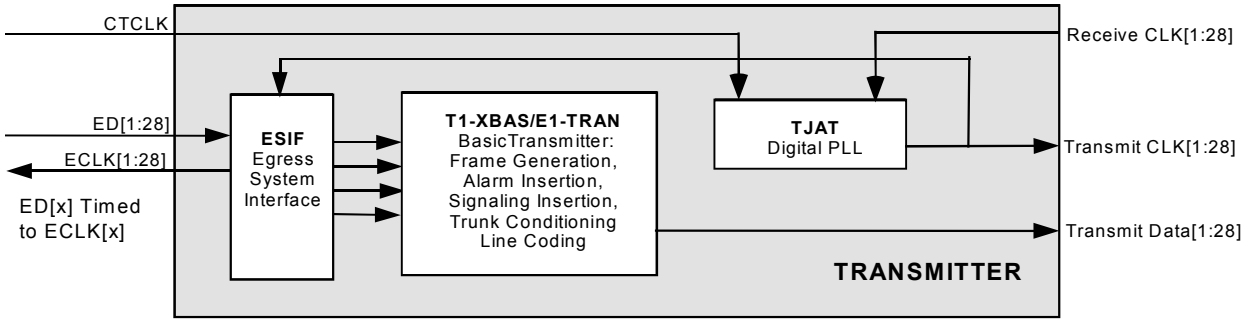
EDE	'0' ED[x] is sampled on ECLK[x] rising edge. '1' ED[x] is sampled on ECLK[x] falling edge.

e) Register 008H+80H*N: T1/E1 Egress Parity Enable (Not Supported for TEMAP)

EDPEN	'0' Egress Data Parity disabled '1' Egress Data Parity Enabled
EPTYP	'0' Odd Parity selected '1' Even Parity selected
EPEXTD	'0' Parity calculated over current frame '1' Parity calculated over previous frame

5.1.2 Egress Clock Master: NxChannel (Not Supported for TEMAP)

Figure 18 Egress Clock Master: NxChannel



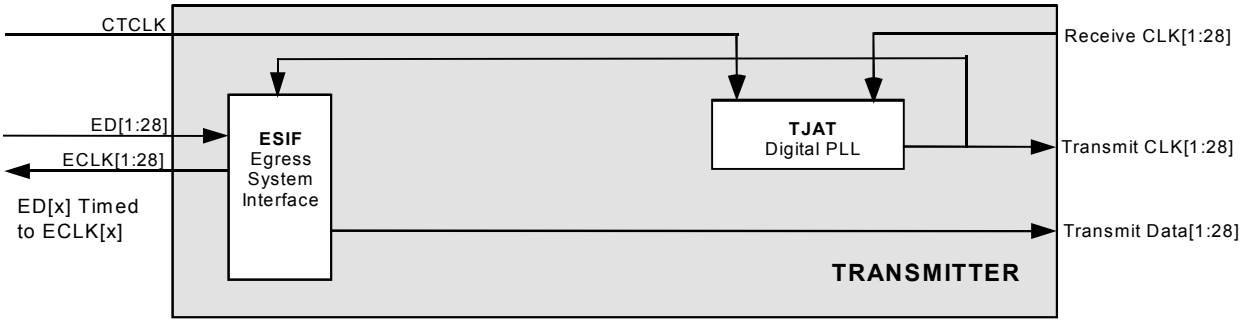
Clock Master: NxChannel mode does not indicate frame alignment to the upstream device. Instead, ECLK[x] is gapped on a per channel basis so that a subset of the 24 channels in a T1 frame or 32 channels in an E1 frame are inserted on ED[x]. The IDLE_CHAN bits in the TPSC block's Egress Control Bytes control channel insertion. The framing bit position is always gapped, so the number of ECLK[x] pulses is controllable from 0 to 192 pulses per T1 frame or 0 to 256 pulses per E1 frame on a per-channel basis. The parity functions should not be enabled in NxChannel mode.

a) Register 006H+80H*N: T1/E1 Egress Serial Interface Mode Select

EMODE[2:0]	'00X' Clock Master: NxChannel/ Full T1/E1
ENXCHAN[1:0]	'00' Full Frame '01' 56 kbit/s NxChannel '10' 64 kbit/s NxChannel '11' 64 kbit/s NxChannel with F bit (only valid for E1). Used to carry T1 over E1 if E1 is selected. When in NxChannel mode only those time slots with their IDLE_CHAN bit set to '0' in the TSPC Indirect Registers : PCM Data Control byte will be clocked out.

5.1.3 Egress Clock Master: Clear Channel

Figure 19 Egress Clock Master: Clear Channel



Clock Master: Clear Channel mode has no frame alignment therefore a frame alignment is not indicated to the upstream device. ECLK[x] is a continuous clock at 1.544Mb/s for T1 links or 2.048Mb/s for E1 links.

a) Register 006H+80H*N: T1/E1 Egress Serial Interface Mode Select

EMODE[2:0]	'11X' Clock Master: Clear Channel

b) Register 004H+80H*N: T1/E1 Egress Line Interface Configuration

TXCLRCH	'1' Transmit Framer is bypassed. '0' The TJAT is not bypassed. (This must be set to '1' when using the unframed tributary type with the SBI Bus or when using the Clear Channel Modes with serial clock and data. When using framed tributary type with the SBI Bus this bit should be set to '0').

5.2 Egress Clock Slave

a) Register 004H+80H*N: T1/E1 Egress Line Interface Configuration

PLLREL[1:0]	Selects the source of the clock going into the TJAT Digital PLL. '00' Slave Clock '11' Slave Clock (Do not use when on Clock Master mode)
TJATPLLBYP	'0' Jitter Attenuation is done on the Transmit Clock '1' Jitter attenuation on the transmit clock is not done (This is useful to jitter attenuate an external transmit reference clock)
TJATFIFOBYP	'0' TJAT FIFO is used to attenuate jitter on the Transmit data '1' TJAT FIFO is not active and no Transmit Data Jitter Attenuation is done. This reduces the latency by 40 bits

b) Register 0005H: Master Common Egress Serial and H-MVIP Interface Configuration (Not Supported for TEMAP)

CECLK2M	'0' CECLK is 1.544MHz in T1 mode '1' CECLK is 2.048MHz in T1 mode
CEFE	'0' CEFP is sampled on falling edge of CECLK '1' CEFP is sampled on rising edge of CECLK
CEFPINV	'0' CEFP normally low and pulse high to indicate a frame boundary. '1' CEFP is normally high and pulse low to indicate a frame boundary.
CEMFP	'0' EFP indicates a frame boundary '1' EFP indicates a multiframe boundary

c) Register 003H+80H*N: T1/E1 Alarm Configuration (Not Supported for TEMAP)

XCLKDIV2	'0' when CECLK2M of Register 005H is set to '0' '1' when CECLK2M of Register 005H is set to '1'

d) Register 009H+80H*N: T1/E1 Serial Interface Configuration

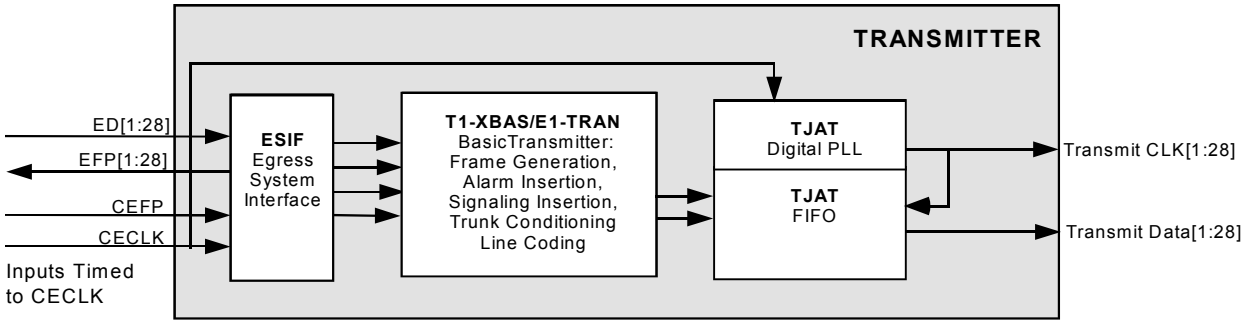
EMFP [1]	'0' EFP[x] indicates a frame alignment '1' EFP[X] indicates a frame boundary either every 12 (SF) or 24 (ESF) in T1 modes. Indicates a Multiframe every 16 frames in E1
EPINV [1]	'0' EFP[x] is normally low and pulses high to indicate a frame boundary '1' EFP[x] is normally high and pulses low to indicate a frame boundary
EDE	'0' ED[x] and is sampled on CECLK rising edge '1' ED[x] and is sampled on CECLK falling edge
EFE [1]	If EFE equals EDE, EFP[x] is updated one CECLK cycle before ED[x] is sampled If EFE does not equal EDE, EFP[x] is updated one half CECLK cycle before ED[x]
Notes: 1. This bit is not supported for the TEMAP.	

e) Register 008H+80H*N: T1/E1 Egress Parity Enable (Not Supported for TEMAP)

EDPEN	'0' Egress Data Parity disabled '1' Egress Data Parity Enabled
EPTYP	'0' Odd Parity selected '1' Even Parity selected
EPEXTD	'0' Parity calculated over current frame '1' Parity calculated over previous frame

5.2.1 Clock Slave, EFP Enabled (Not Supported for TEMAP)

Figure 20 Clock Slave with EFP



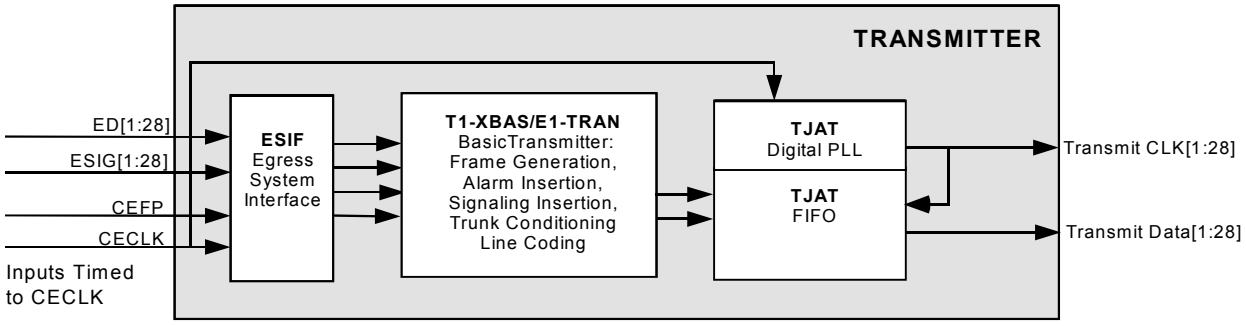
In Clock Slave EFP Enabled mode, the common egress clock, CECLK, clocks the egress interface. The transmitter is either frame-aligned or superframe-aligned to the common egress frame pulse, CEFP, via the CEMFP bit in the Master Egress Slave Mode Serial Interface Configuration register. EFP[x] is configurable to indicate the frame alignment or the superframe alignment of ED[x]. CECLK can be enabled to be either a 1.544 MHz clock for T1 links or a 2.048 MHz clock for T1 and E1 links. The CECLK2M bit in the Master Egress Slave Mode Serial Interface Configuration register selects the 2.048MHz clock for T1 operation.

a) Register 006H+80H*N: T1/E1 Egress Serial Interface Mode Select

EMODE[2:0]	'001' Clock Slave: EFP Enabled [1]
Notes: 1. This mode is not supported in the TEMAP.	

5.2.2 Clock Slave : External Signaling (Not Supported for TEMAP)

Figure 21 Clock Slave: External Signaling



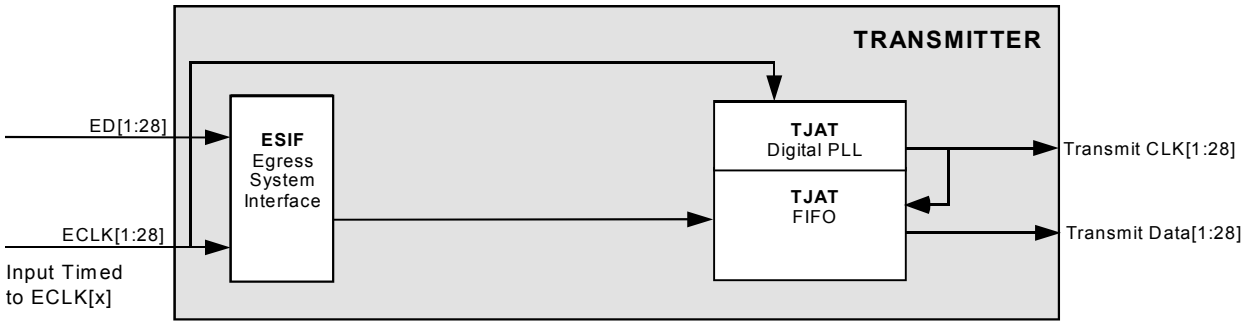
In Clock Slave External Signaling mode, the common egress clock, CECLK, clocks the egress interface. The transmitter is either frame-aligned or superframe-aligned to the common egress frame pulse, CEFP, via the CEMFP bit in the Master Egress Slave Mode Serial Interface Configuration register. The ESIG[x] signal contains the robbed-bit signaling data to be inserted into Transmit Data[x], with the four least significant bits of each channel on ESIG[x] representing the signaling state (ABCD or ABAB in T1 SF mode). EFP[x] is not available in this mode.

a) Register 006H+80H*N: T1/E1 Egress Serial Interface Mode Select

EMODE[2:0]	'000' Clock Slave: External Signaling [1]
Notes: 1. This mode is not supported in the TEMAP.	

5.2.3 Clock Slave : Clear Channel

Figure 22 Clock Slave: Clear Channel



In Clock Slave Clear Channel mode, the egress interface is clocked by the externally provided egress clock, ECLK[x]. ECLK[x] must be a 1.544 MHz clock for T1 links or a 2.048 MHz clock for E1 links. In this mode the T1/E1 framers are bypassed except for the TJAT which may or may not be bypassed depending on the setting of the TJATBYP bit in the T1/E1 Egress Line Interface Options register. Typically the TJAT would be bypassed unless jitter attenuation is required on ECLK[x].

a) Register 006H+80H*N: T1/E1 Egress Serial Interface Mode Select

EMODE[2:0]	'01X' Clock Slave: Clear Channel

5.3 Ingress Timing Options

The TEMUX/TEMAP/TECT3 supports the following INGRESS Timing Options:

- Clock Master: NxChannel (Not Supported for TEMAP)
- Clock Master: Full T1/E1 (Not Supported for TEMAP)
- Clock Master: Clear Channel
- Clock Slave: External Signaling (Not Supported for TEMAP)
- Clock Slave: H-MVIP *Please refer to H-MVIP section (Not Supported for TEMAP)
- Clock Master: Floating SBI *Please refer to SBI section
- Clock Slave: Synchronized SBI *Please refer to SBI section

5.3.1 Ingress Clock Master Options

a) Register 009H+80H*N: T1/E1 Serial Interface Configuration

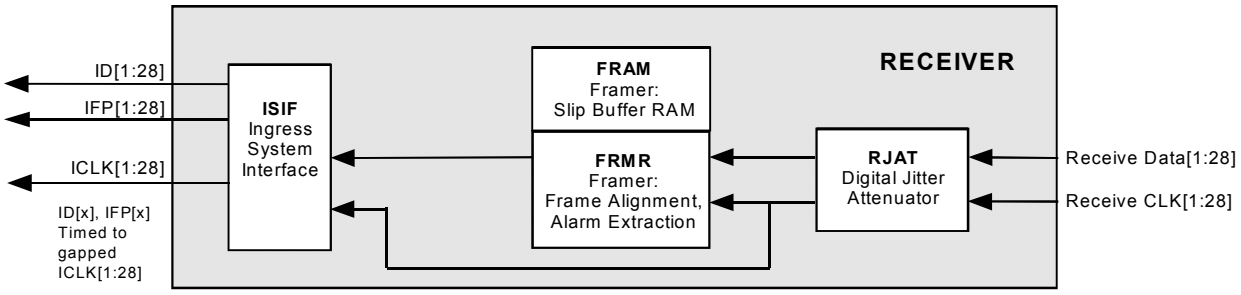
IMFP [1]	'0' IFP[x] indicates a frame alignment '1' IFP[X] indicates a frame boundary either every 12 (SF) or 24 (ESF) in T1 modes. Indicates a Multiframe every 16 frames in E1
IFPINV [1]	'0' IFP[x] is normally low and pulses high to indicate a frame boundary '1' IFP[x] is normally high and pulses low to indicate a frame boundary
IDE	'0' ID[x] is updated on ICLK[x] rising edge. '1' ID[x] is updated on ICLK[x] falling edge.
IFE [1]	'0' IFP[x] is updated on rising edge of ICLK[x]. '1' IFP[x] is updated on falling edge of ICLK[x].
Notes: 1. This bit is not supported for the TEMAP.	

b) Register 007H+80H*N: T1/E1 Egress Parity Enable (Not Supported for TEMAP)

IDPEN	'0' Ingress Data Parity disabled '1' Ingress Data Parity Enabled
IPTYP	'0' Odd Parity selected '1' Even Parity selected
IPEXTD	'0' Parity calculated over current frame '1' Parity calculated over previous frame

5.3.2 Ingress Clock Master: NxChannel (Not Supported for TEMAP)

Figure 23 Ingress Clock Master: NxChannel



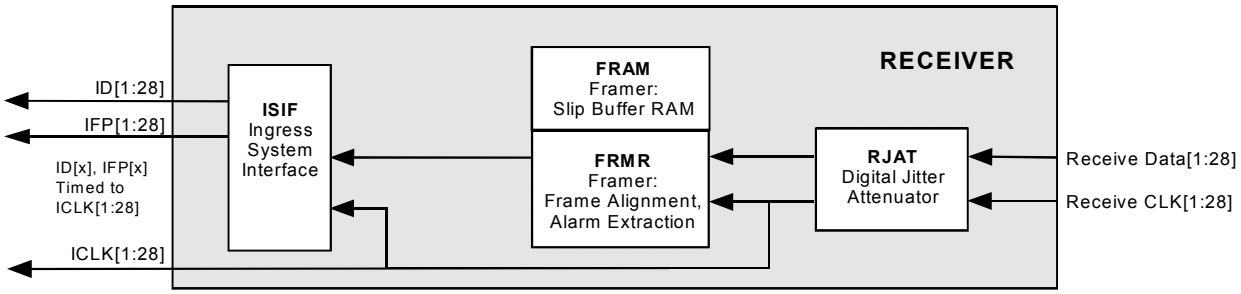
In Clock Master: NxChannel mode, ICLK[x] is a gapped version of the jitter attenuated 1.544 MHz or 2.048 MHz receive clock coming from either the M13 multiplex or SONET/SDH demapper. ICLK[x] is gapped on a per channel basis so that a subset of the 24 channels in the T1 frame or 32 channels in an E1 frame is extracted on ID[x]. IFP[x] indicates frame alignment but has no clock since it is gapped during the framing bits. The RPSC block controls channel extraction. The framing bit position is always gapped, so the number of ICLK[x] pulses is controllable from 0 to 192 pulses per T1 frame or 0 to 256 pulses per E1 frame on a per-channel basis. In this mode, demultiplexed or demapped T1 or E1 streams pass through the TEMUX/TECT3 unchanged during out-of-frame conditions. The parity functions are not usable in NxChannel mode. When the TEMUX/TECT3 is the clock master in the ingress direction, the elastic store is used to buffer between the ingress and egress clocks to facilitate per-Channel loopback.

c) Register 005H+80H*N: T1/E1 Ingress Serial Interface Mode Select

IMODE[1:0]	'10' Clock Master: NxChannel/ Full T1/E1 [1]
INXCHAN[1:0] [2]	'00' Full Frame '01' 56 kbit/s NxChannel '10' 64 kbit/s NxChannel '11' 64 kbit/s NxChannel with F bit (only valid for E1). Used to carry T1 over E1 if E1 is selected. When in NxChannel mode only those time slots with their DTRKC bit set to '0' in the Indirect RSPC registers are clocked out.
IMFPCFG [1:0] [2]	Applies to E1 Only '00' Both E1 CRC and Signaling Multiframe '01' E1 CRC Multiframe '10' E1 Signaling Multiframe '11' Both E1 CRC Signaling Multiframe
Notes: 1. This mode is not supported for the TEMAP. 2. These bits are not supported for the TEMAP.	

5.3.3 Ingress Clock Master: Full T1/E1 (Not Supported for TEMAP)

Figure 24 Ingress Clock Master: Full T1/E1



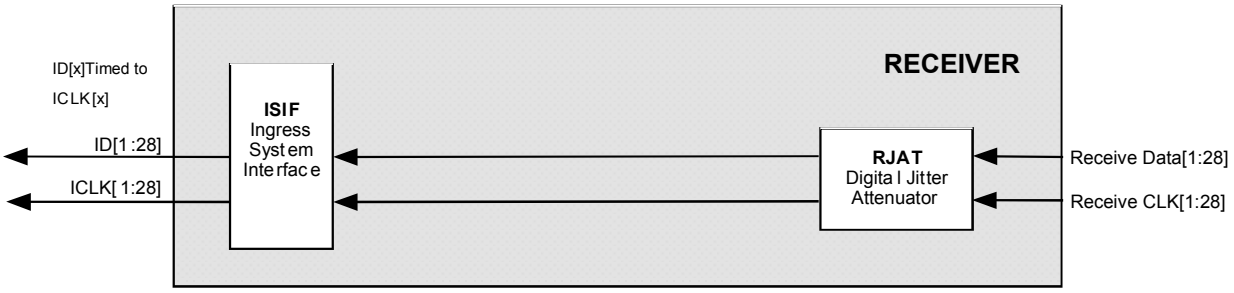
In Clock Master: Full T1/E1 mode, the elastic store is bypassed and the ingress clock (ICLK[x]) is a jitter-attenuated version of the 1.544 MHz or 2.048 MHz receive clock coming from either the M13 multiplex or SONET/SDH demapper. Jitter attenuation is selectable by the RJATBYP bit in the T1/E1 Receive Options register. ICLK[x] is pulsed for each bit in the 193 bit T1 or 256 bit E1 frame. The ingress data appears on ID[x] and the ingress frame alignment is indicated by IFP[x]. In this mode, demultiplexed or demapped T1 or E1 data passes through the TEMUX/TECT3 unchanged during out-of-frame conditions, similar to an offline framer system. When the TEMUX/TECT3 is the clock master in the ingress direction, the elastic store is used to buffer between the ingress and egress clocks to facilitate per-channel loopback.

d) Register 005H+80H*N: T1/E1 Ingress Serial Interface Mode Select

IMODE[1:0]	'10' Clock Master: NxChannel/ Full T1/E1 [1]
INXCHAN[1:0] [2]	'00' Full Frame '01' 56 kbit/s NxChannel '10' 64 kbit/s NxChannel '11' 64 kbit/s NxChannel with F bit (only valid for E1). Used to carry T1 over E1 if E1 is selected. When in NxChannel mode only those time slots with their DTRKC bit set to '0' in the Indirect RSPC registers are clocked out.
IMFPCFG [0:1] [2]	Applies to E1 Only '00' Both E1 CRC and Signaling Multiframe '01' E1 CRC Multiframe '10' E1 Signaling Multiframe '11' Both E1 CRC Signaling Multiframe
Notes: 1. This mode is not supported for the TEMAP. 2. These bits are not supported for the TEMAP.	

5.3.4 Ingress Clock Master: Clear Channel

Figure 25 Ingress Clock Master: Clear Channel



In Clock Master: Clear Channel mode, the elastic store is bypassed and the ingress clock (ICLK[x]) is a jitter attenuated version of the 1.544 MHz or 2.048 MHz receive clock coming from either the M13 multiplex or SONET/SDH demapper. The ingress data appears on ID[x] which no frame alignment indication. Per channel loopbacks are not available in clear channel mode.

a) Register 005H+80H*N: T1/E1 Ingress Serial Interface Mode Select

IMODE[1:0]	'11' Clock Master: Clear Channel

b) Register 002H+80H*N: T1/E1 Receive Option

RCVCLRCH [1]	'1' Receive Framer is bypassed. '0' Receive Framer is not bypassed. (This must be set to '1' when using the unframed tributary type with the SBI Bus or when using the Clock Master Serial Mode with serial clock and data. When using framed tributary types over SBI this must be set to '0')
Notes: 1. This bit is not supported for the TEMAP.	

5.4 Ingress Clock Slave Options

a) Register 009H+80H*N: T1/E1 Serial Interface Configuration

IMFP [1]	'0' IFP[x] indicates a frame alignment '1' IFP[X] indicates a frame boundary either every 12 (SF) or 24 (ESF) in T1 modes. Indicates a Multiframe every 16 frames in E1
IFPINV [1]	'0' IFP[x] is normally low and pulses high to indicate a frame boundary '1' IFP[x] is normally high and pulses low to indicate a frame boundary
IDE	'0' ID[x] and ISIG[x] is updated on CICLK rising edge. '1' ID[x] and ISIG[x] are updated on CICLK falling edge.
IFE [1]	'0' IFP[x] is updated on rising edge of CICLK '1' IFP[x] is updated on falling edge of CICLK
Notes: 1. This bit is not supported for the TEMAP.	

b) Register 0006H: Master Common Ingress Serial and H-MVIP Interface Configuration (Not Supported for TEMAP)

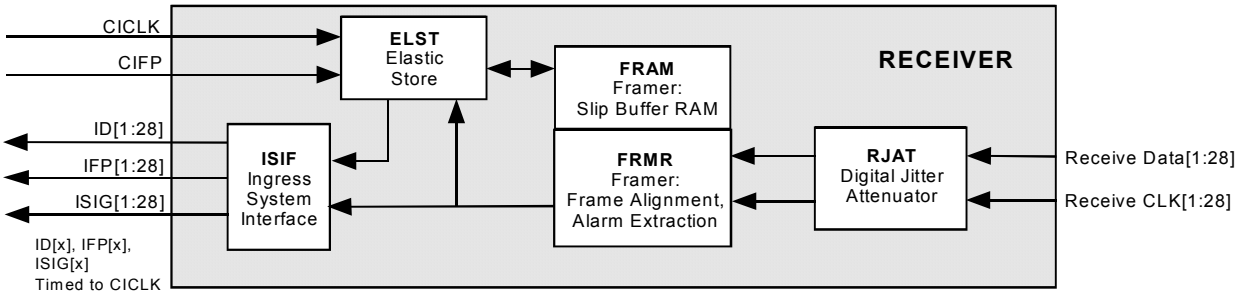
CIFE/CMVIFE	'0' CIFP is sampled on falling edge of CECLK. '1' CIFP is sampled on rising edge of CECLK.
CIFPINV/CMVIFPINV	'0' CIFP is normally low and pulses high to indicate a frame boundary. '1' CIFP is normally high and pulses low to indicate a frame boundary.
CICLK2M	'0' CICLK is a 1.544MHz clock for T1 '1' CICLK is a 2.048MHz clock used to clock for T1.

c) Register 007H+80H*N: T1/E1 Egress Parity Enable (Not Supported for TEMAP)

IDPEN	'0' Ingress Data parity is not generated '1' Ingress Data parity is generated
IPTYP	'0' Odd Parity selected '1' Even Parity selected
IPEXTD	'0' Parity calculated over current frame '1' Parity calculated over previous frame
ISPEN	'0' Ingress Parity is not generated over ISIG[x] '1' Ingress Parity is generated over ISIG[x]

5.4.1 Ingress Clock Slave: External Signaling (Not Supported for TEMAP)

Figure 26 Ingress Clock Slave: External Signaling



In Clock Slave External Signaling mode, the elastic store is enabled to permit CICLK to specify the ingress-side timing. The ingress data on ID[x] and signaling ISIG[x] are bit aligned to the 1.544 MHz or 2.048 MHz common ingress clock (CICLK) and are frame aligned to the common ingress frame pulse (CIFP). CICLK can be enabled to be a 1.544 MHz clock or a 2.048 MHz clock. ISIG[x] contains the robbed-bit signaling state (ABCD or ABAB) in the lower four bits of each channel. IFP[x] indicates either the frame or superframe alignment on ID[x].

a) Register 005H+80H*N: T1/E1 Ingress Serial Interface Mode Select

IMODE[1:0]	'00' Clock Slave: External Signaling [1]
IMFPCFG [1:0] [2]	Applies to E1 Only '00' Both E1 CRC and Signaling Multiframe '01' E1 CRC Multiframe '10' E1 Signaling Multiframe '11' Both E1 CRC Signaling Multiframe
Notes: 1. This mode is not supported for the TEMAP. 2. These bits are not supported for the TEMAP.	

6 T1 Mode Set-up

The TEMUX/TEMAP/TECT3 supports:

- SF mode
- ESF mode
- Unframed mode
- J1 Framed mode

6.1 T1 Global Configuration

a) Register 0001: Global Configuration

E1/T1B	'0' Configured as 28 T1 Framers
SYSOPT[2:0]	'000' Serial Clock and Data Interface '001' H-MVIP Interface (only valid for High Density Framer Mode) [1] '011' SBI Interface with H-MVIP CAS or CCS Interface (only valid for High Density Framer mode). [1] '010' SBI Interface. '1XX' Serial Clock and Data Interface with CCS H-MVIP Interface. (Only valid for High Density Framer Mode). [1]
LINEOPT[1:0] [2]	'1X' set if using T1/E1 Mapper '00' for DS3 LIU
OPMODE[1:0]	'00' High Density Framer Mode [1] (All 28 T1 framers are active) '01' Mapper/Multiplexer Mode (All 28 T1 framers are turned off. Behaves as a 28 T1 Mapper or as PM8313 D3MX with T1 PMON) '10' Transmux Mode [2] (Must set SYSOPT[2:0] = 010 for Transmux mode) (All 28 T1 framers handle unframed data and are used for PMON)
Notes: 1. This mode is not supported for the TEMAP. 2. These bits are not supported for the TECT3.	

b) Register 000H+80*N:T1/E1 Master Configuration

RESET	If set to '1' then that slice of the T1 framer is held in RESET
PMONRST	If set to '1' then that PMON slice of that T1 framer is held in RESET

c) Register 0018H+80*N: RX-ELST Configuration (Not Supported for TEMAP)

IR	'0' for T1 Mode
OR	'0' for T1 Mode

d) Register 005H+80*N:T1/E1 Ingress Serial Interface Mode Select

ALTIFP [1]	'1' required for T1 SF mode over SBI in asynchronous mode configuration, otherwise as selected in section 5.2
Notes: 1. This bit is not supported for the TEMAP.	

e) Register 001CH+80*N: TX-ELST Configuration (Not Supported for TEMAP)

IR	'0' for T1 Mode
OR	'0' for T1 Mode

f) Register 005CH+80*N: RX-SIG-ELST Configuration (Not Supported for TEMAP)

IR	'0' for T1 Mode
OR	'0' for T1 Mode

g) Register 002H+80H*N T1/E1 Receive Options

RJATBYP	'0' Receive Jitter Attenuator Active MUST be set to '0' for proper operation

6.2 RJAT and TJAT Jitter Attenuator Settings for T1

The RJAT and TJAT Jitter attenuator should be correctly set up for SF and ESF modes.

6.2.1 Transmit and Receive Jitter Attenuators

For proper operations, the TJAT and RJAT must first be centered. The following sequence of register operations centers the TJAT and RJAT. This sequence should be preformed in the following order one framer at a time. The following procedure should be followed for DS3 multiplexing mode. For VT/TU Mapping mode please refer to section 16.1.1.

TJAT Centering Procedure

a) Register 0017H + 80H*N TJAT Configuration

CENT	Set to ‘0’
LIMIT	Set to ‘0’
SYNC	Set to ‘1’
Reserved Bits	Set to ‘1’

b) Register 15H + 80H*N TJAT Jitter Attenuator Divider N1 Control

N1[7:0]	Set to 2FH

c) Register 16H + 80H*N TJAT Divider N2 Control

N2[7:0]	Set to 2FH

d) Register 0017H + 80H*N TJAT Configuration

CENT	Set to ‘0’
LIMIT	Set to ‘0’
SYNC	Set to ‘0’
Reserved Bits	Set to ‘1’

Note: When CTCLK is not equal to the line rate for T1, i.e. is some multiple of 8kHz, the N1 value should equal (CTCLK/8kHz – 1) and then be converted to hexadecimal. N2 should be C0H in this case.

RJAT Centering Procedure

a) Register 0013H + 80H*N RJAT Configuration

CENT	Set to ‘0’
LIMIT	Set to ‘0’
SYNC	Set to ‘1’
Reserved Bits	Set to ‘1’

b) Register 11H + 80H*N RJAT Jitter Attenuator Divider N1 Control

N1[7:0]	Set to 2FH

c) Register 12H + 80H*N RJAT Divider N2 Control

N2[7:0]	Set to 2FH

d) Register 0013H + 80H*N RJAT Configuration

CENT	Set to ‘0’
LIMIT	Set to ‘0’
SYNC	Set to ‘0’
Reserved Bits	Set to ‘1’

6.3 T1 SF Mode

a) Register 004H+80H*N T1/E1 Egress Line Interface Configuration

ESF/SF Mode [1]	‘0’ SF mode is set (The ALTIFP bit in T1/E1 Ingress Serial Interface Mode Select register must be set to 1 when The T1 framer is in SF mode and the SBI bus is being used)
Notes: 1. This bit is not supported for the TEMAP.	

b) Register 0068H+80H*N T1 XBAS Configuration (Not Supported for TEMAP)

ESF	‘0’ for SF

c) Register 006CH+80H*N T1 FRMR Configuration

ESF	‘0’ for SF

d) Register 0060H+80H*N T1 ALMI Configuration

ESF	‘0’ for SF

e) Register 0058H+80H*N: SIGX Configuration (COSS=0) (Not Supported for TEMAP)

ESF	‘0’ for SF

6.4 T1 ESF Mode

a) Register 004H+80H*N T1/E1 Egress Line Interface Configuration

ESF/SF Mode [1]	‘1’ ESF Mode is set.
Notes: 1. This bit is not supported for the TEMAP.	

b) Register 0068H+80H*N T1 XBAS Configuration (Not Supported for TEMAP)

ESF	'1' for ESF

c) Register 006CH+80H*N T1 FRMR Configuration

ESF	'1' for ESF

d) Register 0060H+80H*N T1 ALMI Configuration

ESF	'1' for ESF

e) Register 0058H+80H*N: SIGX Configuration (COSS=0) (Not Supported for TEMAP)

ESF	'1' for ESF

6.5 T1 Unframed Mode (Not Supported for TEMAP)

a) Register 002H+80H*N: T1/E1 Receive Options

UNF [1]	'1' for Unframed T1 data. (The Receive Framer is disabled and the recovered data passes through the device)
RCVCLRCH [1]	'1' for Clear channel data (The Framer is bypassed but still monitors receive stream.)
Notes: 1. This bit is not supported for the TEMAP.	

b) Register 004H+80H*N: T1/E1 Egress Line Interface Configuration

TXCLRCH [1]	'1' for Clear channel data
Notes: 1. This bit is not supported for the TEMAP.	

c) Register 00AH+80H*N: T1/E1 Transmit Framing and Bypass Options (Not Supported for TEMAP)

FDIS	'1' for Unframed T1 data. (The Transmit Framer is disabled and the transmit data passes through the device)

6.6 J1 Mode

The settings for J1 mode are based on the settings for ESF or SF mode. Please refer to the settings of ESF and SF modes above.

a) Register 0068H+80H*N: T1 XBAS Configuration (Not Supported for TEMAP)

JPN	‘1’’ Selects the Japanese Variation of the standard framing formats. If ESF mode is set this complies with TTC JT- G704. If SF mode is set the framing bit of frame 12 is forced to ‘1’ when Yellow Alarm is declared.

b) Register 006CH+80H*N: T1 FRMR Configuration

JPN	‘1’’ Selects the Japanese Variation of the standard framing formats. If ESF mode is set this complies with TTC JT- G704. If SF mode is set the framing bit of frame 12 carries a far end receive failure alarm

7 E1 Mode Set-up

The TEMUX/TEMAP/TECT3 supports the following E1 modes:

- E1 Basic Framing
- E1 CRC-4 Framing
- E1 Signaling Multi Frame (CAS)
- E1 CRC-4 and Signaling Multi Frame (CAS)

7.1 E1 Global Configuration

a) Register 0001: Global Configuration

E1/T1B	'1' Configured as 21 E1 Framers
SYSOPT[2:0]	'000' Serial Clock and Data Interface '001' H-MVIP Interface (only valid for High Density Framer Mode.) [1] '011' SBI Interface with CAS or CCS H-MVIP Interface (only valid for High Density Framer mode, not valid in G.747 mode.) [1] '1XX' Serial Clock and Data Interface with CCS H-MVIP Interface. (Only valid for High Density Framer Mode). [1]
LINEOPT[1:0] [2]	'1X' set if using T1/E1 Mapper
OPMODE[1:0]	'00' High Density Framer Mode [1] (All 21 E1 framers are active) '01' Mapper/ Multiplexer Mode (All 21 E1 framers are turned off. Behaves as a 21 E1 Mapper or as PM8313 D3MX) and E1 PMON.
Notes: 1. This mode is not supported for the TEMAP. 2. These bits are not supported for the TECT3.	

b) Register 000H+80*N: T1/E1 Master Configuration

RESET	If set to '1' then that slice of the E1 framer is held in RESET. If TEMUX/TEMAP/TECT3 is in DS3 MUX to G.747 then slices via N=4,8,12,16,20,24, 28 must be in RESET state.
PMONRST	If set to '1' then that PMON slice of that E1 framer is held in RESET

c) Register 005H+80*N: T1/E1 Ingress Serial Interface Mode Select

IMFPCFG[1:0] [1]	'01' for E1 over SBI connected to FREEDM devices. '10' for E1 over SBI connected to AAL1gator devices Otherwise as selected in section 5.2
Notes: 1. These bits are not supported for the TEMAP.	

d) Register 0018H+80*N: RX-ELST Configuration (Not Supported for TEMAP)

IR	'1' for E1 Mode
OR	'1' for E1 Mode

e) Register 001CH+80*N: TX-ELST Configuration (Not Supported for TEMAP)

IR	'1' for E1 Mode
OR	'1' for E1 Mode

f) Register 005CH+80*N: RX-SIG-ELST Configuration (Not Supported for TEMAP)

IR	'1' for E1 Mode
OR	'1' for E1 Mode

7.1.1 Transmit and Receive Jitter Attenuators

For proper operations, the TJAT and RJAT must first be centered. The following sequence of register operations centers the TJAT and RJAT. This sequence should be preformed in the following order one framer at a time. The following procedure should be followed for DS3 multiplexing mode(G.747) only. For VT/TU Mapping mode please refer to section 16.1.1.

TJAT Centering Procedure

a) Register 0017H + 80H*N TJAT Configuration

CENT	Set to '0'
LIMIT	Set to '0'
SYNC	Set to '1'
Reserved Bits	Set to '1'

b) Register 15H + 80H*N TJAT Jitter Attenuator Divider N1 Control

N1[7:0]	Set to FFH

c) Register 16H + 80H*N TJAT Divider N2 Control

N2[7:0]	Set to FFH

d) Register 0017H + 80H*N TJAT Configuration

CENT	Set to '0'
LIMIT	Set to '0'
SYNC	Set to '0'
Reserved Bits	Set to '1'

Note: When CTCLK is not equal to the line rate for E1, i.e. is some multiple of 8kHz, the N1 value should equal (CTCLK/8kHz – 1) and then be converted to hexadecimal. N2 should be FFH in this case.

RJAT Centering Procedure

a) Register 0013H + 80H*N RJAT Configuration

CENT	Set to '0'
LIMIT	Set to '0'
SYNC	Set to '1'
Reserved Bits	Set to '1'

b) Register 11H + 80H*N RJAT Jitter Attenuator Divider N1 Control

N1[7:0]	Set to FFH

c) Register 12H + 80H*N RJAT Divider N2 Control

N2[7:0]	Set to FFH

d) Register 0013H + 80H*N RJAT Configuration

CENT	Set to '0'
LIMIT	Set to '0'
SYNC	Set to '0'
Reserved Bits	Set to '1'

7.2 E1 Basic Mode

a) Register 0060H+80H*N: E1 FRMR Frame Alignment Options

CRCEN	'0' Disables searching for CRC Multiframe.
CASDIS	'1' Disables CAS.
REFR	'0' Set to '1' then '0' to reframe to the incoming signal.
REFRDIS	'0' Allows reframing to occur

b) Register 0070H+80H*N: E1 TRAN Configuration (Not Supported for TEMAP)

SIGEN, DLEN	Set both bits to '0' to cause signal insertion to be disabled and TS16 data is taken directly from the egress data.
GENCRC	Set to '0' disables CRC Generation
INDIS	'0' International Bits (CRC-4 Bits) in TS0 are inserted from E1-TRAN International Bits Control Register '1' International Bits Taken from egress data
XDIS	'0' Extra Bits in TS16 are inserted from the E1 TRAN Extra Bits Control Register.
FEBEDIS	Refer to the datasheet for settings

7.3 E1 CRC-4 Multi-Frame Mode

a) Register 0060H+80H*N: E1 FRMR Frame Alignment Options

CRCEN	'1' Enables searching for CRC-4 Multiframe.
CASDIS	'1' Disables FRAMER to frame to Channel Associated Signaling Multiframe
C2NCIWCK	'1' Enables CRC Multiframe Alignment search in CRC to non CRC Interworking Mode.
REFCRCEN	'1' Enables excessive CRC errors to force re synchronization to a new frame alignment.

b) Register 0070H+80H*N: E1 TRAN Configuration (Not Supported for TEMAP)

SIGEN, DLEN	Set both bits to ‘0’ to cause signal insertion to be disabled and TS16 data is taken directly from the egress data.
GENCRC	‘1’ Enables CRC Generation
INDIS	‘0’ International Bits in TS0 are inserted from E1-TRAN International Bits Control Register
XDIS	‘0’ Extra Bits in TS16 are inserted from the E1 TRAN Extra Bits Control Register.
FEBEDIS	‘0’ Normal operation

7.4 E1 Signaling Multi-Frame (CAS) Mode

a) Register 0060H+80H*N: E1 FRMR Frame Alignment Options

CRCEN	‘0’ Disables searching for CRC-4 Multiframe.
CASDIS	‘0’ Enables searching for CAS multiframe

b) Register 0070H+80H*N: E1 TRAN Configuration (Not Supported for TEMAP)

SIGEN, DLEN	Both bits to ‘1’ CAS enabled. TS16 data is taken from external pins or via software registers depending on setting of Global Configuration Register.
GENCRC	‘0’ Disables CRC Generation
INDIS	‘0’ International Bits in TS0 are inserted from E1-TRAN International Bits Control Register ‘1’ International Bits Taken from Egress Data
XDIS	‘0’ Extra Bits in TS16 are inserted from the E1 TRAN Extra Bits Control Register. ‘1’ Extra Bits Taken from Egress Data
FEBEDIS	‘0’ Normal operation

7.5 E1 CRC-4 Multiframe and Signaling Multi-Frame (CAS) Mode

a) Register 0060H+80H*N: E1 FRMR Frame Alignment Options

CRCEN	'1' Enables searching for CRC-4 Multiframe.
CASDIS	'0' Enables FRAMER to frame to Channel Associated Signaling Multiframe
C2NCIWCK	'1' Enables CRC Multiframe Alignment search in CRC to non CRC Interworking Mode.
REFCRCEN	'1' Enables excessive CRC errors to force re synchronization to a new frame alignment.

b) Register 0070H+80H*N: E1 TRAN Configuration (Not Supported for TEMAP)

SIGEN, DLEN	Both bits to '1' CAS enabled. TS16 data is taken from external pins or via software registers depending on setting of Global Configuration Register.
GENCRC	'1' Enables CRC Generation
INDIS	'0' International Bits in TS0 are inserted from E1-TRAN International Bits Control Register
XDIS	'0' Extra Bits in TS16 are inserted from the E1 TRAN Extra Bits Control Register.
FEBEDIS	'0' Normal operation

7.6 E1 Unframed Mode (Not Supported for TEMAP)

a) Register 002H+80H*N: T1/E1 Receive Options

UNF [1]	'1' for Unframed E1 data. (The Receive Framer is disabled and the recovered data passes through the device)
RCVCLRCH [1]	'1' for Clear channel data (Same as in T1 mode)
Notes: 1. This bit is not supported for the TEMAP.	

b) Register 00AH+80H*N: T1/E1 Transmit Framing and Bypass Options (Not Supported for TEMAP)

FDIS	'1' for Unframed E1 data. (The Transmit Framer is disabled and the transmit data passes through the device)

c) Register 004H+80H*N: T1/E1 Egress Line Interface Configuration

TXCLRCH [1]	'1' for Clear channel data
Notes: 1. This bit is not supported for the TEMAP.	

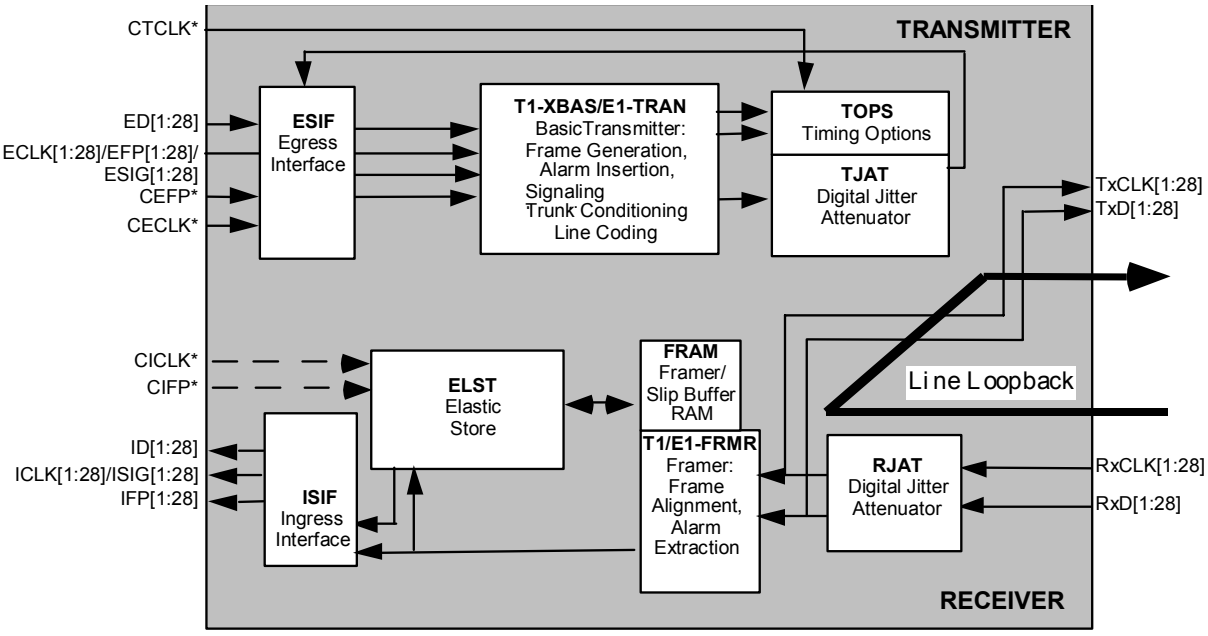
7.7 T1/E1 Loopback Modes

The TEMUX/TEMAP/TECT3 provides three loopback modes for T1/E1 links to aid in network and system diagnostics. The internal T1/E1 line loopback can be initiated at any time via the µP interface, but is usually initiated once an inband loopback activate code is detected. The system Diagnostic Digital loopback can be initiated at any time by the system via the µP interface to check the path of system data through the framer. The payload can also be looped-back on a per-DS0 basis to allow network testing without taking an entire DS1 off-line.

7.7.1 T1/E1 Line Loopback

T1/E1 Line loopback is initiated by setting the LLOOP bit to a 1 in the T1/E1 Diagnostics register (000DH + N*80H, N=1 to 28). When in line loopback mode the appropriate T1/E1 framer in the TEMUX/TEMAP/TECT3 is configured to internally connect the jitter-attenuated clock and data from the RJAT to the transmit clock and data (shown as TxD[x] and TxCLK[x] in the line loopback diagram) going to the M13 mux and SONET/SDH mapper. The RJAT may be bypassed if desired. Conceptually, the data flow through a single T1/E1 framer in this loopback condition is illustrated in Figure 27

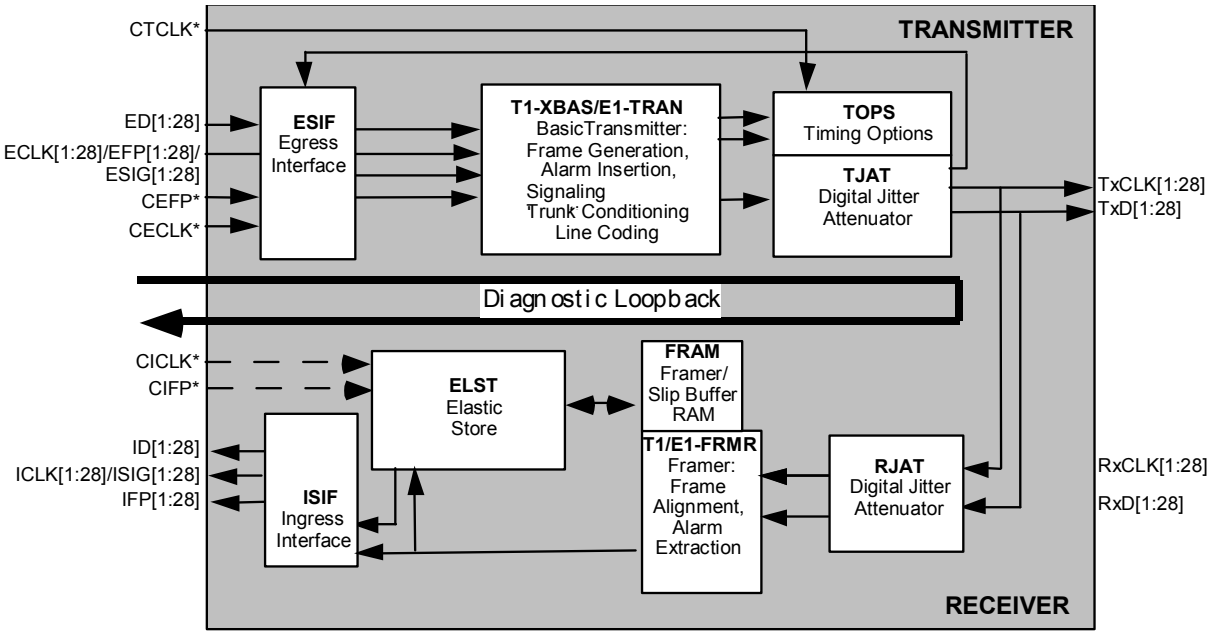
Figure 27 T1/E1 Line Loopback



7.7.2 T1/E1 Diagnostic Digital Loopback

When Diagnostic Digital loopback is initiated, by writing a 1 to the DLOOP bit in the T1/E1 Diagnostics register (000DH + N*80H, N=1 to 28), the appropriate T1/E1 framer in the TEMUX/TEMAP/TECT3 is configured to internally connect its transmit clock and data (shown as TxD[x] and TxCLK[x] in the diagnostic loopback figure) to the receive clock and data (shown as RxD[x] and RxCLK[x] in the diagnostic loopback figure) The data flow through a single T1/E1 framer in this loopback condition is illustrated in Figure 28

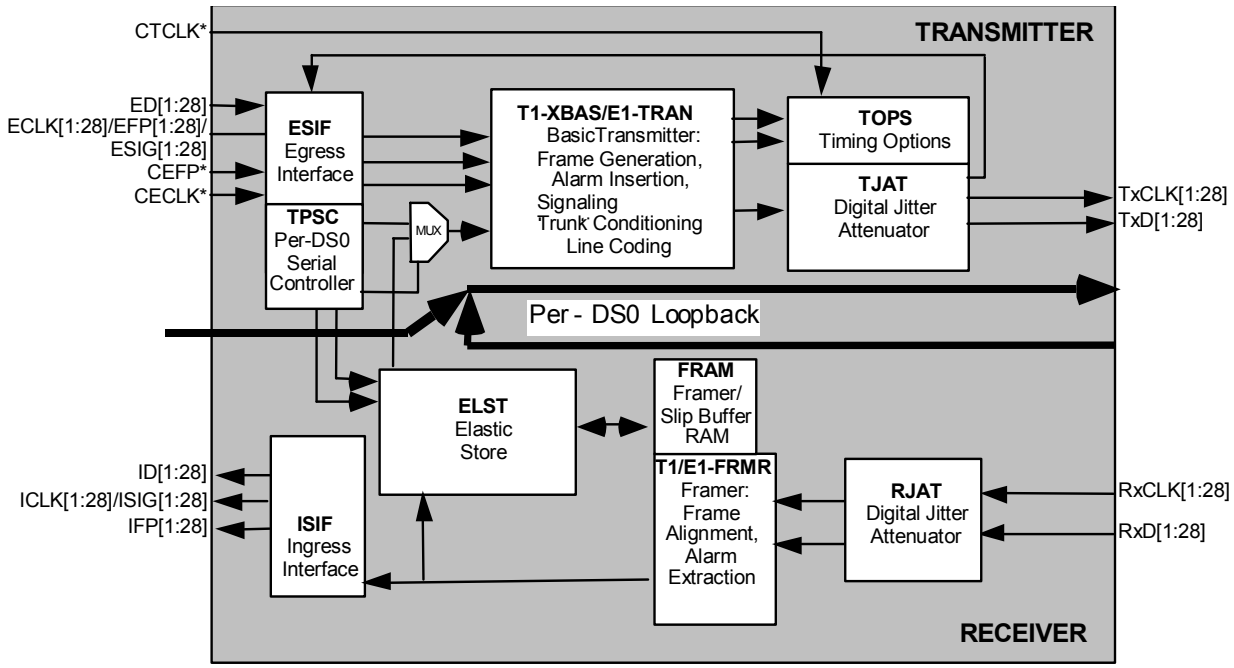
Figure 28 T1/E1 Diagnostic Digital Loopback



7.7.3 Per-Channel Loopback (Not Supported for TEMAP)

The T1/E1 payload may be looped-back on a per-channel basis through the use of the TPSC. If all channels are looped-back, the result is very similar to Payload Loopback on other PMC framers. In order for per-channel loopback to operate correctly, the Ingress Interface must be in Clock Master mode, or else CIFP and CICLK must be connected to CEFP and CECLK, respectively. The LOOP bit must be set to logic 1 in the TPSC Internal Registers for each channel desired to be looped back, and the PCCE bit must be set to logic 1 in the TPSC Configuration register. When all these configurations have been made, the ingress DS0s or timeslots selected will overwrite their corresponding egress channels; the remaining egress channels will pass through intact. Note that because the egress and ingress streams will not be superframe aligned, that any robbed-bit signaling in the ingress stream may not fall in the correct frame once looped-back, and that egress robbed-bit signaling will overwrite the looped-back channel data if signaling insertion is enabled. The data flow in per-channel loopback is illustrated in Figure 29

Figure 29 Per-Channel Loopback

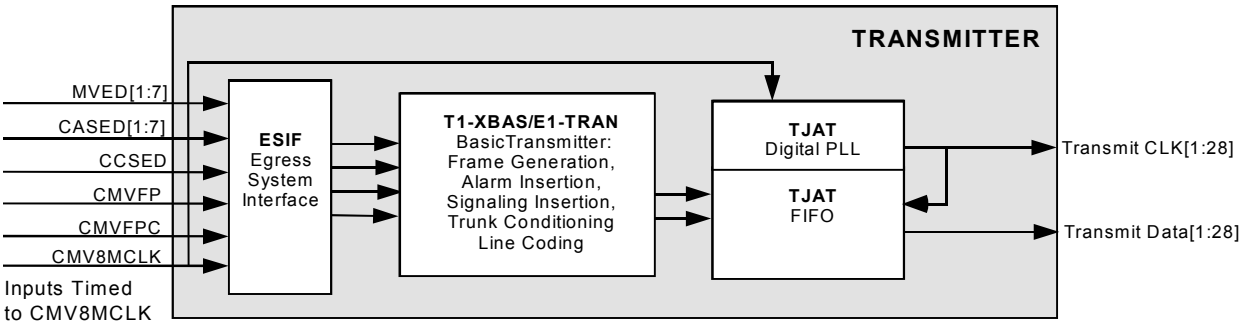


8 H-MVIP Set-up and Timing (Not Supported for TEMAP)

The H-MVIP system interface is not available on the TEMAP. This entire section does not apply to the TEMAP.

8.1.1 H-MVIP Ingress Interface Set-up (Clock Slave)

Figure 30 H-MVIP Ingress Interface Set-up (Clock Slave)



When Clock Slave: H-MVIP mode is enabled a 8.192Mb/s H-MVIP egress interface multiplexes up to 672 channels from 28 T1s or 21 E1s, up to 672 channel associated signaling (CAS) channels from 28 T1s or 21 E1s and common channel signaling from up to 28 T1s or 21 E1s. The H-MVIP interfaces use common clocks, CMV8MCLK and CMVFPC, and frame pulse, CMVFPB, for synchronization.

Seven H-MVIP data signals, MVED[1:7], share pins with serial PCM data inputs, ED[x], to provide H-MVIP access for up to 672 data channels. The H-MVIP mapping is fixed such that each group of four nearest neighbor T1 or E1 links makes up the individual 8.192Mb/s H-MVIP signal. The multiplexed data input is shared with the lowest numbered T1 or E1 serial PCM link in the bundle, for example MVED[2] combines the DS0s or timeslots of ED[5,6,7,8] and is pin multiplexed with ED[5]. This mode is selected when the SYSOPT[2:0] bits in the Global Configuration register are set to H-MVIP.

A separate seven-signal H-MVIP interface is for access to the channel associated signaling for 672 channels. The CAS H-MVIP interface is time division multiplexed exactly the same way as the data channels. The CAS H-MVIP is synchronized with the H-MVIP data channels when SYSOPT[2:0] is set to H-MVIP mode. Over a T1 or E1 multi-frame the four CAS bits per channel are repeated with each data byte. Four stuff bits are used to pad each CAS nibble (ABCD bits) out to a full byte in parallel with each data byte. The egress CAS H-MVIP interface, CASED[1:7], is multiplexed with seven serial PCM egress data pins, ED[2,6,10,14,18,22,26].

The CAS H-MVIP interface can be used in parallel with the SBI Add bus as an alternative method for accessing the CAS bits while data transfer occurs over the SBI bus. This is selected when the SYSOPT[2:0] bits in the Global Configuration register are set to “SBI Interface with CAS or CCS H-MVIP Interface” and the ECCSEN bit in the T1/E1 Egress Serial Interface Mode Select register is set to 0.

A separate H-MVIP interface consisting of a single signal is used to time division multiplex the common channel signaling (CCS) for all T1s and E1s and additionally the V5 channels in E1 mode. The CCS H-MVIP interface, CCSED, is not multiplexed with any other pins. CCSED can be used in parallel with the Clock Slave: H-MVIP mode when SYSOPT[2:0] is set to "H-MVIP Interface" and the ECCSEN bit in the T1/E1 Egress Serial Interface Mode Select register is set to 1, a Clock Slave serial interface when SYSOPT[2:0] is set to "Serial Clock and Data Interface with CCS H-MVIP Interface", or the SBI Add bus when SYSOPT[2:0] is set to "SBI Interface with CAS or CCS H-MVIP Interface" and the ECCSEN bit is set to 1. The V5 channels in E1 mode can also be enabled over CCSEN when the ETS15EN and ETS31EN bits in the T1/E1 Egress Serial Interface Mode Select register are set to 1.

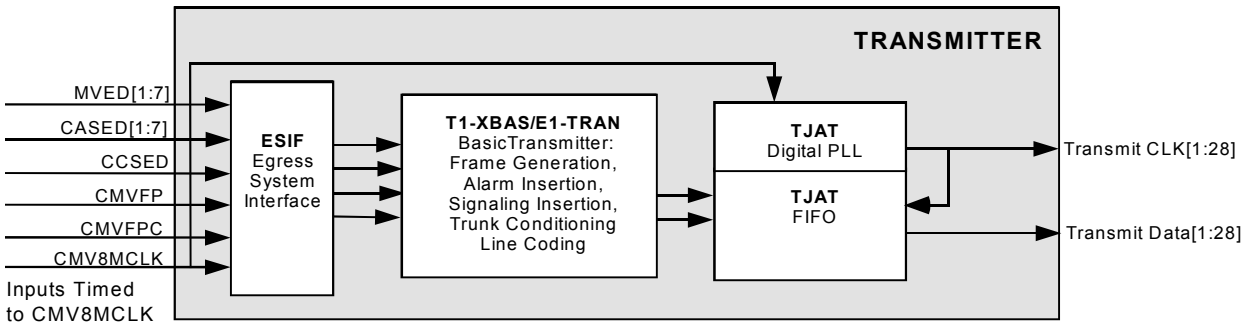
When accessing the CAS or CCS signaling via the H-MVIP interface in parallel with the SBI interface a transmit signaling elastic store is used to adapt any timing differences between the data interface and the CAS or CCS H-MVIP interface.

a) Register 0006H: Master Common Ingress Serial and H-MVIP Interface Configuration

CIFE/CMVIFE	'0' CMVFPC falling edge is used CMVFPB (Standard H-MVIP) '1' CMVFPC rising edge is used for CMVFPB
CIFPINV/CMVIFPINV	'0' CMVFB is not inverted (normally low and pulses high to indicate a frame boundary). '1' CMVFB is inverted (normally high and pulses low to indicate a frame boundary). (Standard H-MVIP)
CMVIDE	'0' Ingress signals MVID[7:0], CASID[7:0] and CCSID updated on falling edge of CMV8MCLK. (Standard H-MVIP) '1' Ingress signals MVID[7:0], CASID[7:0] and CCSID updated on rising edge of CMV8MCLK.

8.1.2 H-MVIP Egress Interface Set-up (Clock Slave)

Figure 31 H-MVIP Egress Interface Set-up (Clock Slave)



When Clock Slave: H-MVIP mode is enabled a 8.192Mb/s H-MVIP egress interface multiplexes up to 672 channels from 28 T1s or 21 E1s, up to 672 channel associated signaling (CAS) channels from 28 T1s or 21 E1s and common channel signaling from up to 28 T1s or 21 E1s. The H-MVIP interfaces use common clocks, CMV8MCLK and CMVFPC, and frame pulse, CMVFPB, for synchronization.

Seven H-MVIP data signals, MVED[1:7], share pins with serial PCM data inputs, ED[x], to provide H-MVIP access for up to 672 data channels. The H-MVIP mapping is fixed such that each group of four nearest neighbor T1 or E1 links makes up the individual 8.192Mb/s H-MVIP signal. The multiplexed data input is shared with the lowest numbered T1 or E1 serial PCM link in the bundle, for example MVED[2] combines the DS0s or timeslots of ED[5,6,7,8] and is pin multiplexed with ED[5]. This mode is selected when the SYSOPT[2:0] bits in the Global Configuration register are set to H-MVIP.

A separate seven-signal H-MVIP interface is for access to the channel associated signaling for 672 channels. The CAS H-MVIP interface is time division multiplexed exactly the same way as the data channels. The CAS H-MVIP is synchronized with the H-MVIP data channels when SYSOPT[2:0] is set to H-MVIP mode. Over a T1 or E1 multi-frame the four CAS bits per channel are repeated with each data byte. Four stuff bits are used to pad each CAS nibble (ABCD bits) out to a full byte in parallel with each data byte. The egress CAS H-MVIP interface, CASED[1:7], is multiplexed with seven serial PCM egress data pins, ED[2,6,10,14,18,22,26].

The CAS H-MVIP interface can be used in parallel with the SBI Add bus as an alternative method for accessing the CAS bits while data transfer occurs over the SBI bus. This is selected when the SYSOPT[2:0] bits in the Global Configuration register are set to “SBI Interface with CAS or CCS H-MVIP Interface” and the ECCSEN bit in the T1/E1 Egress Serial Interface Mode Select register is set to 0.

A separate H-MVIP interface consisting of a single signal is used to time division multiplex the common channel signaling (CCS) for all T1s and E1s and additionally the V5 channels in E1 mode. The CCS H-MVIP interface, CCSED, is not multiplexed with any other pins. CCSED can be used in parallel with the Clock Slave: H-MVIP mode when SYSOPT[2:0] is set to “H-MVIP Interface” and the ECCSEN bit in the T1/E1 Egress Serial Interface Mode Select register is set to 1, a Clock Slave serial interface when SYSOPT[2:0] is set to “Serial Clock and Data Interface with CCS H-MVIP Interface”, or the SBI Add bus when SYSOPT[2:0] is set to “SBI Interface with CAS or CCS H-MVIP Interface” and the ECCSEN bit is set to 1. The V5 channels in E1 mode can also be enabled over CCSEN when the ETS15EN and ETS31EN bits in the T1/E1 Egress Serial Interface Mode Select register are set to 1.

When accessing the CAS or CCS signaling via the H-MVIP interface in parallel with the SBI interface a transmit signaling elastic store is used to adapt any timing differences between the data interface and the CAS or CCS H-MVIP interface.

a) Register 0005H: Master Common Egress Serial and H-MVIP Interface Configuration

CMVEDE	'0' Egress H-MVIP signals sampled on falling edge of CMV8MCLK '1' Egress H-MVIP signals sampled on rising edge of CMV8MCLK (Standard H-MVIP)
CEFPINV	'0' CEFP is normally low and pulse high to indicate a boundary condition (Standard H-MVIP) '1' CEFP is normally high and pulses low to indicate a boundary condition

8.1.3 H-MVIP Mode Set-up

a) Register 0001H: Global Configuration

SYSOPT[2:0]	'001' H-MVIP Interface (only valid for High Density Framer Mode) '011' SBI Interface with H-MVIP CAS or CCS Interface (only valid for High Density Framer mode) '1XX' Serial Clock and Data Interface with CCS H-MVIP Interface. (Only valid for High Density Framer Mode).
LINEOPT[1:0] [1]	'1X' set if using T1/E1 Mapper '00' if DS3 LIU
OPMODE[1:0]	'00' High Density Framer Mode (All 28 T1/21 E1 framers are active)
Notes: 1. These bits are not supported for the TECT3.	

b) Register 005H+80H*N: T1/E1 Ingress Serial Interface Mode Select

ICCSSEL	'0' CAS bits for E1 or T1 over H-MVIP available over CASID[1:7] pins. '1' The T1 or E1 Common Channel Signaling Interface is available via the CCSID pin. In T1 mode the CCS channel is on DS024. In E1 Mode the CCS channel is on timeslots 16,15 and 31 (V5.2).

c) Register 006H+80H*N: T1/E1 Egress Serial Interface Mode Select

ETS31EN	E1 mode only '0' CAS for timeslot 31 is sourced from CASED pins. '1' CAS for timeslot 31 is sourced from CCSED pin. E1 mode the SIGEN/DLEN bits in the E1 TRAN Configuration register must both be set to 1 to enable CAS to be inserted. ECCSEN must also be set to '1'.
ETS15EN	E1 mode only '0' CAS for timeslot 15 is sourced from CASED pins. '1' CAS for timeslot 15 is sourced from CCSED pin . E1 mode the SIGEN/DLEN bits in the E1 TRAN Configuration register must both be set to 1 to enable CAS to be inserted. ECCSEN must also be set to '1'.
ECCSEN	'0' CAS sourced from CASED pins. '1' CAS is sourced from CCSED. In T1 Timeslot 24 is sourced and in E1 timeslot 16. In E1 mode the SIGEN/DLEN bits in the E1 TRAN Configuration register must both be set to 1 to enable CAS to be inserted.

9 Setting the Per Channel Serial E1/T1 Controllers (Not Supported for TEMAP)

The Per-Channel Serial Controllers (TPSC and RPSC) control the per-channel functions of the Transmit and Receive PCM data.

The Per-Channel Serial Controllers (TPSC and RPSC) blocks are not available in the TEMAP. This entire section does not apply to the TEMAP.

9.1 Setting the Receive Per Channel Serial E1/T1 Controllers (RPSC)

Setting the PCCE bit in RPSC Configuration Register to logic 0 should disable the output control streams. Then, all 96 locations of the RPSC must be filled with valid data. Finally, the output streams can be enabled by setting the PCCE bit in the RPSC.

The RPSC configurations should be setup when the TEMUX/TECT3 is in the ACTIVATION state. The following steps should be followed in order:

1. Disable the PCCE bit and Enable the IND bit in the RPSC Configuration Register (0030H+80H*N).
2. Program the required RPSC Configuration.
3. Enable the PCCE bit in the RPSC Configuration Register (0030H+80H*N).

The following sections discuss step 2.

9.2 Receive Per Channel Serial Controller (RSPC)

On power up, the per-channel control is normally disabled by default. Once the RPSC is configured, the PCCE bit in RPSC Configuration Register (00030H+80H*N) must be set to activate per channel control.

a) Register 0030H+80H*N: RSPC Configuration

PCCE	'0' Per channel functions are disabled. Must be set to '0' On power up '1' enables the Data Trunk Conditioning Code Byte and Signaling Trunk Conditioning Byte to modify the received data.

The RPSC Indirect Registers (PCM Data Control byte(20H-3FH), Data Trunk Conditioning Code byte(40H-5FH), and Signaling Trunk Conditioning byte(61H-7FH)) are accessible on a per-channel basis. Table 8 provides a summary of some of the control bits (in the RPSC Indirect Registers 20H-3FH: PCM Data Control byte) that must be programmed to configure the channels.

b) RPSC Indirect Registers 20H-3FH: PCM Data Control Byte

DTRKC	'0' No Trunk Conditioning Applied '1' Ingress Data is replaced by Data Trunk Conditioning Byte (40H-5FH) for the channel. When in T1/E1 Master Ingress Serial Interface Mode this also control ICLK[x] generation.
STRKC	'0' No Signaling Trunk Conditioning Applied '1' Ingress Signaling is replaced by Signaling Trunk Conditioning Byte (61H-7FH) for the channel.
DMW	No digital milliwatt pattern replaces Ingress Data.
DMWALAW	'0' If applicable if DMW='1', A-Law pattern is used. '1' If applicable if DMW='1', u-Law pattern is used.
SIGNINV	'0' No Inversion takes place '1' Most Significant Bit of data output on Ingress Data is inverted for the channel.

9.3 Direct Access Mode

Direct access mode to the RPSC is not used in the TEMUX/TEMAP/TECT3. However, direct access mode is selected by default whenever the TEMUX/TEMAP/TECT3 is reset. The IND bit within the RPSC Configuration Registers must be set to logic 1 after a reset is applied to access the indirect RPSC registers.

9.4 Indirect Access Mode

Indirect access mode is selected by setting the IND bit in the RPSC Configuration Register to logic 1. When using the indirect access mode, the status of the BUSY indication bit should be polled to determine the status of the microprocessor access: when the BUSY bit is logic 1, the RPSC is processing an access request; when the BUSY bit is logic 0, the RPSC has completed the request.

9.4.1 Indirect Write Sequence

The indirect write programming sequence for the RPSC is as follows:

1. Check that the BUSY bit in the 0031H+80H*N:RPSC µP Access Status Register is logic 0.

2. Write the channel data to the 0033H+80H*N:RPSC Channel Indirect Data Buffer register.

3. Write RWB=0 and the channel address to the 0032H+80H*N:RPSC Channel Indirect Address/Control Register.

4. Poll the BUSY bit until it goes to logic 0. The BUSY bit will go to logic 1 immediately after step 3 and remain at logic 1 until the request is complete.

5. If there is more data to be written, go back to step 1. (0031H+80H*N:RPSC µP Access Status Register).

9.4.2 Indirect Read Sequence

The indirect read programming sequence for the RPSC is as follows:

1. Check that the BUSY bit in the 0031H+80H*N:RPSC µP Access Status Register is logic 0.

2. Write RWB=1 and the channel address to the 0032H+80H*N:RPSC Channel Indirect Address/Control Register.

3. Poll the BUSY bit, waiting until it goes to logic 0. The BUSY bit will go to logic 1 immediately after step 2 and remain at logic 1 until the request is complete. (0031H+80H*N:RPSC µP Access Status Register).

4. Read the requested channel data from the 0033H+80H*N:RPSC Channel Indirect Data Buffer register.

5. If there is more data to be read, go back to step 1.

9.5 Setting the Per Channel Transmit Serial E1/T1 Controllers (TPSC)

Setting the PCCE bit in the TPSC Configuration Register to logic 0 should disable the output control streams. Then, all 96 locations of the RPSC must be filled with valid data. Finally, the output streams can be enabled by setting the PCCE bit in the TPSC

The TPSC configurations should be setup when the TEMUX/TECT3 is in the ACTIVATION state. The following steps should be followed in order:

1) Disable the PCCE bit and Enable the IND bit in the TPSC Configuration Register (0034H+80H*N).

2) Program the required TPSC Configuration.

3) Enable the PCCE bit in the TPSC Configuration Register (0034H+80H*N).

The following sections discuss step 2.

9.6 Transmit Per Channel Serial Controller (TSPC)

On power up, the per-channel control is normally disabled by default. Once the TPSC is configured, the PCCE bit in TPSC Configuration must be set to activate per channel control.

a) Register 0034H+80H*N: TSPC Configuration

PCCE	'0' Per channel functions are disabled. Must be set to '0' On power up '1' enables the Data Trunk Conditioning Code Byte and Signaling Trunk Conditioning Byte to modify the received data.

The TPSC Indirect Registers (PCM Data Control byte(20H-3FH), IDLE Control Byte(40H-5FH) and Signaling Control Byte (61H-77H)) are accessible on a per-channel basis. The Table below provides a summary of some of the control bits (in the TPSC Indirect Registers 20H-3FH:PCM Data Control byte) that must be programmed to configure the channels.

b) TPSC Indirect Registers 20H-3FH: PCM Data Control Byte

INVERT	T1 mode only '0' no effect on data '1' inverts the data
IDLE_CHAN	'0' has no effect '1' Replaces data for that byte with IDLE Control Byte register value. Only for T1 mode. In Clock Master NxChannel Egress System Mode this bit control Egress Clock generation. Useful when interface to a FREEDM device.
SIGINV	Only applicable in T1 '0' has no effect '1' Most significant bit from the Egress System Interface is inverted for that channel.
DMW	'0' No effect '1' Digital Milliwatt pattern replaces Egress System Data.
TEST	'0' No effect '1' Applies test pattern from PRBS to that time slot/channel
LOOP	'0' No effect '1' Enables per channel loopback.
ZCSO, ZCS1	Applies various Code Suppression Formats. See datasheet.

9.7 Direct Access Mode

Direct access mode to the TPSC is not used in the TEMUX/TECT3. However, direct access mode is selected by default whenever the TEMUX/TECT3 is reset. The IND bit within the TPSC Configuration Registers must be set to logic 1 after a reset is applied, to access the indirect registers.

9.8 Indirect Access Mode

Indirect access mode is selected by setting the IND bit in the TPSC Configuration Register to logic 1. When using the indirect access mode, the status of the BUSY indication bit should be polled to determine the status of the microprocessor access. When the BUSY bit is logic 1, the TPSC is processing an access request; when the BUSY bit is logic 0, the TPSC has completed the request.

9.8.1 Indirect Write Sequence

The indirect write programming sequence for the TPSC is as follows:

1. Check that the BUSY bit in the 0035H+80H*N:TPSC µP Access Status Register is logic 0.
2. Write the channel data to the 0037H+80H*N:TPSC Channel Indirect Data Buffer register.
3. Write RWB=0 and the channel address to the 0036H+80H*N:TPSC Channel Indirect Address/Control Register.
4. Poll the BUSY bit until it goes to logic 0. The BUSY bit will go to logic 1 immediately after step 3 and remain at logic 1 until the request is complete.
5. If there is more data to be written, go back to step 1. (0035H+80H*N:TPSC µP Access Status Register).

9.8.2 Indirect Read Sequence

The indirect read programming sequence for the TPSC is as follows:

1. Check that the BUSY bit in the 0035H+80H*N:TPSC µP Access Status Register is logic 0.
2. Write RWB=1 and the channel address to the 0036H+80H*N:TPSC Channel Indirect Address/Control Register.
3. Poll the BUSY bit, waiting until it goes to logic 0. The BUSY bit will go to logic 1 immediately after step 2 and remain at logic 1 until the request is complete. (0035H+80H*N:TPSC µP Access Status Register).
4. Read the requested channel data from the 0037H+80H*N:TPSC Channel Indirect Data Buffer register.
5. If there is more data to be read, go back to step 1.

10 Using the Signaling Extraction Block (SIGX) (Not Supported for TEMAP)

The Signaling Extraction (SIGX) block provides channel associated signaling (CAS) extraction from an E1 signaling multiframe or from SF and ESF T1 Formats. The SIGX block extracts the signaling bits from the received datastream and serializes the results on the Ingress Signaling output.

The Signaling Extraction (SIGX) block is not available in the TEMAP. This entire section does not apply to the TEMAP.

Control of CAS is normally disabled by default, on power-up or reset. The PCCE bit in SIGX Configuration Register (0058H+80H*N) must be set to activate per channel control. The SIGX configuration should be setup when the TEMUX/TECT3 is in the ACTIVATION state. The following steps should be followed in order:

1. Disable the PCCE and enable the IND and COSS bit (if indirect registers need to be accessed) in the SIGX Configuration Register (0058H+80*N).

2. Program the required SIGX Configuration.

3. Enable the PCCE bit in the SIGX Configuration Register (0058H+80*N). The SIGX Configuration Register (58H+80*N) can represent two registers based on how the COSS register bit is set. This is discussed below.

When COSS = 0

The SIGX indirect registers are disabled on reset and have no default value when enabled. Setting the IND bit to logic 1 and the COSS bit to logic 0 enables access to the indirect registers in the SIGX Configuration Register(58H+80*N).

When the COSS bit is set to logic 0, the SIGX register space is configured to allow indirect access to each of the 24 T1 or 30 E1 channels. The SIGX Indirect Registers (Timeslot/Channel Signaling Data (20H-3FH) and Per-Timeslot Configuration (40H-05FH)) are accessible on a per-channel basis.

Timeslot/Channel Signaling Data registers store - signaling data to be sent to the Ingress Signaling pin. These registers contain the A,B,C,D bits for the ESF and SF formats. The Per-Timeslot Configuration registers provide data conditioning in conjunction with the RPSC Data Control bytes.

When COSS = 1

When the COSS bit is set to 1, the SIGX Change of Signaling State Registers (50H-53H) are used to indicate a change of signaling state on a channel. In T1 mode, COSS bits 1 to 24 represent each of the 24 channels. In E1 mode, COSS bits 1 to 30 represent each of the 30 timeslots. These registers may be polled to determine the channel that had a signaling state change. The COSS bits are cleared when the register is read.

SIGX Indirect Register Access

The SIGX indirect registers are for the channel associated signaling from framing formats. On power-up, the per-channel control is normally disabled by default. The PCCE bit in SIGX Configuration Register (COSS=0) (58H+80*N) must be set to enable per channel control.

The “IND” bit of the SIGX Configuration Register (COSS=0) (58H+80*N) must be set to logic 1 and the COSS bit must be set to logic 0 before the software can access SIGX indirect registers. By default, on power-up or software reset, these bits are clear. Once the “IND” bit is set, the following sequence how to read a SIGX indirect register and write to a SIGX indirect register.

10.1 Reading a SIGX Indirect Register

1. Set COSS bit to ‘0’
2. Read the BUSY bit to make sure that it is set to ‘0’
3. Write the address of the signaling information to be read into Register 005AH+80H*N: SIGX Channel Indirect Address/Control. Set the RWB bit to ‘1’.
4. Wait until the BUSY bit is set ‘0’ by polling Register 0059H+80*N: SIGX Change Of Signaling State Change.
5. Read the contents of the signaling information from Register 005BH+80H*N: SIGX Channel Indirect Data Buffer.

Repeat from stage 2 onwards for further writes.

10.2 Writing to a SIGX Indirect Register

1. Set COSS bit to ‘0’
2. Read the BUSY bit to make sure that it is set to ‘0’
3. Write the contents of the signaling information into Register 005BH+80H*N: SIGX Channel Indirect Data Buffer.
4. Write the address of the signaling information to be written into Register 005AH+80*N: SIGX Channel Indirect Address/Control. Set the RWB bit to ‘0’.
5. Wait until the BUSY bit is set ‘0’ by polling Register 0059H+80*N: SIGX Change Of Signaling State Change.

Repeat from stage 2 onwards for further writes.

11 HDLC Programming (Not Supported for TEMAP)

The TEMUX/TECT3 provides one HDLC controller for each T1/E1slice, each with 128-byte transmit and receive buffers.

The HDLC controller block is not available in the TEMAP. This entire section does not apply to the TEMAP.

11.1 Using the Internal HDLC Transmitters

11.1.1 Transmit HDLC Controller

The access rate to the TDPR registers is limited by the transmit T1/E1 clock rate; therefore, it is important that they are accessed at a rate no faster than that clock.

Upon reset, setting the EN bit in the TDPR Configuration Register (0048H+80H*N) to logic 0 (default value) disables the TDPR. After making all initial configurations to the TDPR, the EN bit should be set to logic 1 to enable the TDPR. Then the FIFOCLR bit should be set and then cleared to initialize the TDPR FIFO. The TDPR is now ready to transmit.

To initialize the TDPR, the TDPR Configuration Register (0048H+80H*N) must be properly set. If FCS generation is desired, the CRC bit should be set to logic 1. If the block is to be used in interrupt driven mode, then interrupts should be enabled by setting the FULLE, OVRE, UDRE, and LFILLE bits in the TDPR Interrupt Enable (004BH+80H*N) register to logic 1.

The TDPR operating parameters in the TDPR Upper Transmit Threshold (0049H+80H*N) and TDPR Lower Interrupt Threshold (004AH+80H*N) registers should be set to the desired values. The TDPR Upper Transmit Threshold (0049H+80H*N) sets the value at which the TDPR automatically begins the transmission of HDLC packets, even if no complete packets are in the FIFO.

Transmission will continue until the current packet is transmitted and the number of bytes in the TDPR FIFO falls to, or below, this threshold level. The TDPR will always transmit all complete HDLC packets (packets with EOM attached) in its FIFO. Finally, setting the EN bit to logic 1 enables the TDPR. If no message is sent after the EN bit is set to logic 1, continuous flags will be sent.

The TDPR can be used in a polled or interrupt driven mode for the transfer of packet data. In the polled mode, the processor controlling the TDPR must periodically read the TDPR Interrupt Status (004CH+80H*N) register to determine when to write to the TDPR Transmit Data (004DH+80H*N) register. In the interrupt driven mode, the processor controlling the TDPR uses the INTB output to identify the interrupts which determine when writes can or must be done to the TDPR Transmit Data (0048H+80H*N) register.

11.1.2 Automatic Transmission Mode Using Interrupts

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold (0049H+80H*N). The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold (004AH+80H*N) should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 1 so an interrupt on INT is generated upon detection of a FIFO full state, a FIFO depth below the lower limit threshold, a FIFO overrun, or a FIFO underrun. The following procedure should be followed to transmit HDLC packets:

1. Wait for data to be transmitted. Once data is available to be transmitted, go to step 2.

2. Write the data byte to the TDPR Transmit Data (004DH+80H*N) register.

3. If all bytes in the packet have been sent, set the EOM bit in the TDPR Configuration (0048H+80H*N) register to logic 1. Proceed to step 1.

4. If there are more bytes in the packet to be sent, return to step 2.

While performing steps 1 to 4, the processor should monitor for interrupts generated by the TDPR. When an interrupt is detected, the TDPR Interrupt Routine should be executed.

The TDPR will force transmission of the packet information when the FIFO depth exceeds the threshold programmed with the UTHR[6:0] bits in the TDPR Upper Transmit Threshold (0049H+80H*N) register. Transmission will not stop until the last byte of all complete packets is transmitted and the FIFO depth is at or below the threshold limit. The user should watch the FULLI and LFILLI interrupts to prevent overruns and underruns.

11.1.3 TDPR Interrupt Routine:

The following procedure should be carried out when an interrupt is detected on INTB:

1. Read the TDPR Interrupt Status (004CH+80H*N) register.

2. If UDRI=1, then the FIFO has underrun and the last packet transmitted has been corrupted and needs to be retransmitted. When the UDRI bit transitions to logic 1, one Abort sequence and continuous flags will be transmitted. The TDPR FIFO is held in reset state. The UDRI interrupt is cleared when the TDPR Interrupt Status register (004CH+80H*N) is read.

3. If OVRI=1, then the FIFO has overflowed. The packet, which the last byte written into the FIFO belongs to, has been corrupted and must be retransmitted. Other packets in the FIFO are not affected. When an overflow occurs, the OVRI bit is set to indicate that the TPDR FIFO was already full when another data byte was written to the TPDR Transmit Data register. Either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set. The OVRI interrupt remains set until the TDPR Interrupt Status (004CH+80H*N) register is read.

   If the FIFO overflows on the packet currently being transmitted (packet is greater than 128 bytes long), the OVRI interrupt is set, an Abort signal is scheduled to be transmitted, the FIFO is emptied, and then flags are continuously sent until there is data to be transmitted. The FIFO is held in reset until a write to the TDPR Transmit Data (004DH+80H*N) register occurs. This write contains the first byte of the next packet to be transmitted.

4. If FULLI=1 and FULL=1, then the TDPR FIFO is full and no further bytes can be written. When in this state, either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit. If FULLI=1 and FULL=0, then the TDPR FIFO had reached the FULL state earlier, but has since emptied out some of its data bytes and now has space available in its FIFO for more data.

5. If LFILLI=1 and BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. If there is more data to transmit, then it should be written to the TDPR Transmit Data (004DH+80H*N) register before an underrun occurs. If there is no more data to transmit, then an EOM should be set at the end of the last packet byte. Flags will then be transmitted once the last packet has been transmitted.

   If LFILLI=1 and BLFILL=0, then the TDPR FIFO had fallen below the lower-threshold state earlier, but has since been refilled to a level above the lower-threshold level.

11.1.4 Automatic transmission mode using polling:

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold. The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold (004AH+80H*N) should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 0 since packet transmission is set to work with a periodic polling procedure. The following procedure should be followed to transmit HDLC packets:

1. Wait until data is available to be transmitted, then go to step 2.

2. Read the TDPR Interrupt Status (004CH+80H*N) register.

3. If FULL=1, the TDPR FIFO is full and no further bytes can be written.

   Continue polling the TDPR Interrupt Status (004CH+80H*N) register until either FULL=0 or BLFILL=1. Then, proceed to either step 4 or 5 depending on implementation preference.

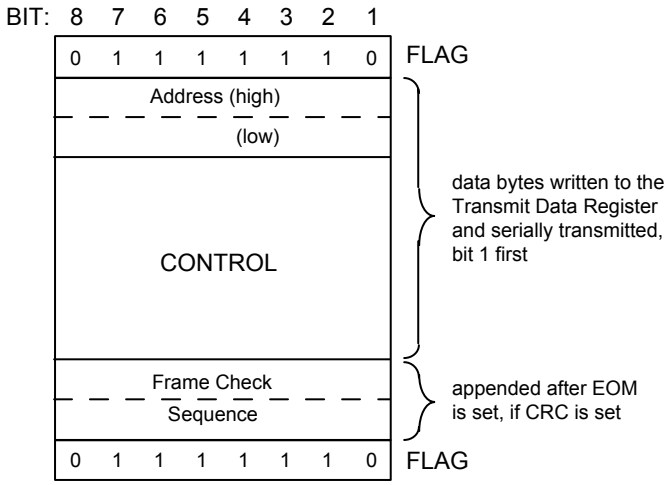
4. If BLFILL=1, the TDPR FIFO depth is below its lower threshold limit. Write the data into the TDPR Transmit Data (004DH+80H*N) register. Advance to step 6.

5. If FULL=0, the TDPR FIFO has room for at least 1 more byte to be written. Write the data into the TDPR Transmit Data (004DH+80H*N) register. Move on to step 6.

6. If more data bytes are to be transmitted in the packet, proceed to step 2.

7. If all bytes in the packet have been sent, set the EOM bit in the TDPR Configuration (0048H+80H*N) register to logic 1. Go to step 1.

Figure 32 Typical HDLC Data Frame



11.1.5 Effect of XBOC on HDLC Packets Being Transmitted

The T1 XBOC Code (0065H+80H*N) register enables the XBOC to generate a bit oriented code and selects the 8-bit code to be transmitted. If the T1 XBOC Code (004DH+80H*N) register is written with any 6-bit code other than 111111B, that code will be transmitted repeatedly in the ESF Facility Data Link overwriting any HDLC packets currently being transmitted. The XBOC is disabled when T1 XBOC Code (004DH+80H*N) register is written with the 6-bit code 111111B.

11.1.6 Use of HDLC Controller in E1 mode

When using the internal HDLC controllers in E1 mode there are some restrictions to be aware of:

- If data is inserted into a timeslot from the internal HDLC controller and the previous timeslot has an idle code byte inserted from the TPSC, the last two bits of the idle code can be corrupted. This means that if timeslot 4 has data inserted from the HDLC controller, and an idle code has been inserted in timeslot 3 from the TPSC, the least significant two bits of timeslot 3 can be corrupted. It is recommended that HDLC traffic be inserted from the backplane rather than the internal controller if idle codes are being transmitted in the preceding timeslot.
- If data is inserted into timeslot 1 from the internal HDLC controller, the least significant bit in timeslot 0 for NFAS frames only (i.e., Sa8) can be corrupted if configured to come from the backplane. The National Use Bits codeword, however, operates correctly on Sa8 if enabled. It is recommended that timeslot 1 not be used for HDLC traffic inserted from the internal controller.
- In normal operation, if a timeslot is configured for both HDLC transmission and idle code insertion, HDLC is supposed to be transmitted and the idle code ignored. It is possible in TEMUX/TECT3 for the last two bits of the HDLC data to be corrupted. To get around this, simply disable idle code insertion for that timeslot when HDLC data is being transmitted.
- Inserting HDLC data into the National bits Sa8, Sa7, Sa6, or Sa5 can cause the neighboring more significant bit to be corrupted. For example, if HDLC is inserted into Sa7, then Sa6 can be corrupted, but only if Sa6 is inserted from the backplane. The National bits are always inserted error-free when they are generated via the National Bits Codeword register of the E1-TRAN block.
- Inserting HDLC data into the Si bit in TS0 (i.e., the international bit) can cause the least significant two bits of an IDLE code in TS31 to be corrupted.

11.2 Using the Internal HDLC Receivers

On power up of the system, setting the EN bit in the Configuration Register (0040H+80H*N) to logic 0 disables the RDLC. The Interrupt Control Register (0041H+80H*N) should then be initialized to enable the INTB output and to select the FIFO buffer fill level at which an interrupt will be generated. If the INTE bit is not set to logic 1, the Status Register (0042H+80H*N) must be continuously polled to check the interrupt status (INTR) bit.

After the Interrupt Control Register (0041H+80H*N) has been written, the RDLC can be enabled at any time by setting the EN bit in the Configuration Register (0040H+80H*N) to logic 1. When the RDLC is enabled, it will assume the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated, and a dummy byte will be written into the FIFO buffer providing alignment of link up status with the data read from the FIFO. When an abort character is received, another dummy byte and link down status is written into the FIFO providing alignment of link down status with the data read from the FIFO. The controlling processor is responsible for checking the COLS Status Register bit for a change in the link status. If the COLS Status Register bit (0042H+80H*N) is set to logic 1, the FIFO must be emptied to determine the current link status. The first flag and abort status, encoded in the PBS bits, are used to set and clear a Link Active software flag.

When the last byte of a properly terminated packet is received, an interrupt is generated. When the Status Register (0042H+80H*N) is read, the PKIN bit will be logic 1, which can either be a signal to the external processor to empty the bytes remaining in the FIFO or an increment of a number-of-packets-received count. Wait for the FIFO to fill to a programmable level. Once the Status Register (0042H+80H*N) is read, the PKIN bit is cleared to logic 0. If the Status Register (0042H+80H*N) is read immediately after the last packet byte is read from the FIFO, the PBS[2] bit will be logic 1 and the CRC and non-integer byte status can be checked by reading the PBS[1:0] bits.

When the FIFO fill level is exceeded, an interrupt is generated. The FIFO must be emptied to remove this source of interrupt.

The RDLC can be used in polled, interrupt driven or DMA-controlled mode for the transfer of frame data. In the polled mode, the INTB output is not used, and the processor controlling the RDLC must periodically read the Status Register (0042H+80H*N) of the RDLC to determine when to read the Data Register. In the interrupt driven mode, the processor controlling the RDLC uses the INTB output to determine when to read the Data Register (0043H+80H*N).

In the case of interrupt driven data transfer from the RDLC to the processor, the INTB output of the RDLC is connected to the interrupt input of the processor. Once the processor has determined that the RDLC is the source of the interrupt, the interrupt service routine should process the data in the following order:

1. RDLC Status Register (0042H+80H*N) Read. If INTR=1 then proceed to step 2 otherwise find the interrupt source elsewhere.

2. If OVR = 1, discard last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

3. If COLS = 1, set the EMPTY FIFO software flag.

4. If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will be delayed until the FIFO fill level is exceeded.

5. Data Register Read (0043H+80H*N).

6. Status Register Read (0042H+80H*N).

7. If OVR = 1, discard last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

8. If COLS = 1, set the EMPTY FIFO software flag.

9. If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will be delayed until the FIFO fill level is exceeded.

10. Start the processing of FIFO data. Use the PBS[2:0] packet byte status bits to decide what is to be done with the FIFO data.

a) If PBS[2:0] = 001, discard data byte read in step 5 and set the LINK ACTIVE software flag.

b) If PBS[2:0] = 010, discard the data byte read in step 5 and clear the LINK ACTIVE software flag.

c) If PBS[2:0] = 1XX, store the last byte of the packet, decrement the PACKET COUNT, and check the PBS[1:0] bits for CRC or NVB errors before deciding whether or not to keep the packet.

d) If PBS[2:0] = 000, store the packet data.

11. If FE = 0 and INTR = 1 or FE = 0 and EMPTY FIFO = 1, go to step 5 else clear the EMPTY FIFO software flag and leave this interrupt service routine to wait for the next interrupt.

The Link State is typically a local software variable. The Link State is inactive if the RDLC is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones. The Link State is active if the RDLC is receiving flags or data.

If the RDLC data transfer is operating in the polled mode, processor operation is exactly as shown above for the interrupt driven mode, except that the entry to the service routine is from a timer, rather than an interrupt.

12 Performance Monitoring

The TEMUX/TEMAP/TECT3 provides counters for performance monitoring and automatic performance monitoring for T1 mode.

12.1 Performance Monitoring Counters

The TEMUX/TEMAP/TECT3's Performance Monitoring Counters (PMON) block accumulates: CRC error events, Frame Synchronization bit error events and Out Of Frame events. Optionally, Change of Frame Alignment (COFA) events, with saturating counters over consecutive intervals as defined by the period of the supplied transfer clock signal (typically 1 second), may be accumulated. When the transfer clock signal is applied, the PMON transfers the counter values into holding registers and resets the counters to begin accumulating events for the interval. The counters are reset in such a manner that error events occurring during the reset are not missed. If the holding registers are not read between successive transfer clocks, an OVERRUN register bit is asserted.

Generation of the transfer clock within the TEMUX/TEMAP/TECT3 is performed by writing to any counter register location or by writing to the Revision Global PMON Update register (0002H). The holding register addresses are contiguous to facilitate faster polling operations.

The tables show the TEMUX/TEMAP/TECT3's performance counters for each of the counter types.

Table 4 PMON Registers for T1 Mode

Counter Type	Register	Description
Framing Bit Error	0039H+80H*N	Number of framing bit error events that occurred during the last accumulation interval
Out of Frame (OOF) Errors	003AH+80H*N -003AH+80H*N	Number of OOF events that occurred during the last accumulation interval
Bit Errors	003CH+80H*N -003DH+80H*N	Number of bit error events that occurred during the previous accumulation interval

Table 5 PMON Registers for E1 mode

Counter Type	Register	Description
Framing Bit Error	0039H+80H*N	Number of framing bit error events that occurred during the last accumulation interval
Far End Block Errors	003AH+80H*N -003AH+80H*N	Number of far end block error events that occurred during the previous accumulation interval
CRC Errors	003CH+80H*N -003DH+80H*N	Number of CRC error events that occurred during the previous accumulation interval

12.2 Automatic Performance Monitoring

The TEMUX/TEMAP/TECT3 may automatically update performance reports on a per second basis if the AUTOUPDATE bit, in the T1 APRM Configuration/Control register (0070H+80H*N), is set to logic 1. Table 6 below shows the message structure and contents of the performance report. Table 7 and Table 8 display bit explanations.

Table 6 Performance Report Message Structure and Contents

Octet No.	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
1	FLAG							
2	SAPI						C/R	EA
3	TEI							EA
4	CONTROL							
5	G3	LV	G4	U1	U2	G5	SL	G6
6	FE	SE	LB	G1	R	G2	Nm	NI
7	G3	LV	G4	U1	U2	G5	SL	G6
8	FE	SE	LB	G1	R	G2	Nm	NI
9	G3	LV	G4	U1	U2	G5	SL	G6
10	FE	SE	LB	G1	R	G2	Nm	NI
11	G3	LV	G4	U1	U2	G5	SL	G6
12	FE	SE	LB	G1	R	G2	Nm	NI
13	FCS							
14	FCS							
15	FLAG							

Notes:

The order of transmission of the bits is LSB (Bit 1) to MSB (Bit 8).

Table 7 Performance Report Message Structure Notes

Octet No.	Octet Contents	Interpretation
1	01111110	Opening LAPD Flag
2	00111000 00111010	From CI: SAPI=14, C/R=0, EA=0 From carrier: SAPI=14,C/R=1,EA=0
3	00000001	TEI=0,EA=1
4	00000011	Unacknowledged Frame
5,6	Variable	Data for latest second (T')
7,8	Variable	Data for Previous Second(T'-1)
9,10	Variable	Data for earlier Second(T'-2)
11,12	Variable	Data for earlier Second(T'-3)
13,14	Variable	CRC16 Frame Check Sequence
15	01111110	Closing LAPD flag

Table 8 Performance Report Message Contents

Bit Value	Interpretation
G1=1	CRC ERROR EVENT =1
G2=1	1<CRC ERROR EVENT ≤5
G3=1	5<CRC ERROR EVENT ≤10
G4=1	10<CRC ERROR EVENT ≤100
G5=1	100<CRC ERROR EVENT ≤319
G6=1	CRC ERROR EVENT ≥ 320
SE=1	Severely Errored Framing Event ≥ 1(FE shall =0)
FE=1	Frame Synchronization Bit Error Event ≥1 (SE shall=0)
LV=1	Line code violation event ≥1
SL=1	Slip Event ≥ 1
LB=1	Payload Loopback Activated
U1,U2=0	Under Study For Synchronization
R=0	Reserved (Default Value =0)
NmNI=00,01,10,11	One second Report Modulo 4 Counter

12.3 Using the Internal DS3 FDL Transmitter

It is important to note that the access rate to the TDPR registers is limited by the rate of the internal high-speed system clock. Consecutive accesses to the TDPR Configuration (1020H), TDPR Interrupt Status/UDR Clear (1024H), and TDPR Transmit Data register (1025) should be accessed (with respect to WRB rising edge and RDB falling edge) at a rate no faster than 1/8 that of the selected TDPR high-speed system clock. This time is used by the high-speed system clock to sample the event, write the FIFO, and update the FIFO status. Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the line clock) must be considered when determining the procedure used to read and write the TDPR registers.

Upon reset of the TEMUX/TEMAP/TECT3, the TDPR should be disabled by setting the EN bit in the TDPR Configuration Register (1020H) to logic 0 (default value). An HDLC all-ones idle signal will be sent while in this state. Setting the EN bit to logic 1 enables the TDPR. The FIFOCLR bit should be set and then cleared to initialize the TDPR FIFO. The TDPR is now ready to transmit.

To initialize the TDPR, the TDPR Configuration Register (1020H) must be properly set. If FCS generation is desired, the CRC bit should be set to logic 1. If the block is to be used in interrupt driven mode, then interrupts should be enabled by setting the FULLE, OVRE, UDRE, and LFILLE bits in the TDPR Interrupt Enable register (1023H) to logic 1. The TDPR operating parameters in the TDPR Upper Transmit Threshold (1021H) and TDPR Lower Interrupt Threshold (1022H) registers should be set to the desired values. The TDPR Upper Transmit Threshold (1021H) sets the value at which the TDPR automatically begins the transmission of HDLC packets, even if no complete packets are in the FIFO. Transmission will continue until current packet is transmitted and the number of bytes in the TDPR FIFO falls to, or below, this threshold level. The TDPR will always transmit all complete HDLC packets (packets with EOM attached) in its FIFO. Finally, setting the EN bit to logic 1 can enable the TDPR. If no message is sent after the EN bit is set to logic 1, continuous flags will be sent.

The TDPR can be used in a polled or interrupt driven mode for the transfer of data. In the polled mode the processor controlling the TDPR must periodically read the TDPR Interrupt Status register (1024H) to determine when to write to the TDPR Transmit Data register (1025H). In the interrupt driven mode, the processor controlling the TDPR uses the INTB output, the TEMUX/TEMAP/TECT3 Interrupt Status register (1024H) to identify TDPR interrupts which determine when writes can or must be done to the TDPR Transmit Data register (1025H).

12.4 Interrupt Driven Mode

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold (1021H). The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold (1022H) should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 1 so an interrupt on INTB is generated upon detection of a FIFO full state, a FIFO depth below the lower limit threshold, a FIFO overrun, or a FIFO underrun. The following procedure should be followed to transmit HDLC packets:

1. Wait for data to be transmitted. Once data is available to be transmitted, then go to step 2.

2. Write the data byte to the TDPR Transmit Data register (1025H).

3. If all bytes in the packet have been sent, then set the EOM bit in the TDPR Configuration register (1020H) to logic 1. Go to step 1.

4. If there are more bytes in the packet to be sent, then go to step 2.

5. While performing steps 1 to 4, the processor should monitor for interrupts generated by the TDPR. When an interrupt is detected, the TDPR Interrupt Routine detailed in the following text should be followed immediately.

The TDPR will force transmission of the packet information when the FIFO depth exceeds the threshold programmed with the UTHR[6:0] bits in the TDPR Upper Transmit Threshold register (1021H). Unless an error condition occurs, transmission will not stop until the last byte of all complete packets is transmitted and the FIFO depth is at or below the threshold limit. The user should watch the FULLI and LFILLI interrupts to prevent overruns and underruns.

12.5 TDPR Interrupt Routine

Once the source of the interrupt has been identified as TDPR, then the following procedure should be carried out:

1. Read the TDPR Interrupt Status register (1024H).

2. If UDRI=1, then the FIFO has underrun and the last packet transmitted has been corrupted and needs to be retransmitted. When the UDRI bit transitions to logic 1, one Abort sequence and continuous flags will be transmitted. The TDPR FIFO is held in reset state. To re- enable the TDPR FIFO and to clear the underrun, the TDPR Interrupt Status/UDR Clear (1024H) register should be written with any value.

3. If OVRI=1, then the FIFO has overflowed. The packet, which the last byte written into the FIFO belongs to, has been corrupted and must be retransmitted. Other packets in the FIFO are not affected. Either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

   If the FIFO overflows on the packet currently being transmitted (packet is greater than 128 bytes long), OVRI is set, an Abort signal is scheduled to be transmitted, the FIFO is emptied, and then flags are continuously sent until there is data to be transmitted. The FIFO is held in reset until a write to the TDPR Transmit Data register (1025H) occurs. This write contains the first byte of the next packet to be transmitted.

4. If FULLI=1 and FULL=1, then the TDPR FIFO is full and no further bytes can be written. When in this state, either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

   If FULLI=1 and FULL=0, then the TDPR FIFO had reached the FULL state earlier, but has since emptied out some of its data bytes and now has space available in its FIFO for more data.

5. If LFILLI=1 and BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. If there is more data to transmit, then it should be written to the TDPR Transmit Data register (1025H) before an underrun occurs. If there is no more data to transmit, then an EOM should be set at the end of the last packet byte. Flags will then be transmitted once the last packet has been transmitted.

   If LFILLI=1 and BLFILL=0, then the TDPR FIFO had fallen below the lower-threshold state earlier, but has since been refilled to a level above the lower-threshold level.

12.6 Polling Mode

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold (1021H). The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold (1022H) should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 0 since packet transmission is set to work with a periodic polling procedure. The following procedure should be followed to transmit HDLC packets:

1. Wait until data is available to be transmitted, then go to step 2.

2. Read the TDPR Interrupt Status register (1024H).

3. If FULL=1, then the TDPR FIFO is full and no further bytes can be written. Continue polling the TDPR Interrupt Status register until either FULL=0 or BLFILL=1. Then, go to either step 4 or 5 depending on implementation preference.

4. If BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. Write the data into the TDPR Transmit Data register (1025H). Go to step 6.

5. If FULL=0, then the TDPR FIFO has room for at least 1 more byte to be written. Write the data into the TDPR Transmit Data register (1025H). Go to step 6.

6. If more data bytes are to be transmitted in the packet, then go to step 2.

7. If all bytes in the packet have been sent, then set the EOM bit in the TDPR Configuration register (1020H) to logic 1. Go to step 1.

12.7 Using the Internal Data Link Receiver

It is important to note that the access rate to the RDLC registers is limited by the rate of the internal high-speed system clock Consecutive accesses to the RDLC Status and RDLC Data registers should be accessed at a rate no faster than 1/10 that of the selected RDLC high-speed system clock. This time is used by the high-speed system clock to sample the event and update the FIFO status. Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the receive line clock) must be considered when determining the procedure used to read RDLC registers.

On power up of the system, the RDLC should be disabled by setting the EN bit in the Configuration Register (1028H) to logic 0 (default state). The RDLC Interrupt Control register (1029H) should then be initialized to enable the INT output and to select the FIFO buffer fill level at which an interrupt will be generated. If the INTE bit is not set to logic 1, the RDLC Status register (102AH) must be continuously polled to check the interrupt status (INTR) bit.

After the RDLC Interrupt Control register (1029H) has been written, the RDLC can be enabled at any time by setting the EN bit in the RDLC Configuration (1028H) register to logic 1. When the RDLC is enabled, it will assume the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated, and a dummy byte will be written into the FIFO buffer. This is done to provide alignment of link up status with the data read from the FIFO. When an abort character is received, another dummy byte and link down status is written into the FIFO. This is done to provide alignment of link down status with the data read from the FIFO. It is up to the controlling processor to check the COLS bit in the RDLC Status register (102AH) for a change in the link status. If the COLS bit is set to logic 1, the FIFO must be emptied to determine the current link status. The first flag and abort status encoded in the PBS bits is used to set and clear a Link Active software flag.

When the last byte of a properly terminated packet is received, an interrupt is generated. While the RDLC Status register (102AH) is being read the PKIN bit will be logic 1. This can be a signal to the external processor to empty the bytes remaining in the FIFO or to just increment a number-of-packets-received count and wait for the FIFO to fill to a programmable level. Once the RDLC Status register (102AH) is read, the PKIN bit is cleared to logic 0. If the RDLC Status register (102AH) is read immediately after the last packet byte is read from the FIFO, the PBS[2] bit will be logic 1 and the CRC and non-integer byte status can be checked by reading the PBS[1:0] bits.

When the FIFO fill level is exceeded, an interrupt is generated. The FIFO must be emptied to remove this source of interrupt.

The RDLC can be used in a polled or interrupt driven mode for the transfer of frame data. In the polled mode, the processor controlling the RDLC must periodically read the RDLC Status register (102AH) to determine when to read the RDLC Data register. In the interrupt driven mode, the TEMUX/TEMAP/TECT3 Interrupt Status registers should be read to determine when to read the RDLC Data register (102BH).

Once an interrupt has identified that the RDLC has generated the interrupt, it processes the data in the following order:

1. RDLC Status register (102AH) read. The INTR bit should be logic 1.

2. If OVR = 1, then discard last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

3. If COLS = 1, then set the EMPTY FIFO software flag.

4. If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will be delayed until the FIFO fill level is exceeded.

5. Read the RDLC Data register (102BH).

6. Read the RDLC Status register (102AH).

7. If OVR = 1, then discard last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

8. If COLS = 1, then set the EMPTY FIFO software flag.

9. If PKIN = 1, increment the PACKET COUNT. If the FIFO is to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will be delayed until the FIFO fill level is exceeded.

10. Start the processing of FIFO data. Use the PBS[2:0] packet byte status bits to decide what is to be done with the FIFO data.

    a) If PBS[2:0] = 001, discard data byte read in step 5 and set the LINK ACTIVE software flag.

    b) If PBS[2:0] = 010, discard the data byte read in step 5 and clear the LINK ACTIVE software flag.

    c) If PBS[2:0] = 1XX, store the last byte of the packet, decrement the PACKET COUNT, and check the PBS[1:0] bits for CRC or NVB errors before deciding whether or not to keep the packet.

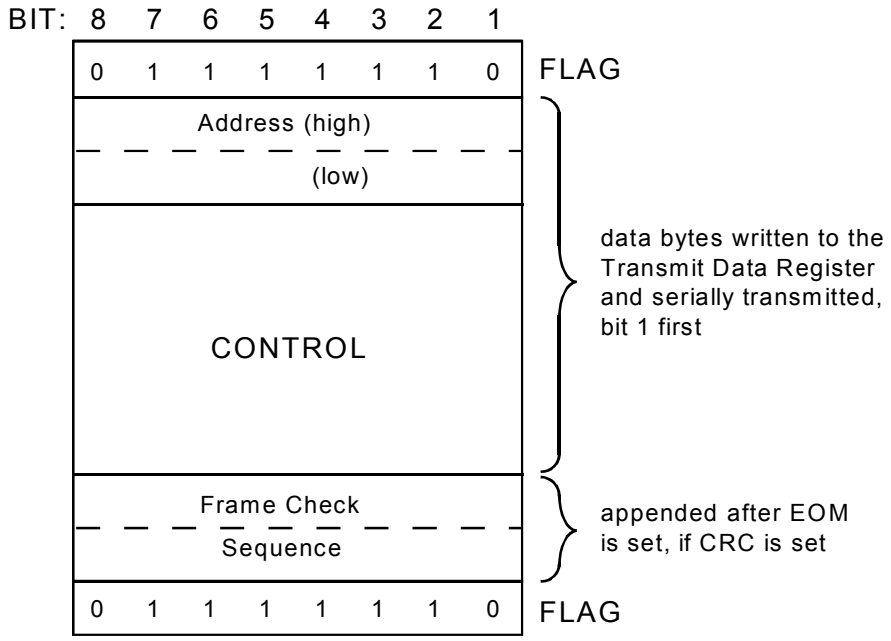
    d) If PBS[2:0] = 000, store the packet data.

11. If FE = 0 and INTR = 1 or FE = 0 and EMPTY FIFO = 1, go to step 5 else clear the EMPTY FIFO software flag and leave this interrupt service routine to wait for the next interrupt.

The link state is typically a local software variable. The link state is inactive if the RDLC is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RDLC is receiving flags or data.

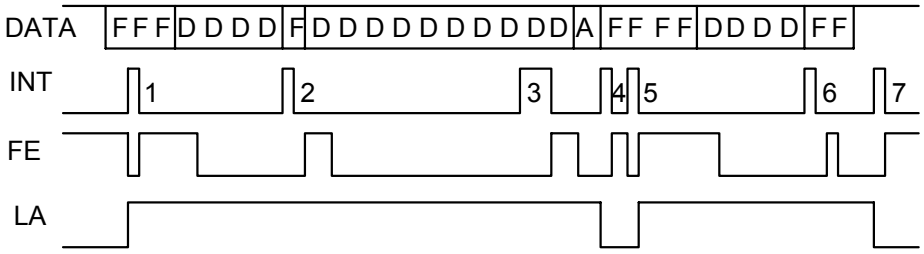
If the RDLC data transfer is operating in the polled mode, processor operation is exactly as shown above for the interrupt driven mode, except that the entry to the service routine is from a timer, rather than an interrupt.

Figure 33 Typical Data Frame



Bit 1 is the first serial bit to be received. When enabled, the primary, secondary and universal addresses are compared with the high order packet address to determine a match.

Figure 34 Example Multi-Packet Operational Sequence



F	- flag sequence (01111110)
A	- abort sequence (01111111)
D	- packet data bytes
INT	- active high interrupt output
FE	- internal FIFO empty status
LA	- state of the LINK ACTIVE software flag

Figure 34 shows the timing of interrupts, the state of the FIFO, and the state of the Data Link relative the input data sequence. The cause of each interrupt and the processing required at each point is described in the following paragraphs.

At points 1 and 5 the first flag after all ones or abort is detected. A dummy byte is written in the FIFO, FE goes low, and an interrupt goes high. When the interrupt is detected by the processor it reads the dummy byte, the FIFO becomes empty, and the interrupt is removed. The LINK ACTIVE (LA) software flag is set to logic 1.

At points 2 and 6 the last byte of a packet is detected and interrupt goes high. When the interrupt is detected by the processor, it reads the data and status registers until the FIFO becomes empty. The interrupt is removed as soon as the RDLC Status register is read since the FIFO fill level of 8 bytes has not been exceeded. It is possible to store many packets in the FIFO and empty the FIFO when the FIFO fill level is exceeded. In either case the processor should use this interrupt to count the number of packets written into the FIFO. The packet count or a software time-out can be used as a signal to empty the FIFO.

At point 3 the FIFO fill level of 8 bytes is exceeded and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed.

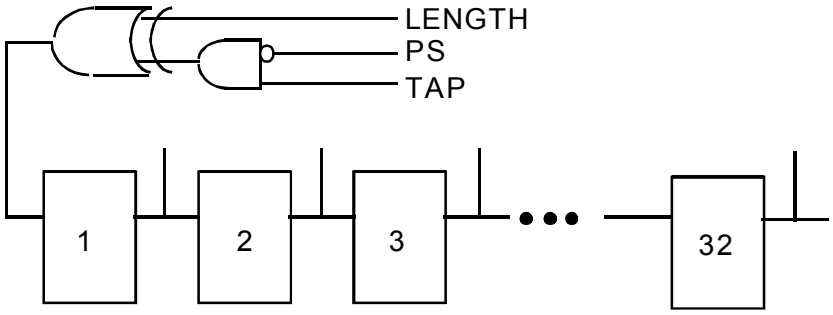
At points 4 or 7 an abort character is detected, a dummy byte is written into the FIFO, and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed. The LINK ACTIVE software flag is cleared.

13 DS3 PRGD Pattern Generation

A pseudo-random or repetitive pattern can be inserted/extracted in the DS3 payload

The pattern generator can be configured to generate pseudo random patterns or repetitive patterns as shown in Figure 35 below:

Figure 35 PRGD Pattern Generator



The pattern generator consists of a 32 bit shift register and a single XOR gate. The XOR gate output is fed into the first stage of the shift register. The XOR gate inputs are determined by values written to the length register (PL[4:0]) and the tap register (PT[4:0], when the PS bit is low). When PS is high, the pattern detector functions as a recirculating shift register, with length determined by PL[4:0].

13.1.1 Generating and Detecting Repetitive Patterns

When a repetitive pattern (such as 1-in-8) is to be generated or detected, the PS bit must be set to logic 1 in the PRGD Control register (1030H). The pattern length register must be set to (N-1) in the PRGD length register (1032H), where N is the length of the desired repetitive pattern. Several examples of programming for common repetitive sequences are given below in the Common Test Patterns section.

For pattern generation, the desired pattern must be written into the PRGD Pattern Insertion registers (1038H-103BH). The repetitive pattern will then be continuously generated. The generated pattern will be inserted in the output data stream, but the phase of the pattern cannot be guaranteed.

For pattern detection, the PRGD will determine if a repetitive pattern of the length specified in the pattern length register (1032H) exists in the input stream. It does so by loading the first N bits from the data stream, and then monitoring to see if the pattern loaded repeats itself error free for the subsequent 48 bit periods. It will repeat this process until it finds a repetitive pattern of length N, at which point it begins counting errors (and possibly re-synchronizing) in the same way as for pseudo-random sequences. Note that the PRGD does NOT look for the pattern loaded into the Pattern Insertion registers (1038H-103BH), but rather automatically detects any repetitive pattern of the specified length. The precise pattern detected can be determined by initiating a PRGD update, setting PDR[1:0] = 00 in the PRGD Control register (1030H), and reading the Pattern Detector registers (103CH-103FH) (which will then contain the 32 bits detected immediately prior to the strobe).

13.1.2 Common Test Patterns

The PRGD can be configured to monitor the standardized pseudo random and repetitive patterns described in ITU-T O.151. The register configurations required to generate these patterns and others are indicated in the two tables below:

Table 9 Pseudo Random Pattern Generation (PS bit = 0)

Pattern Type	TR	LR	IR#1	IR#2	IR#3	IR#4	TINV	RINV
$2^3 - 1$	00	02	FF	FF	FF	FF	0	0
$2^4 - 1$	00	03	FF	FF	FF	FF	0	0
2^5-1	01	04	FF	FF	FF	FF	0	0
$2^6 - 1$	04	05	FF	FF	FF	FF	0	0
$2^7 - 1$	00	06	FF	FF	FF	FF	0	0
2^7 -1 (Fractional T1 LB Activate)	03	06	FF	FF	FF	FF	0	0
2^7 -1 (Fractional T1 LB Deactivate)	03	06	FF	FF	FF	FF	1	1
2^9 -1 (O.153)	04	08	FF	FF	FF	FF	0	0
$2^{10} - 1$	02	09	FF	FF	FF	FF	0	0
2^{11} -1 (O.152, O.153)	08	0A	FF	FF	FF	FF	0	0
2^{15} -1 (O.151)	0D	0E	FF	FF	FF	FF	1	1
$2^{17} - 1$	02	10	FF	FF	FF	FF	0	0
$2^{18} - 1$	06	11	FF	FF	FF	FF	0	0
2^{20} -1 (O.153)	02	13	FF	FF	FF	FF	0	0
2^{20} -1 (O.151 QRSS bit=1)	10	13	FF	FF	FF	FF	0	0
$2^{21} - 1$	01	14	FF	FF	FF	FF	0	0
$2^{22} - 1$	00	15	FF	FF	FF	FF	0	0
2^{23} -1 (O.151)	11	16	FF	FF	FF	FF	1	1
$2^{25} - 1$	02	18	FF	FF	FF	FF	0	0
$2^{28} - 1$	02	1B	FF	FF	FF	FF	0	0
$2^{29} - 1$	01	1C	FF	FF	FF	FF	0	0
$2^{31} - 1$	02	1E	FF	FF	FF	FF	0	0

Table 10 Repetitive Pattern Generation (PS bit = 1)

Pattern Type	TR	LR	IR#1	IR#2	IR#3	IR#4	TINV	RINV
All ones	00	00	FF	FF	FF	FF	0	0
All zeros	00	00	FE	FF	FF	FF	0	0

Alternating ones/zeros	00	01	FE	FF	FF	FF	0	0
Double alternating ones/zeros	00	03	FC	FF	FF	FF	0	0
3 in 24	00	17	22	00	20	FF	0	0
1 in 16	00	0F	01	00	FF	FF	0	0
1 in 8	00	07	01	FF	FF	FF	0	0
1 in 4	00	03	F1	FF	FF	FF	0	0
Inband loopback activate	00	04	F0	FF	FF	FF	0	0
Inband loopback deactivate	00	02	FC	FF	FF	FF	0	0

Notes for the Pseudo Random and Repetitive Pattern Generation Tables

1. The PS bit and the QRSS bit are contained in the PRGD Control register (1030H)
2. TR = PRGD Tap Register (1033H)
3. LR = PRGD Length Register (1032H)
4. IR#1 = PRGD Pattern Insertion #1 Register (1038H)
5. IR#2 = PRGD Pattern Insertion #2 Register (1039H)
6. IR#3 = PRGD Pattern Insertion #3 Register (103AH)
7. IR#4 = PRGD Pattern Insertion #4 Register (103BH). This register must be written last when setting a new pattern.
8. The TINV bit and the RINV bit are contained in the PRGD Control register (1030H).

14 Scaleable Bandwidth Interconnect Set-Up

14.1 SBI Master Configuration

The SBI on the TEMUX/TEMAP/TECT3 can map and demap the following:

- Unframed or Channelized T1 1.544Mb/s links for DS3 Multiplex or SONET/SDH Mapping.
- Unframed or Channelized E1 2.048 Mb/s links for SONET/SDH Mapping.
- A single Channelized or Unchannelized 44.736Mb/s link.

Note: The DS3 signal can also be unframed for mapping into a SONET/SDH. The Unchannelized DS3 is applicable when in DS3 framer only mode. The DS3 can only be channelized with T1s. DS3 G.747 mode over the SBI bus is not supported.

a) Register 1700H: SBI Master Reset/Bus Signal Monitor

RESET	'0' SBI functions as normal '1' SBI Block held in RESET

b) Register 0001H: Global Configuration

SYSOPT[2:0]	'010' SBI Interface '011' SBI Interface with CAS or CCS H-MVIP Interface. [1] (Only valid in High Density Framer Mode).
Notes: 1. This mode is not supported for the TEMAP.	

c) Register 1701H: SBI Master Configuration

SDROPSEL[1:0]	Select which SPE on the DROP side the TEMUX/TEMAP/TECT3 will provide data '00' Disabled '01' SPE #1 '10' SPE #2 '11' SPE #3
SADDSEL[1:0]	Select which SPE on the ADD side the TEMUX/TEMAP/TECT3 will act on '00' Disabled '01' SPE #1 '10' SPE #2 '11' SPE #3
MFSC1FP	'0' Will generate 2KHz pulses '1' Will generate multiframes (Required when sending CAS over the SBI bus)
SC1FPMSTR	'0' SC1FP expected on this TEMUX/TEMAP/TECT3 '1' SC1FP is generated by this TEMUX/TEMAP/TECT3 Only one TEMUX/TEMAP/TECT3 device can be a MASTER and other devices will listen for SC1FP signal.
FASTCLKFREQ	'0' CLK52M is 44.928MHz '1' CLK52M is 51.84MHz Must match setting for FASTCLKFREQ in SONET/SDH Master DS3 Clock Generation Control Register.

d) Register 1702H: SBI Bus Master Configuration

BUSMASTER	'0' TEMUX/TEMAP/TECT3 only drives the SBI Bus during links enabled for this device. '1' TEMUX/TEMAP/TECT3 will drive the SBI Drop Bus during all links and SBI overhead bytes except when it detect other device are driving the bus when the SBIDET[1:0] signals are set to '1'. In the drop direction, one TEMUX/TEMAP/TECT3 should be selected as bus master so that it drives the bus during all SBI locations that are not driven by the other TEMUX/TEMAP/TECT3s. This is done with the SBI busmaster register bit. For multiple device driving the add bus to TEMUX/TEMAP/TECT3, there should be one device nominated as bus master. The device(s) driving the add bus to the TEMUX/TEMAP/TECT3 must drive all the SBI columns or parity errors will be detected.

Note:

1. When in E1 mode over SBI the IMFPCFG[1:0] bits must be set to ‘01’ or ‘10’ for correct operation. For CAS in E1 the bits should be ‘10’. These bits are found in Register 005H+80H*N: T1/E1 Ingress Serial Interface Mode Select.

2. In T1 SF mode the ALTIFP bit must be set to 1 before the SBI block is initialized for correct operation.

14.2 SBI ADD Bus Set-up

a) Register 1710H: EXSBI Control

SBI_PAR_CTL	‘1’ Sets Odd Parity

14.2.1 Configuring the Indirect RAM for the SBI Add Bus

The SBI ADD bus must be correctly configured by accessing the indirect RAM through a register sequence to configure the bus for T1, E1 or DS3 applications. The sequence for the Read and Write process is a follows: (details of individual registers are included below)

Reading the Indirect SBI Add Bus RAM

1. Select the TRIB[4:0] and the SPE[1:0] in EXSBI Tributary RAM Indirect Access Register 1713H.

2. Set the RWB bit to ‘1’ in EXSBI: Tributary RAM Indirect Access Control Register 1714H to indicate a Read request.

3. Poll the BUSY bit until it is set to ‘0’ in EXSBI: Tributary RAM Indirect Access Control Register 1714H.

4. Read the set up for that Tributary by reading EXSBI:Tributary Control Indirect Access Data Register 1716H.

5. Repeat from stage 1) for further reads.

Writing to the Indirect SBI Add Bus RAM

1. Set up the Tributary Information by writing to the EXSBI:Tributary Control Indirect Access Data Register 1716H.

2. Set the TRIB[4:0] and the SPE[1:0] in EXSBI Tributary RAM Indirect Access Register 1713H.

3. Set the RWB bit to ‘0’ in EXSBI: Tributary RAM Indirect Access Control Register 1714H.

4. Poll the BUSY bit until it is set to ‘0’ in EXSBI: Tributary RAM Indirect Access Control Register 1714H. This indicates a write transfer has completed.

5. Repeat from stage 1) for further writes.

14.2.2 Indirect Tributary RAM Registers

a) Register 1713H: EXSBI Tributary RAM Indirect Access Address

SPE[1:0]	'01' SPE 1 is selected '10' SPE 2 is selected '11' SPE 3 is selected
TRIB[4:0]	Binary '00001 to 11100' are valid Selects the Tributary For T1 = 1 to 28 (Binary 00001 to 11100) For E1 = 1 to 21 (Binary 00001 to 10101) For DS3 =1 (Binary 00001)

b) Register 1716H: EXSBI Tributary Control Indirect Access Data

ENBL	'0' Disables the Tributary '1' Actives the Tributary
TRIB_TYP[1:0]	'00' Framed with CAS (T1 or E1) '01' Framed without CAS (T1, E1 or DS3) '10' Unframed (T1, E1 or DS3)
CLK_MSTR	'0' TEMUX/TEMAP/TECT3 is clock slave for the selected Tributary. (For example when interfacing to an AAL1gator device over SBI). '1' TEMUX/TEMAP/TECT3 is clock master for the selected Tributary. (For example when interfacing to FREEDM over SBI).
CLK_MODE	'00' Link Rate Octet not used '01' Use only ClkRate field of Link Rate octet '10' Use only Phase Field of Link Rate octet

When TEMUX/TEMAP/TECT3 serves as the SBI clock master for a given tributary (CLK_MSTR ='1'), the TEMUX/TEMAP/TECT3's EXSBI must be enabled (set ENBL = 1) before the far-end SBI device's INSBI block is enabled.

For example, to set up the SBI ADD bus between the TEMUX/TEMAP/TECT3 and FREEDM-84P672:
First, set the ENBL bit of Register 1716H to '1'.
Then, set the ENBL bit of FREEDM Register 689H to '1'.

When the TEMUX/TEMAP/TECT3 is clock slave (CLK_MSTR = '0'), set up the far-end device's INSBI first, and then set up the TEMUX/TEMAP/TECT3 EXSBI.

14.3 SBI Drop Bus Set-up

a) Register 1720H: INSBI Control

SBI_PAR_CTL	'1' Sets Odd Parity

14.3.1 Configuring the Indirect RAM for the SBI Drop Bus

The SBI DROP bus must be correctly configured by accessing the indirect RAM through a register sequence to configure the bus for T1, E1 or DS3 applications. The sequence for the Read and Write process is shown below, with details of individual registers:

Reading the Indirect SBI Drop Bus RAM

1. Select the TRIB[4:0] and the SPE[1:0] in INSBI Tributary RAM Indirect Access Register 1723H.
2. Set the RWB bit to '1' in INSBI: Tributary RAM Indirect Access Control Register 1724H to indicate a Read request.
3. Poll the BUSY bit until it is set to '0' in INSBI: Tributary RAM Indirect Access Control Register 1724H.
4. Read the set up for that tributary by reading INSBI: Tributary Control Indirect Access Data Register 1726H.
5. Repeat from stage 1 for further reads

Writing to the Indirect SBI Add Bus RAM

1. Set up the Tributary Information by writing to the INSBI: Tributary Control Indirect Access Data Register 1726H.
2. Set the TRIB[4:0] and the SPE[1:0] in INSBI Tributary RAM Indirect Access Register 1723H.
3. Set the RWB bit to '0' in INSBI: Tributary RAM Indirect Access Control Register 1724H.
4. Poll the BUSY bit until it is set to '0' in INSBI: Tributary RAM Indirect Access Control Register 1724H. This indicates a write transfer has completed.
5. Repeat from stage 1 for further writes.

14.3.2 Indirect Tributary RAM Registers

a) Register 1723H: INSBI Tributary RAM Indirect Access Address

SPE[1:0]	'01' SPE 1 is selected '10' SPE 2 is selected '11' SPE 3 is selected
TRIB[4:0]	Binary '00001 to 11100' are valid Selects the Tributary For T1 = 1 to 28 (Binary 00001 to 11100) For E1 = 1 to 21 (Binary 00001 to 10101) For DS3 =1 (Binary 00001)

b) Register 1726H: INSBI Tributary Control Indirect Access Data

ENBL	'0' Disables the Tributary '1' Actives the Tributary
TRIB_TYP[1:0]	'00' Framed with CAS (T1 or E1) '01' Framed without CAS (T1, E1 or DS3) '10' Unframed (T1, E1 or DS3)
ITVT	'0' Normal operation '1' Selects a Transparent VT for Mapper Mode only
SYNCH_TRIB	Applies to T1/E1 mode '0' Normal operation '1' Forces T1 or E1 timeslots are locked in a fixed location within the SBI structure. The T1/E1 framer must be operating synchronously to the SBI Bus. Tributary must pass through the T1/E1 Elastic store and thus the SYNCSBI bit must be set to '1' in the T1/E1 Receive Options Register (002H+80H*N). The tributary should be reset when this bit is changed, disable the tributary and then re-enable it.

When TEMUX/TEMAP/TECT3 serves as the SBI clock master for a given tributary (SYNCH_TRIB = '0'), the TEMUX/TEMAP/TECT3's INSBI must be enabled (set ENBL = 1) before the far-end device's EXSBI block is enabled.

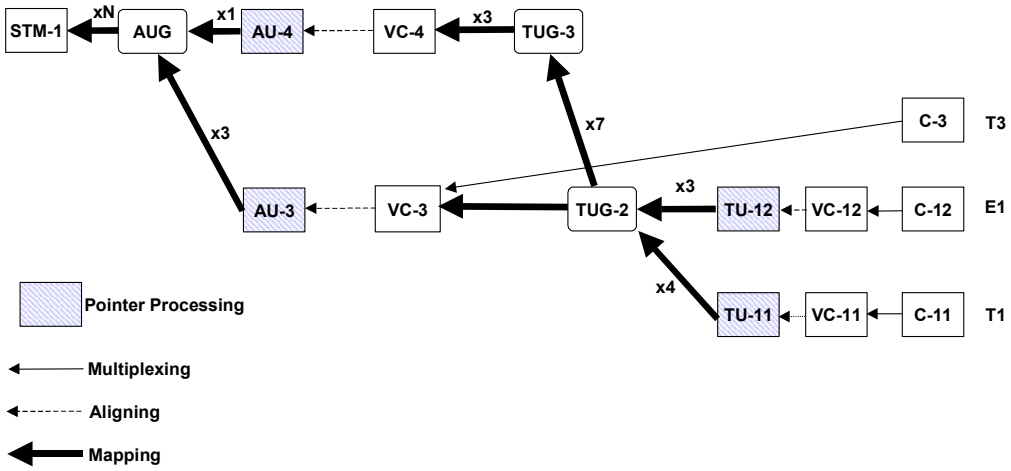
For example, to set up the SBI ADD bus between the TEMUX/TEMAP/TECT3 and FREEDM-84P672:
First, set the ENBL bit of Register 1726H to '1'.
Then, set the ENBL bit of FREEDM Register 5D8H to '1'.

15 TelecomBus Mapping (Not Supported for TECT3)

15.1 Telecom Bus Multiplex Overview

The TEMUX/TEMAP is able to map and demap VT1.5 payload (C-11), VT2 payload (C-12) and DS3 payload (C-3). The TEMUX/TEMAP will map T1 and E1 streams into VT payloads (containers) in any of the combinations shown below. In the mapping function a jitter attenuator is included.

Figure 36 Multiplexing Overview



15.2 SONET/SDH Equivalents

The TEMUX/TEMAP will operate under SDH and SONET conventions. The naming convention is as follows:

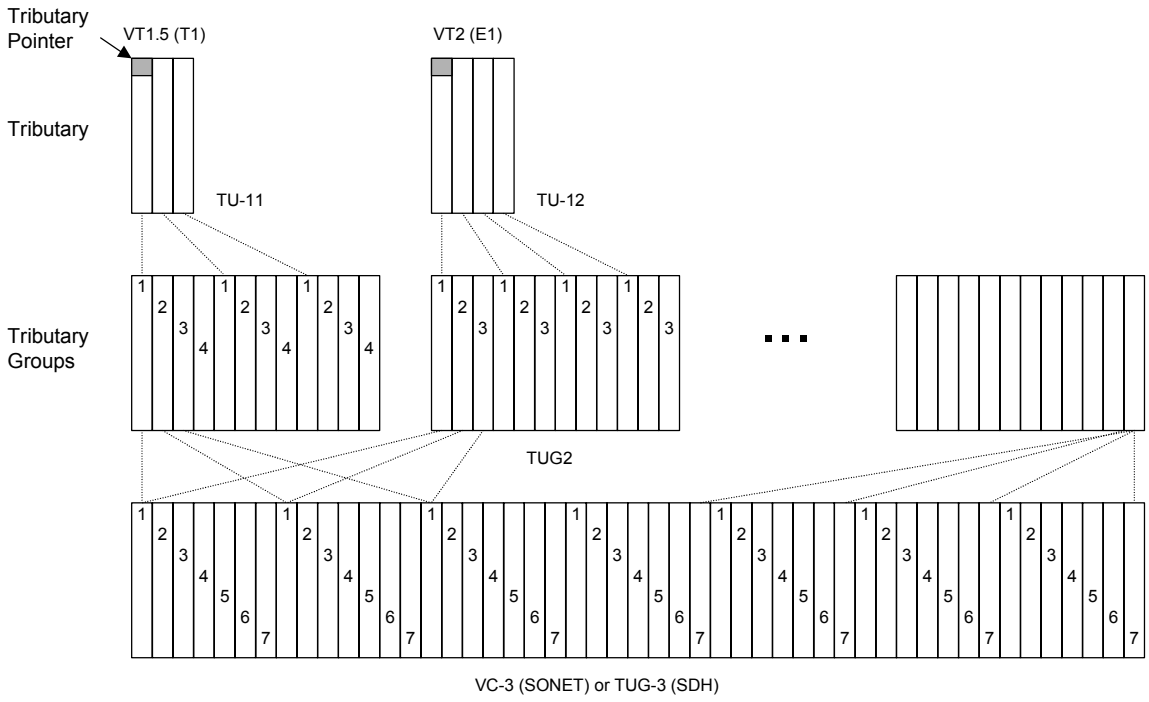
Table 11 SONET/ SDH Naming Conventions

SONET Entity	SDH Entity
VT1.5 Payload	C-11
VT2 Payload	C-12
VT1.5 SPE	VC-11
VT2 SPE	VC-12
VT1.5	TU-11
VT2	TU-12
VT Group	TUG-2
STS-1 Payload	TUG-3
STS-1 SPE	VC-3
STS-3c SPE	VC-4
(no equivalent)	AU-3
(no equivalent)	AU-4
(no equivalent)	AUG
STS-1	(no equivalent)
STS-3	STM-1
DS3 Payload	C-3

15.3 Tributary Structures

The mapping of VT1.5 (T1) payload and VT2 (E1) payload is as follows:

Figure 37 Tributary Mapping Default



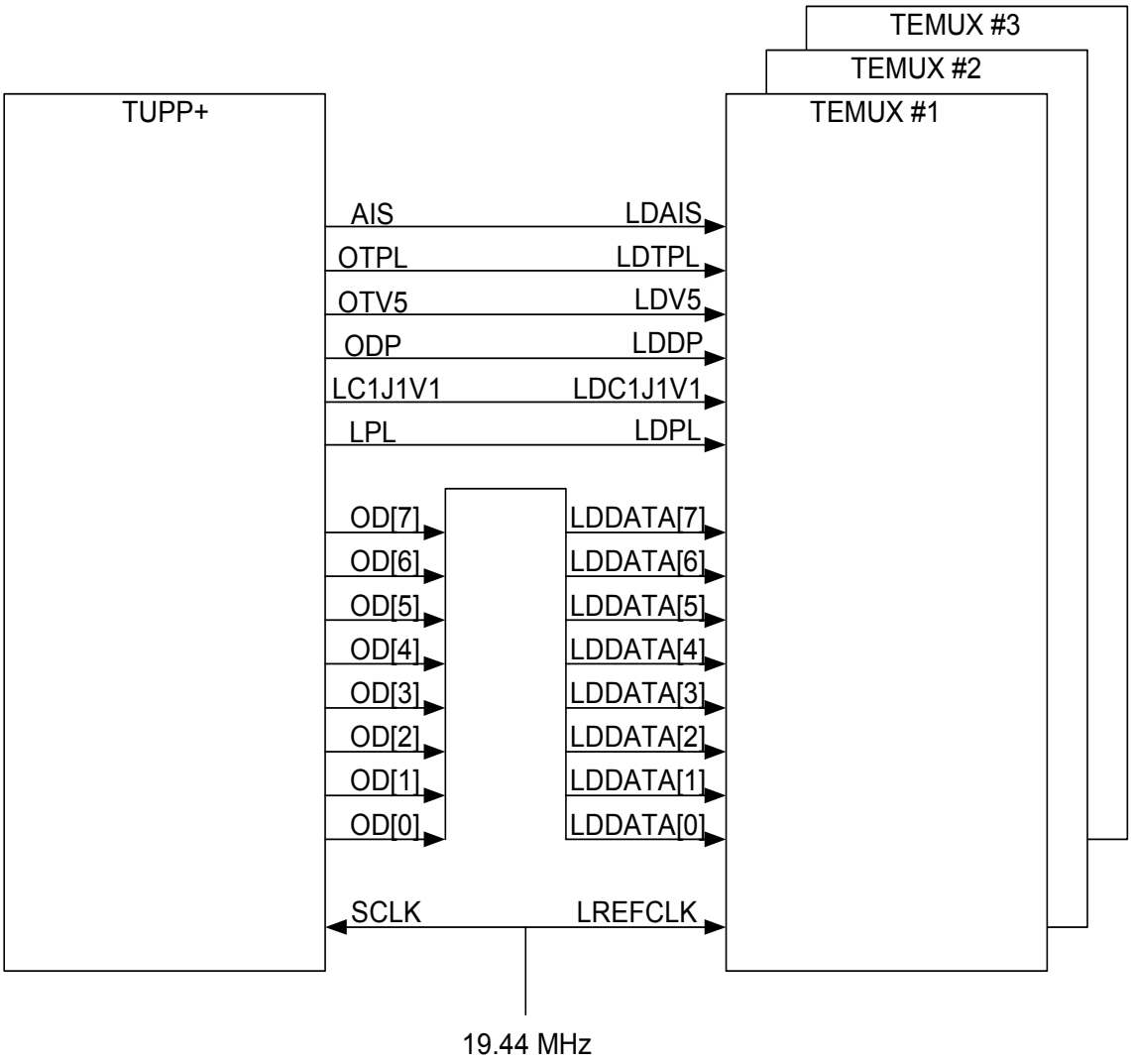
In an OC-3/STM-1 application each TEMUX/TEMAP can be configured to process one of the 3 STS1s/STM-0s. Here are some examples for configuring the 3 TEMUX/TEMAPs. If the tributary data per SPE is to be switched between TEMUX/TEMAPs then the tributary pointer processing needs to be done externally first to align all 3 SPEs together before tributaries can be switched between SPEs. A PM5362 TUPP+ device would perform this task. Please refer to figure 36 below. Note that the IVTPP must be bypassed in each TEMUX in this mode and the RTDM Time Switch RAM must be configured.

a) TEMUX/TEMAP #1 set up for 28 T1s, TEMUX/TEMAP #2 set up for 21 E1s and TEMUX/TEMAP #3 set up for DS3 SPE#1 for TEMUX/TEMAP #1, SPE#2 for TEMUX/TEMAP #2 and SPE#3 for TEMUX/TEMAP #3 are all independent and data cannot switch between them.

b) TEMUX/TEMAP #1 set up for 28 T1s, TEMUX/TEMAP #2 set up for 28 T1s and TEMUX/TEMAP #3 set up for 21 E1s. A T1 payload from TEMUX/TEMAP #1 can be switched in to the SPE#2 which is dedicated to TEMUX/TEMAP #2 and vice versa. However a T1 payload cannot be extracted from SPE#3 which belongs to TEMUX/TEMAP #3 because this is configured for E1 mapping operation. Follow the RTDM Time Switch RAM initialization procedure in section 16.4.1 to setup this type of function.

c) TEMUX/TEMAP #1 set up for 28 T1s, TEMUX/TEMAP #2 set up for 28 T1s and TEMUX/TEMAP #3 set up for 28 T1s. A T1 payload from TEMUX/TEMAP #1 can be switched in to the SPE#2 which is dedicated to TEMUX/TEMAP #2 and or SPE#3 which is dedicated to TEMUX/TEMAP #3 and vice versa. Follow the RTDM Time Switch RAM initialization procedure in section 16.4.1 to setup this type of function.

Figure 38 External Tributary Pointer Processing with PM5362 TUPP+



16 TU-11 (VT1.5) or TU-12 (VT2) Set Up (Not Supported for TECT3)

16.1 Programming Initialization Sequence

16.1.1 Initialization Sequencing in VT/TU Mapping Mode

When using TEMUX/TEMAP in VT/TU mapping mode with any system side option, care should be taken in the initialization of the device to make sure it comes up in the proper state. Please use the recommended initialization sequences below.

VT/TU mapping mode is not supported for the TECT3. This entire section does not apply to the TECT3.

Initialization of Framer Timing Options

In TEMUX/TEMAP Register 004H+80H*N: T1/E1 Egress Line Interface Configuration, select the transmit timing source by setting PLLREF[1:0] correctly. The T1/E1 transmit timing can be sourced from the two clock master sources, the CTCLK input or the recovered T1/E1 clock, or from the four clock slave sources, an ECLK[x] input, the CECLK input, the SBI tributary rate received on the SBI add bus and the H-MVIP clock. Do not bypass the TJAT. This will ensure that when the transmit timing source is optionally referenced to the recovered timing for the tributary the transition will be smooth. TJAT is also used in the TTMP centering procedure outlined in section 3 below. Note that in the case where the ECLK[x] input, CECLK input, the SBI add bus or the H-MVIP clock is the source of the transmit timing, looptiming via the PLLREF[1:0] bits is invalid.

Initialization of RTDM

Program Register 12E0H: RTDM Pointer Justification Rate Control for a T1 rate control of 0.4 seconds (T1RATE[1:0]=10) in T1 mode or an E1 rate control of 0.4 seconds (E1RATE[1:0]=10) in E1 mode.

Initialization of RJAT and TJAT for all TU11/TU12 T1/E1 Framing Configurations

In the initial setting of the RJAT (registers 0011+80*N, 0012+80*N and 0013+80*N) perform both PLL reset and FIFO centering with the following sequence. In the RJAT configuration register, set the CENT and LIMIT bits to 0 and the reserved and SYNC bits to 1. Program the RJAT N1 and N2 divisors to 2F and then go back to write a logic 0 to the CENT, LIMIT and SYNC bits and a logic 1 to the reserved bit. This is done for both T1 and E1. The time between writing the N1 and N2 values and clearing the SYNC bit needs to be as short as possible.

Note the following applies only to configurations in which the transmit timing source is equal to line rate (T1 or E1). This is applicable for all transmit timing modes except when the CTCLK input is a multiple of 8 kHz. For that configuration use the TTMP Re-provision Procedure workaround that follows the RJAT initialization Procedure and TJAT Centering Procedure below.

The TJAT for a specific tributary should be initialized after the transmit tributary mapper's (TTMP) tributary is provisioned and the transmit timing source has been selected. Then for the initial setting of the TJAT (registers 0015+80*N, 0016+80*N and 0017+80*N) perform both PLL reset and FIFO centering with the following sequence. Program the TJAT N1 and N2 divisors to 2F and then write a logic 0 to the CENT, LIMIT and SYNC bits and a logic 1 to the reserved bit. Next the N2 divisor should be programmed to the value **"A"** specified in Table 12 depending upon the mode selected (T1 or E1) frequency referenced to TJAT initially. Delay 100ms, then change the N1 value to **"B"** specified in Table 12. Delay another 100ms then change the N1 value to **"C"** specified in Table 12. Then in the TJAT configuration register, set the CENT and LIMIT bits to 0 and the reserved and SYNC bits to 1. Rewrite the value **"C"** into the N1 register and then clear the SYNC bit back to 0. Accurate delays need to be implemented in this procedure. The speed is important in order to create long frequency steps that are required to stabilize the TTMP. In addition, keep the relative time between re-writing the **"C"** value to N2 clearing SYNC bit as short as possible.

It is recommended to have the TTMP FIFO check from Section 16.1.2, "TTMP FIFO Check Procedure" in place following the TJAT centering procedure or the TTMP re-provision procedure to make sure the centering was successful. If this check is to be performed immediately after the above procedure then an additional 100ms of delay is required before the check. If the check of the TTMP FIFO is performed after all the tributaries have had the above procedure performed the additional delay is not required because considerable time will have passed since the centering procedure was performed on the first tributary.

RJAT initialization Procedure

a) Register 0013H + 80H*N RJAT Configuration

CENT	Set to '0'
LIMIT	Set to '0'
SYNC	Set to '1'
Reserved Bits	Set to '1'

b) Register 011H+80H*N RJAT Output Clock Divider N1 Control

N1[7:0]	Set to 2FH

c) Register 012H+80H*N RJAT Output Clock Divider N2 Control

N2[7:0]	Set to 2FH

d) Register 0013H + 80H*N RJAT Configuration

CENT	Set to '0'
LIMIT	Set to '0'
SYNC	Set to '0'
Reserved Bits	Set to '1'

TJAT Centering Procedure

a) Register 0017H + 80H*N TJAT Configuration

CENT	Set to ‘0’
LIMIT	Set to ‘0’
SYNC	Set to ‘0’
Reserved Bits	Set to ‘1’

b) Register 15H + 80H*N TJAT Jitter Attenuator Divider N1 Control

N1[7:0]	Set to 2FH

c) Register 16H + 80H*N TJAT Divider N2 Control

N2[7:0]	Set to 2FH

d) Register 16H + 80H*N TJAT Divider N2 Control

N2[7:0]	Set to A value of Table 12 below

e) Wait 100 ms

f) Register 15H + 80H*N TJAT Jitter Attenuator Divider N1 Control

N1[7:0]	Set to B value of Table 12 below

g) Wait 100 ms

h) Register 15H + 80H*N TJAT Jitter Attenuator Divider N1 Control

N1[7:0]	Set to C value Table 12 Below

i) Register 0017H + 80H*N TJAT Configuration

CENT	Set to ‘0’
LIMIT	Set to ‘0’
SYNC	Set to ‘1’
Reserved Bits	Set to ‘1’

j) Register 15H + 80H*N TJAT Jitter Attenuator Divider N1 Control

N1[7:0]	Set to C value of Table 12 below

k) Register 0017H + 80H*N TJAT Configuration

CENT	Set to '0'
LIMIT	Set to '0'
SYNC	Set to '0'
Reserved Bits	Set to '1'

l) Wait 100ms before conducting the procedure of section 16.1.2 on the tributary that corresponds to the TJAT that was just centered.

Table 12 N1 and N2 values for TJAT centering procedure

T1/E1 Transmit Clock (kHz)	T1			E1		
	A	B	C	A	B	C
1544	0xff	0x70	0xff	N/A	N/A	N/A
2048	N/A	N/A	N/A	0xff	0xa0	0xff

Note: This only applies to configurations where the T1/E1 transmit clock = Line Rate.

TTMP Re-provision Procedure

a) Register 1580H+08H*x+01H*y+20H*z: TTMP TU x in TUG2 y of TUG3 z, where x = 0-3, y = 0-6 and z = 0-2

PROV	Read to check if set to 1, if 0 tributary isn't provisioned thus pointers do not need to be checked

b) Register 1580H+08H*x+01H*y+20H*z: TTMP TU x in TUG2 y of TUG3 z, where x = 0-3, y = 0-6 and z = 0-2

PROV	Set to 0 if set to 1 in a) above

c) Wait 1 us

d) Register 1580H+08H*x+01H*y+20H*z: TTMP TU x in TUG2 y of TUG3 z, where x = 0-3, y = 0-6 and z = 0-2

PROV	Set to 1 to attempt to center the FIFO

e) Wait 250ms before conducting the procedure of section 16.1.2 on the tributary that was just re-provisioned.

16.1.2 TTMP FIFO Check Procedure

a) Register 15E6H FIFO Depth

FIFO_DEPTH[3:0]	Read to 'fifoSize'

b) Register 15E7H MAP Debug SVRam Capture Address

Map capture address[6:0]	Set to '10 11 0101' for tug3 # 2, tug2 #5; tu #3 for example

c) Register 15E8H MAP Debut SVRam Control Signals and Bistint

map capture enable	Set to '1'
map read enable	Set to '1'
Bistinit_abort	Set to '0'

d) Wait 6 ms

e) Register 15E8H MAP Debut SVRam Control Signals and Bistint

map capture enable	Set to '0'
map read enable	Set to '1'
Bistinit_abort	Set to '0'

f) Register 15F3 Byte 3 of the TTMP Vector

Unused	
Unused	
Unused	
readPointer[4]	Read
readPointer[3]	Read
readPointer[2]	Read
readPointer[1]	Read
writePointer[4]	Read

g) Register 15F2 Byte 2 of the TTMP Vector

writePointer[3]	Read
writePointer[2]	Read
writePointer[1]	Read
Unused	
Unused	
Unused	
Unused	
Unused	

h) If |(writePointer – readPointer)| <= 1 or

|(writePointer – readPointer)| >= (fifosize – 2)

then the Pointers are out of range. Repeat the TJAT centering procedure in 16.1.1.

16.1.3 Operation in VT/TU Mapping Mode

Procedure for Ingress Datapath Recovery

Once the datapath has been restored, the RJAT should be centered.

For all cases the TU-LOP alarm (located in register 1240H for TU#1 of TUG2#1) and the TU-AIS alarm (located in register 1241H for TU#1 of TUG2#1) as the trigger for centering the RJAT FIFO.

In framed E1 mode you can optionally use the removal of the E1 RED Alarm (located in register 0067+80*N) as the trigger for centering the RJAT FIFO. The centering procedure will cause a sudden bit slip and thus will cause the E1 framer to have a single change of frame alignment

Once the centering procedure has been completed an interval of 50ms is required before, optionally, switching back to looptimed mode if applicable.

RJAT Centering Procedure

a) Register 0013H + 80H*N RJAT Configuration

CENT	Set to ‘0’
LIMIT	Set to ‘0’
SYNC	Set to ‘1’
Reserved Bits	Set to ‘1’

b) Register 011H+80H*N RJAT Output Clock Divider N1 Control

N1[7:0]	Set to 2FH

c) Register 0013H + 80H*N RJAT Configuration

CENT	Set to ‘0’
LIMIT	Set to ‘0’
SYNC	Set to ‘0’
Reserved Bits	Set to ‘1’

d) After the RJAT centering is complete the TEMUX/TEMAP INSBI should be reset if the SBI bus is in use.

Register 1726H: INSBI Tributary Control Indirect Access Data

ENBL	Set to 1 again to reset recovered tributary

Algorithm for Datapath Corruption Restoration with Internally Timed Link

With the T1 or E1 link internally timed, upon detection of datapath corruption the RJAT Centering Procedure should be used before bringing the link back up as described above.

A sample algorithm is as follows:

```
#define data_corruption_event // either E1 RED or TU-AIS/LOP as noted above
processed by an interrupt service routine

#define centerRJAT() // Centering procedure as shown above

#define declare_link_up // Routine for bringing up a link

#define declare_link_down // Routine for tearing down a link

#define ingress_SBI_reset  // Routine for resetting a tributary on the ingress
SBI bus if SBI bus is used

if (!data_corruption_event) {

  centerRJAT(framer)

  wait 50ms

  ingress_SBI_reset(trib)

  declare_link_up(framer)

  } else {

      declare_link_down(framer)

      }
```

Algorithms for Switching From Internally Timed to Looptimed and Vice Versa

When switching from looptimed to internally timed mode, or vice-versa, the initialization sequence is important. Once the desired mode has been set, the TJAT should be centered using the TJAT Centering Procedure in section 16.1.1 above and the TTMP FIFO Check Procedure listed in 16.1.2 above should also be followed.

Sample algorithms are as follows:

```
looptime(framer) {

  write temux/temap 0x04+(0x80*$framer) = 0x62

  centerTJAT(framer)

  check_TTMP_pointers(framer)

}

internaltime(framer) {

  write temux/temap 0x04+(0x80*$framer) = 0x61

  centerTJAT(framer)

  check_TTMP_pointers(framer)

}
```

Algorithm for Datapath Corruption and Restoration When Link is Looptimed

With the T1 or E1 link looptimed, upon detection of datapath corruption as defined above, the transmit timing reference to TJAT must be changed to the normal transmit timing source. This occurs because the recovered clock for that link is not valid. Thus when the datapath is restored not only must the RJAT Centering Procedure above be used before bringing the link back up but the TJAT Centering Procedure from section 16.1.1 should be used after referencing it back to the recovered clock.

A sample algorithm is as follows:

```
#define data_corruption_event // either framed or unframed as noted above
processed by an interrupt service routine

#define centerRJAT() // Recentering procedure as shown above

#define declare_link_up() // Routine for bringing up a link

#define declare_link_down() // Routine for tearing down a link

#define looptime() // write PLLREF[1:0]=10 of register 004H+80H*N

#define internaltime() write PLLREF[1:0]=01 of register 004H+80H*N

if (!data_corruption_event) {
```

```
centerRJAT(framer)

wait_50ms

looptime(framer)  // includes TJAT center, see above

declare_link_up(framer)

  } else {

    wait 15ms

    internaltime(framer) // includes TJAT center, see above

    declare_link_down(framer)

    }
```

16.1.4 TEMUX/TEMAP Programmed as SPE(TUG3) # 3 Special Requirement

When the TEMUX/TEMAP is setup to receive SPE #3(LDROPSEL[1:0] of register 1200H = 11) of a given STS3 you must use the RTDM's time switch RAM to look at the copy of SPE#3 that exists on SPE#2. Otherwise you will see data corruption in the framer adjacent to the framer receiving TU-AIS. The internal RAM makes a copy of the data in SPE #3 in all three TUG3s in this configuration so to prevent this problem from occurring, the RTDM Time Switch should be setup to switch the copy of SPE#3's data in TUG3 #2 to TUG3 #3.

The following is a script to switch TU #1 of TUG2 #1 of TUG3 #2 to TU#1 of TUG2 #1 of TUG3 #3. It should be repeated for all 28 VT1.5/TU11s for T1 mode or all 21 VT2/TU12s for E1 mode.

a) Register 12E2H RTDM Time Switch Page Control

APAGE	Set to 0 when configuring page 1 Set to 1 when configuring page 0

b) Register 12A0H RTDM TU #1 in TUG2 #1 of TUG3#2, Control

PROV	Set to 1

c) Register 12C0H RTDM TU #1 in TUG2 #1 of TUG3 #3, Control

PROV	Set to 1

d) Register 12E4H RTDM Indirect Time Switch Internal Link Address

INT_SPE[1:0]	Set to '11'
INT_LIINK[4:0]	Set to '00001'

e) Register 12E5H RTDM Indirect Ingress Tributary Data

ING_TUG3[1:0]	Set to ‘10’
ING_TUG2[2:0]	Set to ‘001’
ING_TU[2:0]	Set to ‘001’

f) Register 12E3H RTDM Indirect Time Switch Tributary RAM Status and Control

Check BUSY = 0 before:

RWB	Set to 0
PAGE	Set to 0 if APAGE of 12E2H was set to 1 Set to 1 if APAGE of 12E2H was set to 0

g) Repeat a) through f) for the other 27VT1.5/TU11s or 20VT2/TU12s.

h) Register 12E2H RTDM Time Switch Page Control

APAGE	Set to 0 if PAGE 0 was just configured Set to 1 if PAGE 1 was just configured

i) Register 1201H SONET/SDH Master Ingress Configuration

ITSEN	Set to 1

16.2 TU-11 (VT1.5) or TU-12 (VT2) Master Configuration

a) Register 0001H: Global Configuration

OPMODE[1:0]	‘01’ Mapper/Multiplexer Mode ‘00’ High Density Framer Mode
LINOPT[1:0]	‘1X’ T1/E1 Mapper

b) Register 1200H: SONET/SDH Master/Configuration

RESET	'1' SONET/SDH Mapper is held in RESET '0' SONET/SDH is operating in normal mode.
LDROPSEL[1:0]	Selects which DROP side SPE or full Payload the TEMUX/TEMAP will have access to. '00' Full STS-3/STM-1 '01' SPE #1 '10' SPE #2 '11' SPE #3
LADDSEL[1:0]	Selects which ADD side SPE or full Payload the TEMUX/TEMAP will have access to. '00' Full STS-3/STM-1 '01' SPE #1 '10' SPE #2 '11' SPE #3 (See additional notes in datasheet)
LADDOE	'0' Line ADD Bus driven only valid data otherwise the bus is in tristate. '1' Line ADD Bus driven permanently and the LAOE signal is driven whenever the data on the line ADD bus is valid.

c) Register 1201H: SONET/SDH Master Ingress Configuration

LDOP	'0' Expect even parity on drop bus '1' Expect odd parity on drop bus
INCLDC1J1VI	'0' LDC1J1V1 pin is not included in parity calculations Must be programmed to 0 for proper operation.
INCLDPL	'0' LDPL pin is not included in parity calculations '1' LDPL pin is included in parity calculations
ITSEN	'0' No Tributary switching is allowed between multiple TEMUX/TEMAP's sharing an TELECOM-BUS. '1' Tributary switching is allowed between multiple TEMUX/TEMAP's sharing a TELECOMBUS. (See RTDM Time Switch Section) (If ITSEN ='1' Ingress VTPP must be bypassed via IVTPPBYP bit).
IVTPPBYP	'0' Ingress VTPP is active. '1 Ingress VTPP is not active. Must be set to '1' if using the TUPP_PLUS device. Should be set to '1' if planning to use the TTMP block to do VT/TU switching within multiple TEMUX/TEMAP devices. If VTPP is by passed J1 octet must be in a fixed position and LDV5, LDPL and LDTPL signals must be valid
ITMFEN	'0' Ingress VTPP uses H4 input to locate tributary boundaries. '1' Ingress VTPP uses LDC1J1V1 bytes to locate multiframe boundary.

d) Register 1202H: SONET/SDH Master Egress Configuration

LAOP	'0' Expect even parity generated on add bus '1' Expect odd parity generated on add bus
INCLAC1J1VI	'0' LAC1J1V1 pin is not included in parity calculations '1' LAC1J1V1 pin is included in parity calculations
INCLAPL	'0' LAPL pin is not included in parity calculations '1' LAPL pin is included in parity calculations
LAV1EN	'0' LAC1J1V1 output indicates the C1 and optionally the J1 byte '1' LAC1J1V1 output indicates C1, and the optionally J1 and the V1 byte.
LAJ1EN	'0' LAC1J1V1 output indicates the C1 byte and optionally the third byte after J1 if LAVJ1EN is set high. '1' LAC1J1V1 output indicates the C1, J1 and optionally the third byte after J1 (V1)
ETSEN	'0' No Tributary switching is allowed between multiple TEMUX/TEMAP's sharing an TELECOM-BUS. '1' Tributary switching is allowed between multiple TEMUX/TEMAP's sharing an TELECOM-BUS. (See TTMP TSRAM section) (If ETSEN ='1' Egress VTPP must be bypassed via EVTPPBYP bit).
LOCK0	'0' J1 byte is forced to the byte immediately following C1 bytes (pointer offset 522) '1' J1 byte is forced to byte immediately following the H3 bytes (pointer offset 0)

16.2.1 TU-11 (VT1.5) OR TU-12 (VT2) Mapping AU3 Mode

a) Register 1201H: SONET/SDH Master Ingress Configuration

ICONCAT	'0' for AU3 Mode

b) Register 1202H: SONET/SDH Master Egress Configuration

ECONCAT	'0' for AU3 Mode

c) Register 1203H: SONET/SDH Master Ingress VTPP Configuration

ITUG3	'0' for AU3 mode
OTUG3	'0' for AU3 mode

d) Register 1204H: SONET/SDH Master Egress VTPP Configuration

ITUG3	'0' for AU3 mode
OTUG3	'0' for AU3 mode

16.2.2 TU-11 (VT1.5) OR TU-12 (VT2) Mapping AU4 Mode

a) Register 1201H: SONET/SDH Master Ingress Configuration

ICONCAT	'1' for AU4 Mode

b) Register 1202H: SONET/SDH Master Egress Configuration

ECONCAT	'1' for AU4 Mode

c) Register 1203H: SONET/SDH Master Ingress VTPP Configuration

ITUG3	'1' for AU4 mode
OTUG3	'1' for AU4 mode

d) Register 1204H: SONET/SDH Master Egress VTPP Configuration

ITUG3	'1' for AU4 mode
OTUG3	'1' for AU4 mode

16.3 VTPP Set Up For TU-11 (VT1.5) OR TU-12 (VT2) Mapping

a) Register 1200H: SONET/SDH Master/Configuration

VTMPRST	'0' VT Mappers Active
DS3MPRST	'1' DS3 Mapper in RESET

16.3.1 Ingress VTPP Master Set up for TU-11 (VT1.5) or TU-12 (VT2) Mapping

a) Register 1203H: SONET/SDH Master Ingress VTPP Configuration

SOS	'0' Pointer changes as normal '1' Pointer changes have occurred at least three frames ago
MONIS	'0' Outgoing stream monitored for tributary pointer justifications '1' Incoming stream is monitored for tributary pointer justifications
ICODE	'0' IDLE code is chosen to be all 0's '1' IDLE code chosen to be all 1's
NOFILT	'0' Illegal variations from Normal Tributary Pointer values and not accompanied by a new flag are ignored '1' Pointer variations take place immediately

b) Register 1204H: SONET/SDH Master Egress VTPP Configuration

EVTPPBYP	'0' Egress VTPP is active (used in TVT mode) '1' Egress VTPP is bypassed (normal operating mode)
EPTRBYP	'0' VTPP Pointer Interpretation allowed '1' VTPP Pointer Interpretation bypassed

c) Register 1240H, 1242H, 1244H, 1246H, 1248H, 124AH, 124CH: VTPP Ingress, TU#1 in TUG2 #1 to TUG2 #7, Configuration and Status
Register 1250H, 1252H, 1254H, 1256H, 1258H, 125AH, 125CH: VTPP Ingress, TU#2 in TUG2 #1 to TUG2 #7, Configuration and Status

Register 1260H, 1262H, 1264H, 1266H, 1268H, 126AH, 126CH: VTPP Ingress, TU#3 in TUG2 #1 to TUG2 #7, Configuration and Status

Register 1270H, 1272H, 1274H, 1276H, 1278H, 127AH, 127CH: VTPP Ingress, TU#4 in TUG2 #1 to TUG2 #7, Configuration and Status (Only applies to TU-11 (VT 1.5) Mapping)

Reserved	'1' Must be set to '1'
TU11	'1' TU11 (VT1.5) Mapping '0' TU12 (VT2) Mapping
PF	'0' Normal operation '1' Any variation in FIFO depth will cause and outgoing pointer justification event
ALARME	'0' Normal operation '1' Enables LOP and Path AIS Interrupts per TUG-11
DLOP	'0' Normal operation '1' NDF in TU-11 is inverted
IPAIS	'0' Normal '1' Path AIS for TU-11 by forcing all ones into tributary bytes.

d) Register 1241H, 1243H, 1245H, 1247H, 1249H, 124BH, 124DH: VTPP Ingress, TU#1 in TUG2 #1 to TUG2 #7, Alarm Status

Register 1251H, 1253H, 1255H, 1257H, 1259H, 125BH, 125DH: VTPP Ingress, TU#2 in TUG2 #1 to TUG2 #7, Alarm Status

Register 1261H, 1263H, 1265H, 1267H, 1269H, 126BH, 126DH: VTPP Ingress, TU#3 in TUG2 #1 to TUG2 #7, Alarm Status

Register 1271H, 1273H, 1275H, 1277H, 1279H, 127BH, 127DH: VTPP Ingress, TU#4 in TUG2 #1 to TUG2 #7, Alarm Status (Register applies to TU-11 only)

RELAYAIS	'0' AIS declared after 3 consecutive AIS indications '1' AIS declared of a single AIS
PEE	'0' No interrupt on FIFO overflow or underflow '1' Interrupt on FIFO overflow or underflow

16.4 RTDM Receive Tributary Demapper Set-up for TU-11 (VT1.5) or TU-12 (VT2) Mapping

When the TEMUX/TEMAP is programmed with a specific SPE# 1,2 or 3 as selected from register 1200H, then only the TUG3# group that matches the selected SPE# has to be provisioned. All 3 TUG3 groups are accessible for section 16.3.1 and only the TU#s selected by the SPE# should be provisioned, up to 28 TU11s or 21 TU12s.

a) Register 1280H, 1281H, 1282H, 1283H, 1284H, 1285H, 1286H: RTDM TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Register 1288H, 1289H, 128AH, 128BH, 128CH, 128DH, 128EH: RTDM TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Register 1290H, 1291H, 1292H, 1293H, 1294H, 1295H, 1296H: RTDM TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Register 1298H, 1299H, 129AH, 129BH, 129CH, 129DH, 129EH: RTDM TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control (Applies to TU-11 (VT1.5) mapping only).

Register 12A0H, 12A1H, 12A2H, 12A3H, 12A4H, 12A5H, 12A6H: RTDM TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Register 12A8H, 12A9H, 12AAH, 12ABH, 12ACH, 12ADH, 12AEH: RTDM TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Register 12B0H, 12B1H, 12B2H, 12B3H, 12B4H, 12B5H, 12B6H : RTDM TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Register 12B8H, 12B9H, 12BAH, 12BBH, 12BCH, 12BDH, 12BEH: RTDM TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control (Applies to TU-11 (VT1.5) mapping only)

Register 12C0H, 12C1H, 12C2H, 12C3H, 12C4H, 12C5H, 12C6H: RTDM TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Register 12C8H, 12C9H, 12CAH, 12CBH, 12CCH, 12CDH, 12CEH: RTDM TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Register 12D0H, 12D1H, 12D2H, 12D3H, 12D4H, 12D5H, 12D6H : RTDM TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Register 12D8H, 12D9H, 12DAH, 12DBH, 12DCH, 12DDH, 12DEH: RTDM TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control(Applies to TU-11 (VT1.5) mapping only)

TU11, T1	'00' E1 in TU-12 (VT2) '01' T1 in TU-12 '10' T1 in TU-11 (VT1.5)
PROV	'0' De Mapping is disabled '1' De Mapping is enabled
AIS	'0' Normal '1' AIS enabled, all bits of demapped T1 or E1 stream are set high

b) Register 12E0H: RDTM Pointer Justification Rate Control

T1RATE[1:0]	Controls the base rate at which an incoming tributary pointer justification is leaked out for tributaries carrying a T1 stream. MUST SET to '10' 0.50 second for proper operation
E1RATE[1:0]	Controls the base rate at which an incoming tributary pointer justification is leaked out for tributaries carrying an E1 stream. '10' 0.50 second

16.4.1 RDTM Tributary Switching

The internal RDTM ram must be correctly set-up in order for tributary switching to occur across different SPE's. The switching will only occur if the ITSEN bit is set in the Master SONET/SDH Ingress Configuration Register (1201H). **The ITSEN bit should be the last bit to be set**. For access to all tributaries within an STS-3/STM-1 the LDROPSEL[1:0] bits in the SONET/SDH Master Configuration Register should be set to '00' (1200H).

The RDTM is very powerful in that it can for example de map any of the 84 T1 or 63 E1 from a full STS-3 or a combination of payloads into to a single SPE of TEMUX/TEMAP which must be configured for either 21 E1s or 28 T1s.

Because of this de mapping capability the RDTM must be configured via indirect register access. Within each SPE assigned to each TEMUX/TEMAP all VTs must be configured for either TU-11 (VT1.5) or TU-12 (VT2). The TEMUX/TEMAP also provide two memory maps referred to as APAGE with only one page active at each time. This enables software to set up a set of indirect register off line in one memory map while the TEMUX/TEMAP is transferring data via another memory map.

The RTDM registers and sequence of read and write transfers are described in detail below

Sequence to Write to the Indirect RDTM

1. Set the TU#, TUG2# and TUG3# from a full STS-3 in the RTDM Tributary Data Register (12E5H)

2. Set the TEMUX/TEMAP Tributary number in RTDM Indirect Time Switch Internal Link Address Register (12E4H) that you want the tributary to be assigned to.

3. Set the RWB ='0' for a write, Select the PAGE to be written to. The PAGE should be off line for configuration in the RDTM Indirect Time Switch Tributary RAM Status and Control Register (12E3H).

4. Wait for the BUSY bit to clear in the RDTM Indirect Time Switch Tributary RAM Status and Control Register (12E3H).

5. Repeat from Stage 1 for further writes.

6. Once the PAGE has been set up activate the page by setting the relevant bit in the RTDM Time Switch Page Control Register (12E2H).

Sequence to Read from the Indirect RDTM

1. Set the TEMUX/TEMAP Tributary number in RTDM Indirect Time Switch Internal Link Address Register (12E4H) that you want to read.

2. Set the RWB =’1 for a read’, Select the PAGE to be read. The PAGE should be off line for configuration in the RDTM Indirect Time Switch Tributary RAM Status and Control Register (12E3H).

3. Wait for the BUSY bit to clear in the RDTM Indirect Time Switch

4. Tributary RAM Status and Control Register (12E3H).

5. Read the TU#, TUG2# and TUG3# from the RTDM Tributary Data Register (12E5H) to find the STS-3 tributary that is mapped to this TEMUX/TEMAP tributary.

6. Repeat from Stage 1 for further indirect reads.

7. Once the PAGE has been read you may activate the page by setting the relevant bit in the RTDM Time Switch Page Control Register (12E2H).

RDTM Indirect Memory Registers

a) Register 12E2H: RDTM Time Switch Page Control

APAGE	‘0’ Page 0 is used for active page for time switching ‘1’ Page 1 is used for active page for time switching

b) Register 12E2H: RDTM Time Switch Page Control

RWB	Set to ‘0’ for an Indirect Write Access Set to ‘1’ for an Indirect Read Access
PAGE	Set to ‘0’ for PAGE0 Set to ‘1’ for PAGE1 (Only configure the page that is inactive as set by the APAGE bit of Register 12E2H)
BUSY	Poll this bit until it is set to ‘0’ before making any indirect access.

c) Register 12E4H: RDTM Indirect Time Switch Internal Link Address

INT_SPE[1:0]	Set to '01' for all TEMUX/TEMAP devices
INT_LINK[0:4]	Select the TEMUX/TEMAP Tributary For TU-11 (VT1.5) Range is 00001b to 11100b for 1 to 28 T1s For TU-12 (VT2) Range is 00001b to 10101b for 1 to 21 E1s

d) Register 12E5H: RDTM Indirect Ingress Tributary Data

ING_TUG3[1:0]	'01' Selects TUG3#1/ STS-1#1 '10' Selects TUG3#2/ STS-1#2 '11' Selects TUG3#3/ STS-1#3
ING_TUG2[2:0]	Range '001b to 111b to select 1 of 7 TUG-2 /VT Group
ING_TU[2:0]	Range '001b to 100b' select TU within a TUG2/VT Group For TU-11 range '001b to 100b' selects 1 of 4 TUs/VTs for T1 For TU-12 range '001b to 011b' selects 1 of 3 TUs/VTs for E1

16.5 RTOP Set up for TU-11 (VT1.5) or TU-12 (VT2)

a) Register 1205H: SONET/SDH Master RTOP Configuration

RD10	'0' RDI bit and RFI bit is filtered for 5 occurrences '1' RDI bit and RFI bit is filtered for 10 occurrences
PDI[2:0]	Sets the code used to convey Tributary Path Defect Indication (PDI-V) in the V5 byte

b) Register 1300H, 1308H, 1310H, 1318H, 1320H, 1328H, 1330H: RTOP, TU #1 in TUG2 #1 to TUG2 #7, Configuration

Register 1340H, 1348H, 1350H, 1358H, 1360H, 1368H, 1370H: RTOP, TU #2 in TUG2 #1 to TUG2 #7, Configuration

Register 1380H, 1388H, 1390H, 1398H, 13A0H, 13A8H, 13B0H: RTOP, TU #3 in TUG2 #1 to TUG2 #7, Configuration

Register 13C0H, 13C8H, 13D0H, 13D8H, 13E0H, 13E8H, 13F0H: RTOP, TU #4 in TUG2 #1 to TUG2 #7, Configuration (Only applicable in TU-11 (VT1.5) mapping)

RDIE	‘0’ No Interrupt ‘1’ Interrupt due to RDI
RFIE	‘0’ No Interrupt ‘1’ Enables Remote Failure Indication Interrupt
COPSLE	‘0’ No interrupt ‘1’ Interrupt on Path Signal Change
PSLME	‘0’ No interrupt ‘1’ Interrupt on Path Signal Label Mismatch with register
PSLUE	‘0’ No interrupt ‘1’ Interrupt generated on Path Signal Label becoming stable/unstable
BLKBIP	‘0’ BIP-2 errors counted on nibble basis ‘1’ BIP-2 errors counted on block basis
TU11	‘1’ For TU11 (VT1.5) ‘0’ For TU12 (VT2)
Reserved	‘1’

c) Register 1301H, 1309H, 1311H, 1319H, 1321H, 1329H, 1331H: RTOP, TU #1 in TUG2 #1 to TUG #7, Configuration and Alarm Status

Register 1341H, 1349H, 1351H, 1359H, 1361H, 1369H, 1371H: RTOP, TU #2 in TUG2 #1 to TUG #7, Configuration and Alarm Status

Register 1381H, 1389H, 1391H, 1399H, 13A1H, 13A9H, 13B1H: RTOP, TU #3 in TUG2 #1 to TUG #7, Configuration and Alarm Status

Register 13C1H, 13C9H, 13D1H, 13D9H, 13E1H, 13E9H, 13F1H: RTOP, TU #4 in TUG2 #1 to TUG #7, Configuration and Alarm Status (Only applicable in TU-11 (VT1.5) mapping)

PDIVEN	'0' PDI-V is asserted if the incoming path signal label matches the PDI code in PDI[2:0] of the RTOP Configuration Register '1' Tributary Path Defect Indication PDI-V is asserted
TUPTE	'0' AIS is only asserted on LOP (Loss of Pointer) or LOM (Loss of Multiframe Alarm)
RDIZ7EN	'0' RDI and RFI bits in V5 byte used to control RDIV and RFIV register. '1' Three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.
ERDIV[2]	'0' Normal operation '1' When RDIZ7EN is set high these bits are set to the new code of the RDI bits in the Z7 byte seen for 5 or 10 consecutive multi frames determined by RDI10 bit in the RTOP configuration register.

16.6 Egress VTPP Set Up for TU-11 (VT1.5) or TU-12 (VT2) Mapping

a) Register 1400H, 1402H, 1404H, 1406H, 1408H, 140AH, 140CH: VTPP Egress, TU#1 in TUG2 #1 to TUG2 #7, Configuration and Status

Register 1410H, 1412H, 1414H, 1416H, 1418H, 141AH, 141CH: VTPP Egress, TU#2 in TUG2 #1 to TUG2 #7, Configuration and Status

Register 1420H, 1422H, 1424H, 1426H, 1428H, 142AH, 142CH: VTPP Egress, TU#3 in TUG2 #1 to TUG2 #7, Configuration and Status

Register 1430H, 1432H, 1434H, 1436H, 1438H, 143AH, 143CH: VTPP Egress, TU#4 in TUG2 #1 to TUG2 #7, Configuration and Status (Applicable to TU11 (VT1.5) Mapping only)

Reserved	'1' Must be set to '1'
TU11	'1' TU11 (VT1.5) '0' TU12 (VT2)
PF	'0' Normal operation '1' Any variation in FIFO depth will cause and outgoing pointer justification event
ALARME	'0' Normal operation '1' Enables LOP and Path AIS Interrupts per TUG-11
DLOP	'0' Normal operation '1' NDF in TU-11 is inverted
IPAIS	'0' Normal '1' Path AIS for TU-11 by forcing all ones into tributary bytes.

b) Register 1401H, 1403H, 1405H, 1407H, 1409H, 140BH, 140DH: VTPP Egress, TU#1 in TUG2 #1 to TUG2 #7, Alarm Status

Register 1411H, 1413H, 1415H, 1417H, 1419H, 141BH, 141DH: VTPP Egress, TU#2 in TUG2 #1 to TUG2 #7, Alarm Status

Register 1421H, 1423H, 1425H, 1427H, 1429H, 142BH, 142DH: VTPP Egress, TU#3 in TUG2 #1 to TUG2 #7, Alarm Status

Register 1431H, 1433H, 1435H, 1437H, 1439H, 143BH, 143DH: VTPP Egress, TU#4 in TUG2 #1 to TUG2 #7, Alarm Status (Applicable to TU-11 (VT1.5) mapper only)

RELAYAIS	'0' AIS declared after 3 consecutive AIS indications '1' AIS declared of a single AIS
PEE	'0' No interrupt on FIFO overflow or underflow '1' Interrupt on FIFO overflow or underflow

16.7 TRAP Set up for TU-11 (VT1.5) or TU-12 (VT2) Mapping

When the TEMUX/TEMAP is programmed with a specific SPE# 1,2 or 3 as selected from register 1200H, then only the TUG3# group that matches the selected SPE# has to be provisioned. If the entire STM1 is selected then all 3 TUG3 groups are accessible for the TRAP, TTOP and TTMP registers and only up to 28 TU11s or 21 TU12s can be selected. The same 28/21 should be selected for the TRAP, TTOP and TTMP.

a) Register 1480H, 1481H, 1482H, 1483H, 1484H, 1485H, 1486H: TRAP, TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Register 1488H, 1489H, 148AH, 148BH, 148CH, 148DH, 148EH: TRAP, TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Register 1490H, 1491H, 1492H, 1493H, 1494H, 1495H, 1496H: TRAP, TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Register 1498H, 1499H, 149AH, 149BH, 149CH, 149DH, 149EH: TRAP, TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control (Applicable to TU-11 (VT1.5) Mapper only)

Register 140AH, 14A1H, 14A2H, 14A3H, 14A4H, 14A5H, 14A6H: TRAP, TU #1 in TUG2 #1 to TUG2 #7, of TUG3 #2 Control

Register 14A8H, 14A9H, 14AAH, 14ABH, 14ACH, 14ADH, 14AEH: TRAP, TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Register 14B0H, 14B1H, 14B2H, 14B3H, 14B4H, 14B5H, 14B6H: TRAP, TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Register 14B8H, 14B9H, 14BAH, 14BBH, 14BCH, 14BDH, 14BEH: TRAP, TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control (Applicable to TU-11 (VT1.5) only)

Register 14C0H, 14C1H, 14C2H, 14C3H, 14C4H, 14C5H, 14C6H: TRAP, TU #1 in TUG2 #1 to TUG2 #7, of TUG3 #3 Control

Register 14C8H, 14C9H, 14CAH, 14CBH, 14CCH, 14CDH, 14CEH: TRAP, TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Register 14D0H, 14D1H, 14D2H, 14D3H, 14D4H, 14D5H, 14D6H: TRAP, TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Register 14D8H, 14D9H, 14DAH, 14DBH, 14DCH, 14DDH, 14DEH: TRAP, TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control (Applicable to TU-11 (VT1.5) only)

Reserved	'1'
TU11	'1' TU11 (VT1.5) '0' TU12 (VT2)
FORCEEN	'0' RDI and RFI reflect Remote Alarm Status from the Remote Alarm Source via the TRAP Indirect Remote Alarm Register. '1' RDI and RFI controlled by register bits.
RFI	Assuming FORCEEN is high RFI controls value of RFI Indication to TTOP for TU '0' No RFI Alarm '1' RFI Alarm
RDI	Assuming FORCEEN is high RDI controls value of RDI Indication to TTOP for TU '0' No RDI Alarm '1' RDI Alarm

ERDI	'0' Normal RDI. TTOP will insert RDI output into bit 8 of V5 and RFI into bit 4 of V5 byte. '1' Extended RDI Encoding. TTOP will insert RDI into bit 5 of Z7 and RFI into bit 6 of the Z7 byte.
POHDIS	'0' TU is processed as normal '1' TU is processed as Transparent VTs from the SBI bus. Configured by setting the ETVT bit in the TTMP block.

b) Register 14E3H: TRAP RDI Control

RDI20MF[3:0]	'0' The RDI Value of TUG3 #X will be kept for 10 Multiframes '1' The RDI Value for TUG3 #X will be kept for 20 Multiframes as GR-253.
RDIPRIA[1:0], RDIPRIB[1:0]	Specify alarm code priorities (See datasheet for more information)

c) Register 14E8H, 14E9H, 14EAH, 14EBH, 14ECH, 14EDH, 14EEH: TRAP Remote ALARM Port TUG2 #1 to TUG2 #7 of TUG3 #1 Configuration

Register 14FOH, 14F1H, 14F2H, 14F3H, 14F4H, 14F5H, 14F6H: TRAP Remote ALARM Port TUG2 #1 to TUG2 #7 of TUG3 #2 Configuration

Register 14F8H, 14F9H, 14FAH, 14FBH, 14FCH, 14FDH, 14FEH: TRAP Remote ALARM Port TUG2 #1 to TUG2 #7 of TUG3 #3 Configuration

Reserved	'1'
TU11	'1' TU11 (VT1.5) '0' TU12 (VT2)

The TRAP contains some Internal RAM which is used map the alarm condition from one received tributary to that of another on the transmit side. The alarm conditions for the Tributaries may also be taken from the input ports RADEAST and RADWEST serial alarm ports. Three memory pages are available for tributary set up. The pages available are the RADWEST serial port page, RADEAST serial port page and the RTOP Ingress Data page.

The TRAP registers and sequence of read and write transfers are described in detail below.

Sequence to Write to the Indirect TRAP Interface

1. Select the destination Tributary of the ALARM from the full STS-3 payload via setting the TUG3#, TUG2# and TU in TRAP Indirect Remote Alarm Tributary Address Register (14E1H).

2. Set the Tributary to be assigned from the TEMUX/TEMAP via the TRAP Indirect Datapath Tributary Data Register (14E2H).

3. Set the RWB bit to ‘0’ to select a write, and select the page for the write operation in the TRAP Indirect Remote Alarm Page Address (14E0H).

4. Poll the BUSY bit in the TRAP Indirect Remote Alarm Page Address (14E0H) until it is set to ‘0’

5. Repeat from stage 1 for further write update.

Sequence to Read from the Indirect TRAP Interface

1. Select the destination Tributary of the ALARM from the full STS-3 payload via setting the TUG3#, TUG2# and TU in TRAP Indirect Remote Alarm Tributary Address Register (14E1H).

2. Set the RWB bit to ‘1’ to select a read, and select the page for the read operation in the TRAP Indirect Remote Alarm Page Address (14E0H).

3. Poll the BUSY bit in the TRAP Indirect Remote Alarm Page Address (14E0H) until it is set to ‘0’.

4. Read the TEMUX/TEMAP tributary number of the datapath tributary that is associated with the remote alarm tributary from the TRAP Indirect Datapath Tributary Data Register (14E2H).

5. Repeat from stage 1 for further read requests.

Indirect TRAP Interface Registers

a) Register 14E0H: TRAP Indirect Remote Alarm Page Address

RWB	Set to ‘0’ for an Indirect Write Access Set to ‘1’ for an Indirect Read Access
RASEL[1:0]	Select memory page for access ‘01’ RADEAST Serial Alarm Port Page ‘10’ RADWEST Serial Alarm Port Page ‘11’ RTOP Ingress Data Page
BUSY	Poll this bit until it is set to ‘0’ before making any indirect access.

b) Register 14E2H: TRAP Indirect Datapath Tributary Data

DTU[1:0]	Ranges from ‘01b to 11b’ specifies TUG3
DTUG2[0:4]	Select the TEMUX/TEMAP source Tributary For TU-11 (VT1.5) Range is 00001b to 11100b for 1 to 28 T1s For TU-12 (VT2) Range is 00001b to 10101b for 1 to 21 E1s

c) Register 14E1H: Indirect Remote Alarm Tributary Address

RTUG3[1:0]	'01' Selects TUG3#1/ STS-1#1 '10' Selects TUG3#2/ STS-1#2 '11' Selects TUG3#3/ STS-1#3
RTUG2[2:0]	Range '001b to 111b to select 1 of 7 TUG-2 /VT Group
RTU[2:0]	Range '001b to 100b' select TU within a TUG2/VT Group For TU-11 range '001b to 100b' selects 1 of 4 TUs/VTs for T1 For TU-12 range '001b to 011b' selects 1 of 3 TUs/VTs for E1

16.8 Set up the Transmit Path Overhead Processor (TTOP) FOR TU-11 (VT1.5) or TU12 (VT2).

a) Register 1500H, 1501H, 1502H, 1503H, 1504H, 1505H, 1506H: TTOP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Register 1508H, 1509H, 150AH, 150BH, 150CH, 150DH, 150EH: TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Register 1510H, 1511H, 1512H, 1513H, 1514H, 1515H, 1516H: TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Register 1518H, 1519H, 151AH, 151BH, 151CH, 151DH, 151EH: TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control (Applicable to TU-11 (VT1.5) only)

Register 1520H, 1521H, 1522H, 1523H, 1524H, 1525H, 1526H: TTOP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Register 1528H, 1529H, 152AH, 152BH, 152CH, 152DH, 152EH: TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Register 1530H, 1531H, 1532H, 1533H, 1534H, 1535H, 1536H: TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Register 1538H, 1539H, 153AH, 153BH, 153CH, 153DH, 153EH: TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control (Applicable to TU-11 (VT1.5) only)

Register 1540H, 1541H, 1542H, 1543H, 1544H, 1545H, 1546H: TTOP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Register 1548H, 1549H, 154AH, 154BH, 154CH, 154DH, 154EH: TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Register 1550H, 1551H, 1552H, 1553H, 1554H, 1555H, 1556H: TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Register 1558H, 1559H, 155AH, 155BH, 155CH, 155DH, 155EH: TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control (Applicable to TU-11 (VT1.5) only)

Reserved	'1'
TU11	'1 TU11 (VT1.5) Active TU #1, #2, #3 and #4
PSL[2:0]	Default 'b010' denotes asynchronous mapping of payload into tributary. This represent the path signal inserted into the PSL field of the V5 tributary.
TTIEN	'0' Trail Trace Identifier insertion is disabled. '1' Trail Trace Identifier insertion is enabled.

ERDI	'0' Normal RDI selected. Value of RDI from TRAP is inserted into bit 8 of V5 byte. RFI is inserted from TRAP into bit 4 of V5 byte. '1' Extended mode selected. Value of RDI is inserted from TRAP is inserted into bit 6 of the V5 byte. RFI value is inserted from TRAP into bit 4 of V5 byte.
IDLE	'0' Tributary processed as normal '1' Egress Tributary payload bytes all set to zero or all one selected by ICODE register bit.

c) Register 1560H, 1561H, 1562H, TUG3 #1, #2 and #3 Control

UPOHV	'0' Unused Tributary Path Overhead bits are set low '1' Unused Tributary Path Overhead bits are set high
ICODE	'0' Tributary Payload for IDLE tributaries all set to zero '1' Tributary Payload for IDLE tributaries if an Idle Tributary (the corresponding IDLE bit set high) is set to all ones.

The TTOP contains some Internal RAM, which is used to set up the J2 byte tributary trail trace identifier. For SONET applications this is a 64 byte message and for SDH applications this is a 16 byte message. Thus for SDH, it must be written 4 times to fill the 64 bytes of RAM.

Because of this long message the TTOP tributary trail trace identifier must be configured via indirect register access. The TEMUX/TEMAP provide two rams one referred to as a buffer ram and the other referred to as the shadow ram. This enables software to set up a set of indirect registers off line in one ram while the TEMUX/TEMAP is transferring data via in real time using the other ram.

The TTOP registers and sequence of read and write transfers are described in detail below

Sequence to WRITE to the Indirect TTOP Interface

1. Select the RAM bank for set up from TTOP Trail Trace Identifier Page Select Register (1564H)

2. Set the TU#, TUG2# and TUG3# from a full STS-3 in the TTOP Indirect Trail Trace Identifier Tributary Select Register (1565H) to select the TU/VT.

3. Set the data for byte X of the Trail Trace Identifier in the TTOP Indirect Trail Trace Identifier Buffer Data Register (1567H)

4. Set the RWB ='0' for a write, Set the A[5:0] bits of the address for data byte X (Range 0 to 63 for a SONET J2 message or Range 0 to 15 for a SDH message) in the TTOP Indirect Trail Trace Identifier Buffer Address Register (1566H)

5. Wait for the BUSY bit to clear in the TTOP Indirect Trail Trace Identifier Buffer Address Register (1566H).

6. Repeat from Stage 3 for further writes until the complete 16 or 64 byte message is written into the indirect memory.

7. Repeat from Stage 2 for further Tributary Indirect Trail Trace Identifier Messages.

8. Once the memory map has been set up with all the Trail Trace Identifier Messages assigned to the Tributaries the memory map should be activated by setting the appropriate bit in the TTOP Trail Trace Identifier Page Select Register (1564H).

Sequence to READ from the Indirect TTOP Interface

1. Select the RAM bank for READ requests from the TTOP Trail Trace Identifier Page Select Register (1564H).

2. Set the TU#, TUG2# and TUG3# from a full STS-3 in the TTOP Indirect Trail Trace Identifier Tributary Select Register (1565H) to select the TU/VT.

3. Set the RWB =’1’ for a read request, Set the A[5:0] bits of the address for data byte X (Range 0 to 63 for a SONET J2 message or Range 0 to 15 for a SDH message) in the TTOP Indirect Trail Trace Identifier Buffer Address Register (1566H)

4. Wait for the BUSY bit to clear in the TTOP Indirect Trail Trace Identifier Buffer Address Register (1566H).

5. Read the data for byte X of the Trail Trace Identifier from the TTOP Indirect Trail Trace Identifier Buffer Data Register (1567H)

6. Repeat from Stage 3 for further byte reads until the complete 16 or 64 byte message has been read from indirect memory.

7. Repeat from Stage 2 for further Tributary Indirect Trail Trace Identifier Messages to be read.

8. Once the Trail Trace Identifier Messages assigned to the Tributaries have been read from the memory map this may be activated by setting the appropriate bit in the TTOP Trail Trace Identifier Page Select Register (1564H).

Indirect TTOP Interface Registers

a) Register 1564H: TTOP Trail Trace Identifier Page Select

USEBUF	‘0’ Buffer Ram is used for J2 messages ‘1’ Shadow Ram is used for J2 messages
SBUFINUSE	Read this bit to determine which RAM is in use presently by the TEMUX/TEMAP.

b) Register 1565H: TTOP Indirect Trail Trace Identifier Tributary Select

TUG3[1:0]	'01' Selects TUG3#1/ STS-1#1 '10' Selects TUG3#2/ STS-1#2 '11' Selects TUG3#3/ STS-1#3
TUG2[2:0]	Range '001b to 111b to select 1 of 7 TUG-2 /VT Group
TU[2:0]	Range '001b to 100b' select TU within a TUG2/VT Group For TU-11 range '001b to 100b' selects 1 of 4 TUs/VTs for T1 For TU-12 range '001b to 011b' selects 1 of 3 TUs/VTs for E1

c) Register 1566H: TTOP Indirect Trail Trace Identifier Buffer Address

BUSY	Read this bit to make sure it is set to '0' before any Indirect Access
RWB	'0' Triggers an Indirect Write operation '1' Triggers an Indirect Read operation
A[5:0]	Select the address of the J2 byte For SONET range is '000000b to 111111b' For SDH range is '000000b to 010000b'

d) Register 1567H: TTOP Indirect Trail Trace Identifier Buffer Data

D[7:0]	Data to be read or written for a byte of J2 message

16.9 TTMP Transmit tributary mapper Set up for TU-11 (VT1.5) or TU-12 (VT2)

a) Register 1580H, 1581H, 1582H, 1583H, 1584H, 1585H, 1586H: TTMP, TU #1 in TUG2 #1 to TUG2 #7, of TUG3 #1 Tributary Control

Register 1588H, 1589H, 158AH, 158BH, 158CH, 158DH, 158EH: TTMP, TU #2 in TUG2 #1 to TUG2 #7, of TUG3 #1 Tributary Control

Register 1590H, 1591H, 1592H, 1593H, 1594H, 1595H, 1596H: TTMP, TU #3 in TUG2 #1 to TUG2 #7, of TUG3 #1 Tributary Control

Register 1598H, 1599H, 159AH, 159BH, 159CH, 159DH, 159EH: TTMP, TU #4 in TUG2 #1 to TUG2 #7, of TUG3 #1 Tributary Control (Only applicable in TU-11 (VT1.5) mapping)

Register 15A0H, 15A1H, 15A2H, 15A3H, 15A4H, 15A5H, 15A6H: TTMP, TU #1 in TUG2 #1 to TUG2 #7, of TUG3 #2 Tributary Control

Register 15A8H, 15A9H, 15AAH, 15ABH, 15ACH, 15ADH, 15AEH: TTMP, TU #2 in TUG2 #1 to TUG2 #7, of TUG3 #2 Tributary Control

Register 15B0H, 15B1H, 15B2H, 15B3H, 15B4H, 15B5H, 15B6H: TTMP, TU #3 in TUG2 #1 to TUG2 #7, of TUG3 #2 Tributary Control

Register 15B8H, 15B9H, 15BAH, 15BBH, 15BCH, 15BDH, 15BEH: TTMP, TU #4 in TUG2 #1 to TUG2 #7, of TUG3 #2 Tributary Control (Only applicable in TU-11 (VT1.5) mapping)

Register 15C0H, 15C1H, 15C2H, 15C3H, 15C4H, 15C5H, 15C6H: TTMP, TU #1 in TUG2 #1 to TUG2 #7, of TUG3 #3 Tributary Control

Register 15B8H, 15B9H, 15BAH, 15BBH, 15BCH, 15BDH, 15BEH: TTMP, TU #4 in TUG2 #1 to TUG2 #7, of TUG3 #2 Tributary Control (Only applicable in TU-11 (VT1.5) mapping)

Register 15C8H, 15C9H, 15CAH, 15CBH, 15CCH, 15CDH, 15CEH: TTMP, TU #2 in TUG2 #1 to TUG2 #7, of TUG3 #3 Tributary Control

Register 15D0H, 15D1H, 15D2H, 15D3H, 15D4H, 15D5H, 15D6H: TTMP, TU #3 in TUG2 #1 to TUG2 #7, of TUG3 #3 Tributary Control

Register 15D8H, 15D9H, 15DAH, 15DBH, 15DCH, 15DDH, 15DEH: TTMP, TU #4 in TUG2 #1 to TUG2 #7, of TUG3 #3 Tributary Control (Only applicable in TU-11 (VT1.5) mapping)

TU11, T1	'00' E1 in TU-12 (VT2) '01" T1 in TU-12 '10' T1 in TU-11 (VT1.5)
PROV	'0' Tributary is not processed '1' Tributary is processed

ETVTPTRDIS	'0' Enables Egress VTPP to process the pointer. '1' Disables Egress VTPP from processing the pointer if pointer is not valid. If set to '1' VTPP does not use V1 and V2 pointer, but uses the V5 indicator to align the transparent VT
ETVT	'0' T1 or E1 will be asynchronously mapped into a VT1.5 and VT2 '1' Transparent Virtual Tributary from the SBI Bus will be output in the Egress direction
LAOE	'0' The tributary will not be output on the Line ADD '1' The tributary will be output on the Line ADD When LADDSEL[1:0] in Master SONET/SDH Configuration register is not set to '00' this bit has no effect

16.9.1 TTMP Tributary Switching

The internal TTMP ram must be correctly set-up in order for tributary switching to occur across different SPE's. The switching will only occur if the ETSEN bit is set in the Master SONET/SDH Egress Configuration Register (1202H). For access to all tributaries within an STS-3/STM-1 the LADDSEL[1:0] bits in the SONET/SDH Master Configuration Register should be set to '00' (1200H).

Because of this mapping capability the TTMP must be configured via indirect register access. Within each SPE assigned to each TEMUX/TEMAP all VTs must be configured for either TU-11 (VT1.5) or TU-12 (VT2). The TEMUX/TEMAP also provides two memory maps referred to as APAGE with only one page active at each time. This enables software to set up a set of indirect registers off line in one memory map while the TEMUX/TEMAP is transferring data via another memory map.

The TTMP registers and sequence of read and write transfers are described in detail below

Sequence to Write to the Indirect TTMP Interface

1. Set the TU#, TUG2# and TUG3# from a full STS-3 in the TTMP Indirect Egress Tributary Register (15E3H)

2. Set the TEMUX/TEMAP Tributary number in TTMP Indirect Time Switch Internal Link Data Register (15E4H) that you want the to be assigned to the full STS-3.

3. Set the RWB ='0' for a write, Select the PAGE to be written to. (The PAGE should be off line) for configuration in the TTMP Indirect Time Switch Tributary RAM Control and Status Register (15E2H).

4. Wait for the BUSY bit to clear in the TTMP Indirect Time Switch Tributary RAM Control and Status Register (15E2H).

5. Repeat from Stage 1 for further writes

6. Once the PAGE has been set up activate the page by setting the relevant bit in the TTMP Time Switch Page Control Register (15E1H).

Sequence to Read from the Indirect TTMP Interface

1. Set the TU#, TUG2# and TUG3# from a full STS-3 in the TTMP Indirect Egress Tributary Register (15E3H) that you want to read.

2. Set the RWB =’1’ for a read access, Select the PAGE to be read to. (The PAGE should be off line) for configuration in the TTMP Indirect Time Switch Tributary RAM Control and Status Register (15E2H).

3. Wait for the BUSY bit to clear in the TTMP Indirect Time Switch Tributary RAM Control and Status Register (15E2H).

4. Read the TEMUX/TEMAP Tributary number in TTMP Indirect Time Switch Internal Link Data Register (15E4H) to find out which STS-3 Tributary has been assigned to that TEMUX/TEMAP tributary.

5. Repeat from Stage 1 for further Reads

6. Once the PAGE has been read you may want to activate the page by setting the relevant PAGE bit in the TTMP Time Switch Page Control Register (15E1H).

Indirect TTMP Interface Map Registers

a) Register 15E1H: TTMP Time Switch Page Control

APAGE	‘0’ Page 0 is used for active page for time switching ‘1’ Page 1 is used for active page for time switching

b) Register 15E2H: TTMP Time Switch Page Control

RWB	Set to ‘0’ for an Indirect Write Access Set to ‘1’ for an Indirect Read Access
PAGE	Set to ‘0’ for PAGE0 Set to ‘1’ for PAGE1
BUSY	Poll this bit until it is set to ‘0’ before making any indirect access.

c) Register 15E4H: TTMP Indirect Time Switch Internal Link Data

INT_SPE[1:0]	’01 to 11’ for TEMUX/TEMAP #1 to TEMUX #3
INT_LINK[0:4]	Select the TEMUX/TEMAP Tributary For TU-11 (VT1.5) Range is 00001b to 11100b for 1 to 28 T1s For TU-12 (VT2) Range is 00001b to 10101b for 1 to 21 E1s

d) Register 15E3H: TTMP Indirect Egress Tributary Address

EGR_TUG3[1:0]	'01' Selects TUG3#1/ STS-1#1 '10' Selects TUG3#2/ STS-1#2 '11' Selects TUG3#3/ STS-1#3
EGR_TUG2[2:0]	Range '001b to 111b to select 1 of 7 TUG-2 /VT Group
EGR_TU[2:0]	Range '001b to 100b' select TU within a TUG2/VT Group For TU-11 range '001b to 100b' selects 1 of 4 TUs/VTs for T1 For TU-12 range '001b to 011b' selects 1 of 3 TUs/VTs for E1

16.9.2 Setting the FIFO Depth

a) Register 15E6H: FIFO Depth

FIFO_DEPTH[3:0]	Set to '1000'

This register configures the Depth of the FIFO inside the TTMP block. FIFO_DEPTH increases the depth of the input FIFOs. The value in the register is coded as an unsigned integer and is valid from 0 through 8. Other values are illegal. The effective depth is 8 + the value of the register. This value must be programmed for the TJAT centering procedure to operate correctly in section 16.1.1.

17 TU-3 (DS3) MAPPER Set Up (Not Supported for TECT3)

TU-3 (DS3) mapper mode is not supported for the TECT3. This entire section does not apply to the TECT3.

a) Register 0001H: Global Configuration

OPMODE[1:0]	'01' Mapper/Multiplexer Mode [1]
LINEOPT[1:0] [2]	'01' DS3 SONET/SDH Mapper
Notes: 1. This mode is not supported for the TETC3. 2. These bits are not supported for the TECT3.	

b) Register 1200H: SONET/SDH Master/Configuration

RESET	'1' SONET/SDH Mapper is held in RESET '0' SONET/SDH is operating in normal mode.
LDROPSEL[1:0]	Selects which DROP side SPE the TEMUX/TEMAP will access. '01' SPE #1 '10' SPE #2 '11' SPE #3
LADDSEL[1:0]	Selects which ADD side SPE the TEMUX/TEMAP will access. '01' SPE #1 '10' SPE #2 '11' SPE #3 (See additional notes in datasheet)
VTMPRST	'1' VT Mappers RESET
DS3MPRST	'0' DS3 Mapper is active
LADDOE	'0' Line ADD Bus driven only valid data '1' Line ADD Bus driven permanently and the LAOE signal is driven whenever the data on the line ADD bus is valid.

c) Register 1201H: SONET/SDH Master Ingress Configuration

ICONCAT	'0' Telecom Drop Bus runs in AU3 (STS-1) mode.
LDOP	'0' Expect even parity on drop bus '1' Expect odd parity on drop bus
INCLDC1J1VI	'0' LDC1J1V1 pin is not included in parity calculations '1' LDC1J1V1 pin is included in parity calculations
INCLDPL	'0' LDPL pin is not included in parity calculations '1' LDPL pin is included in parity calculations

d) Register 1202H: SONET/SDH Master Egress Configuration

ECONAT	'0' Telecom Drop Bus runs in AU3 (STS-1) mode.
LAOP	'0' Expect even parity generated on add bus '1' Expect odd parity generated on add bus
INCLAC1J1VI	'0' LAC1J1V1 pin is not included in parity calculations '1' LAC1J1V1 pin is included in parity calculations
INCLAPL	'0' LAPL pin is not included in parity calculations '1' LAPL pin is included in parity calculations
LAJ1EN	'0' LAC1J1V1 output indicates the C1 byte and optionally the third byte after J1 if LAVJ1EN is set high. '1' LAC1J1V1 output indicates the C1, J1 and optionally the third byte after J1
LOCK0	'0' J1 byte is forced to the byte immediately following C1 bytes (pointer offset 522) '1' J1 byte is forced to byte immediately following the H3 bytes (pointer offset 0)

e) Register 1209H: SONET/SDH Master DS3 Clock Generation Control

FASTCLKFREQ	'0' CLK52M frequency is 44.928MHz '1' CLK52M frequency is 51.84MHz Must match the setting for FASTCLKFREQ in the SBI Master Configuration Register if using SBI backplane.

f) Register 1604H: Drop Side Mapper Register

AISGEN	'0' Normal operation '1' Configures TEMUX/TEMAP to generate a DS3 AIS signal in the Ingress Data Stream.

g) Register 1644H: Add Side Mapper Register

AISGEN	'0' Normal operation '1' Configures TEMUX/TEMAP to generate a DS3 AIS signal in the Egress Data Stream.
RBSO	'0'' R bits in DS3 frame set to zero '1' R bits in DS3 frame set to one

18 SONET/SDH Loopback (Not Supported for TECT3)

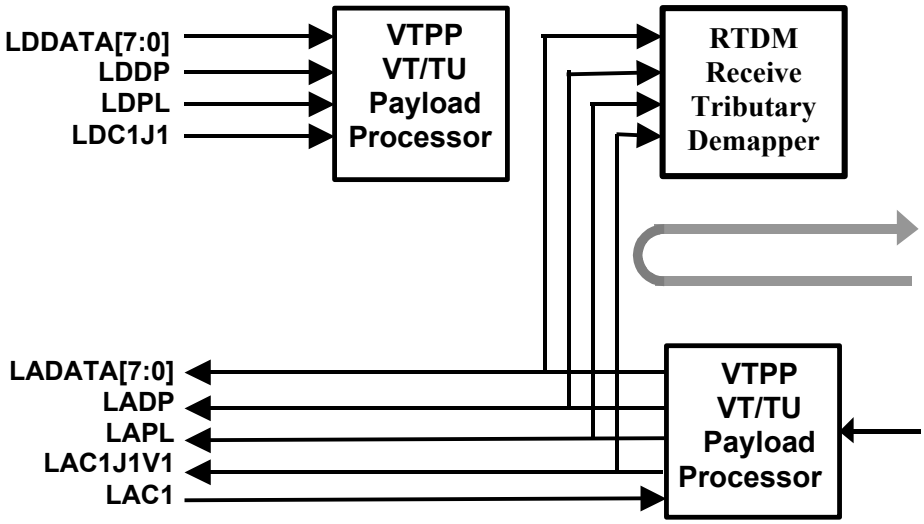
The TEMUX/TEMAP provides two loopbacks at the Telecom bus interface to aid in network and system diagnostics at the SONET/SDH interface. These loopback modes can be enabled via the microprocessor whenever the SONET/SDH block is enabled as the mapper for the T1/E1 framer slices or as the mapper for the DS3 framer or M13 Multiplexer.

SONET/SDH mode is not supported for the TECT3. This entire section does not apply to the TECT3.

18.1 Telecom Diagnostic Loopback

The Telecom Bus Diagnostic Loopback allows the transmitted Telecom bus stream to be looped back into the receive SONET/SDH receive path, overriding the data stream received on the Telecom drop bus inputs. While Telecom diagnostic loopback is active, valid SONET/SDH data continues to be transmitted on the Telecom add bus outputs. The entire Telecom drop bus is overwritten by the diagnostic loopback even though only one STS-1 SPE, STM-1/VC4 TUG3 or STM-1/VC3 is generated by the egress VTPP onto the Telecom add bus. This loopback is only available for VT1.5/VT2/TU11/TU12 mapped tributaries. DS3 mapped tributaries must use the DS3 diagnostic loopback. The Telecom bus diagnostic loopback mode is shown diagrammatically in Figure 39.

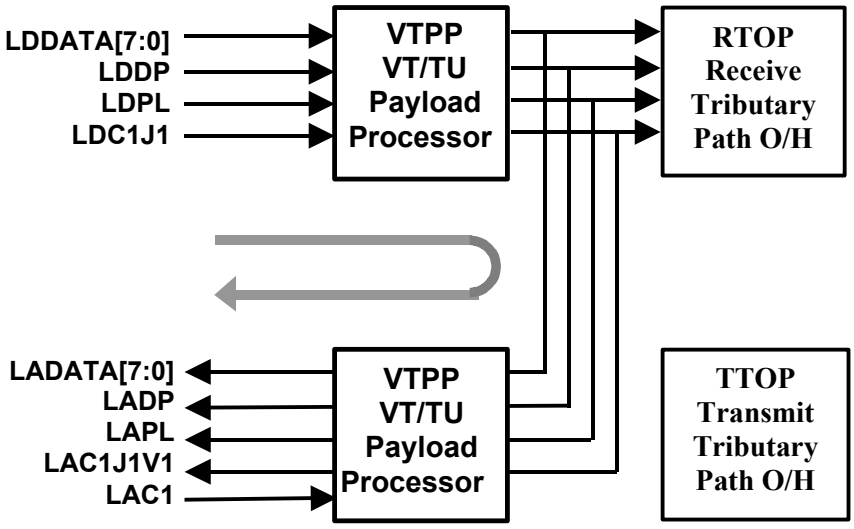
Figure 39 Telecom Diagnostic Loopback Diagram



18.2 Telecom Line Loopback

The Telecom Bus Line Loopback allows the received Telecom drop bus data to be looped back out the Telecom add bus after being processed by both the ingress and egress VTPPs. Both VTPP must be setup for the same STS-1 SPE, STM-1/VC4 TUG3 or STM-1/VC3 otherwise no loopback data will get through. The ingress data path is not affected by the Telecom line loopback. This loopback is only available for VT1.5/VT2/TU11/TU12 mapped tributaries. DS3 mapped tributaries must use the DS3 line loopback. The Telecom bus line loopback mode is shown diagrammatically in Figure 40.

Figure 40 Telecom Line Loopback Diagram



a) Register 120AH: SONET/SDH Master Loopback Control

LLOOP	Telecom Line Loopback '0' Normal operation '1' Ingress STS-1 SPE, STM-1/VC-4 TUG-3 or STM-1/VC3 is looped back onto egress Telecom bus
DLOOP	Diagnostic Telecom Loopback '0' Normal operation '1' Entire STS-3 /STM-1 data is looped back to the ingress data path.

Notes