TDK SEMICONDUCTOR CORP.

78A207
MFR1 Receiver

April 2000

DESCRIPTION

The 78A207 is a single-chip, Multi-Frequency (MF) receiver that can detect all 15 tone-pairs, including ST and KP framing tones. This receiver is intended for use in equal access applications and thus meets both Bell and CCITT R1 central office register signaling specifications.

The 78A207 employs state-of-the-art switched capacitor filters in CMOS technology. The receiver consists of a bank of channel-separation bandpass filters followed by zero-crossing detectors and frequency-measurement bandpass filters, an amplitude check circuit, a timer and decoder circuit, and a clock generator. The device does not attempt to identify strings of digits by the KP (key pulse) and ST (stop) tone pairs.

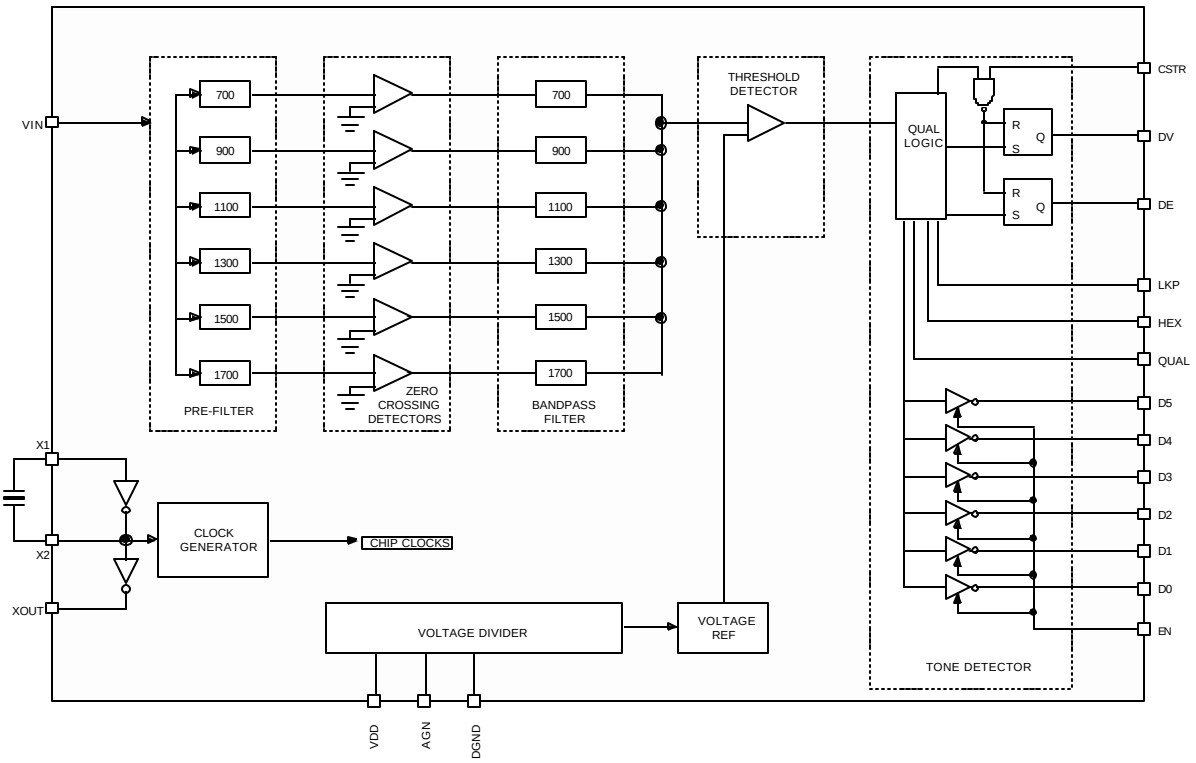
No anti-alias filtering is needed if the input signal is band-limited to 26 KHz. The only external component required is an inexpensive television "color burst" 3.58 MHz crystal.

The outputs interface directly with standard CMOS or TTL circuitry and are three-state enabled to facilitate bus-oriented architecture.

FEATURES

- **Meets Bell and CCITT R1 specifications**
- **20-pin plastic DIP**
- **Single low-tolerance 5V supply**
- **Detects all 15 tone-pairs including ST and KP**
- **Long KP capability**
- **Built-in amplitude discrimination**
- **Excellent noise tolerance**
- **Outputs in either "n of 6" or hexadecimal code**
- **Three-state outputs, CMOS-compatible and TTL-compatible**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

VIN

This pin accepts the analog input. It is internally biased to half the supply and is capacitively coupled to the channel separation filters. The input may be DC coupled as long as it does not exceed VDD or drop below GND. Equivalent input circuit is shown below in Figure 1.

CRYSTAL OSCILLATOR

The 78A207 contains an on-board inverter with sufficient gain to provide oscillation when connected to a low cost television “color-burst” crystal. The on-chip clock signals are generated from the oscillator. The crystal is connected between X1 and X2.

XOUT is a 3.58 MHz square wave capable of driving other circuits as long as the capacitive load does not exceed 50 pF. Other devices driven by XOUT should use X1 as the input pin, while X2 should be left floating.

LKP

The KP timer control: When high, the KP detect time is increased. When low, the KP detect time is the same as for other tones.

QUAL

Enables tone pair qualification. When low, the threshold detector outputs are passed to the data outputs (D0-D5) without validation in the format selected by the HEX pin. These outputs, plus strobes DV and DE, are updated once per 2.3 ms frame. Note that the strobes will cycle once per frame (even when the inputs are stable.) As always, data changes only when both strobes are low.

$\overline{\text{CSTR}}$

This input clears both the DV and DE strobes, and is active low. After $\overline{\text{CSTR}}$ is released, the strobes will remain low until a new detect (or error) occurs. The output data is latched by $\overline{\text{CSTR}}$ and will not change while $\overline{\text{CSTR}}$ is low, even in the event that a new detect is qualified internally. (Note that improper use of $\overline{\text{CSTR}}$ may result in missed detects.)

$\overline{\text{EN}}$

The three-state enable control: When low, the D0-D5 outputs are in the low impedance state. In an interrupt oriented microprocessor interface, $\overline{\text{EN}}$ and $\overline{\text{CSTR}}$ will often be tied together to provide automatic reset of the strobes when the output data is enabled.

STROBE PINS - DV AND DE

Valid data is indicated on the DV strobe pin, and data errors are indicated on the DE strobe pin. Whenever a valid 2 of 6 code has been detected, the DV strobe rises. It remains high until the code goes away, or the $\overline{\text{CSTR}}$ line is activated. When an invalid code is detected, e.g., 1 of 6, 3 of 6, etc., the DE strobe remains high until all errors stop, a valid tone pair is detected, or the $\overline{\text{CSTR}}$ line is activated. Once cleared by $\overline{\text{CSTR}}$, DE will not reactivate until a new invalid condition is detected. The DE and DV strobes will never be high simultaneously.

DATA OUTPUT MODES

The digital output format may be either “n of 6” or 4-bit hexadecimal.

For “hex” mode, the HEX pin is pulled high. Outputs D0 to D3 provide a 4-bit code identifying one of the 15 valid tone combinations according to Table1.

The outputs will be cleared to zero when no valid tone pair is present.

For the “n of 6” mode, the HEX pin is pulled low, and each output represents one of the six frequencies as shown below:

FREQUENCY	OUTPUT PIN
700	D0
900	D1
1100	D2
1300	D3
1500	D4
1700	D5

The outputs will be cleared to zero when no valid tone is present.

TABLE 1:

Channels	Tone Pair Freq.	Name	D3	D2	D1	D0
0-1	700, 900	1	0	0	0	1
0-2	700, 1100	2	0	0	1	0
1-2	900, 1100	3	0	0	1	1
0-3	700, 1300	4	0	1	0	0
1-3	900, 1300	5	0	1	0	1
2-3	1100, 1300	6	0	1	1	0
0-4	700, 1500	7	0	1	1	1
1-4	900, 1500	8	1	0	0	0
2-4	1100, 1500	9	1	0	0	1
3-4	1300, 1500	0	1	0	1	0
2-5	1100, 1700	KP	1	0	1	1
4-5	1500, 1700	ST	1	1	0	0
1-5	900, 1700	ST1	1	1	0	1
3-5	1300, 1700	ST2	1	1	1	0
0-5	700, 1700	ST3	1	1	1	1
	any other signal		0	0	0	0
NOTE: In the hex mode, D4 = DE and D5 = DV.						

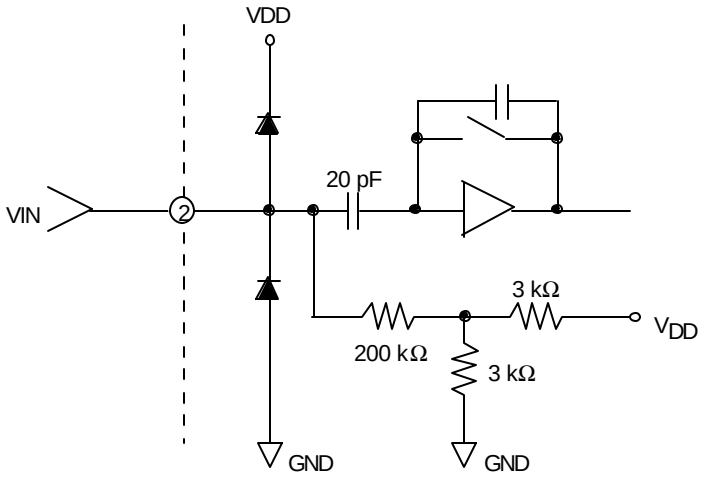


FIGURE 1: VIN Equivalent Input Circuit

TIMING SPECIFICATIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Ton	Tone Time, KP (LKP = VDD)	detect	55			ms
Ton		reject			30	ms
Ton	Tone Time, KP (LKP = DGND)	detect	30			ms
Ton		reject			10	ms
Ton	Tone Time, All Others	detect	30			ms
Ton		reject			10	ms
Tpse	Pause Time	detect	20			ms
Tbr		reject			10	ms
Tsu	Data Setup Time		6			µs
Th	Data Hold Time		7			µs
Tskew	Tone Skew Tolerance				4	ms
Tstr	Minimum Strobe Pulse Width					
	QUAL High		20			ms
	QUAL Low		2			ms
Tsep	Minimum Strobe Separation					
	QUAL High		20			ms
	QUAL Low		2			ms
Tr	Rise Time DV, DE, D0-D5 10-90%	CL = 20 pF			100	ns
Tf	Fall Time DV, DE, D0-D5 10-90%	CL = 20 pF			100	ns
Tw	$\overline{\text{CSTR}}$ Width		50			ns
Ten	Data Enable Time	CL = 20 pF			100	ns
Tdis	Data Disable Time				100	ns
Trst	Strobe Reset Time	CL = 20 pF			100	ns

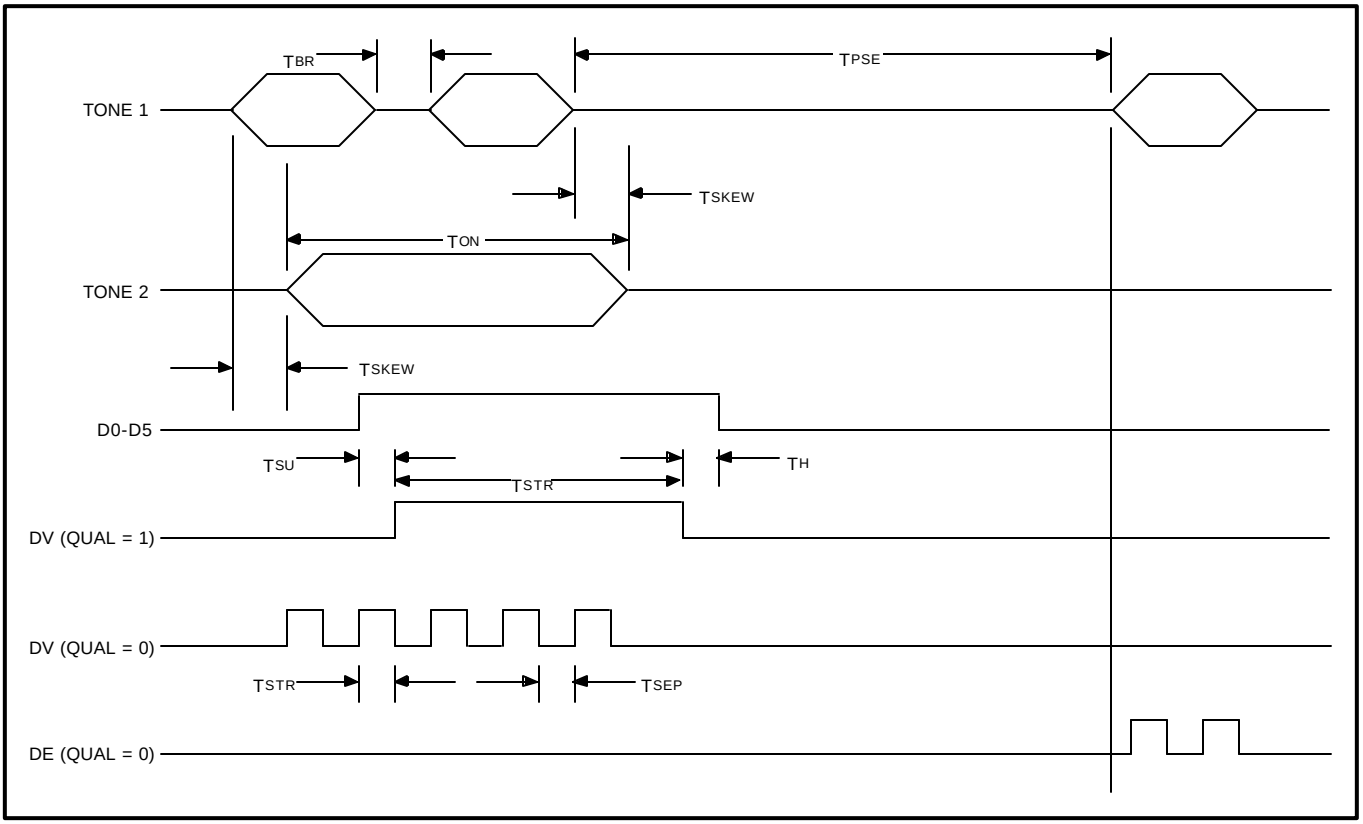


FIGURE 2: 78A207 Timing Diagram

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Operating above absolute maximum ratings may damage the device.)

PARAMETER	RATING
DC Supply Voltage V_{DD}	+ 7V
Operating Temperature	0 to 70 (Ambient)°C
Storage Temperature	65 to 150°C
Power Dissipation (25°C) (Derate above TA=25°C @ 6.25 mW/°C)	650mW
Input Voltage	(V_{DD} + 0.3V) to -0.3V
DC Current into any input	±10mA
Lead Temperature (Soldering, 10 sec.)	300°C

DC ELECTRICAL CHARACTERISTICS (0°C ≤ TA ≤ 70°C, VDD = 5V ± 10%)

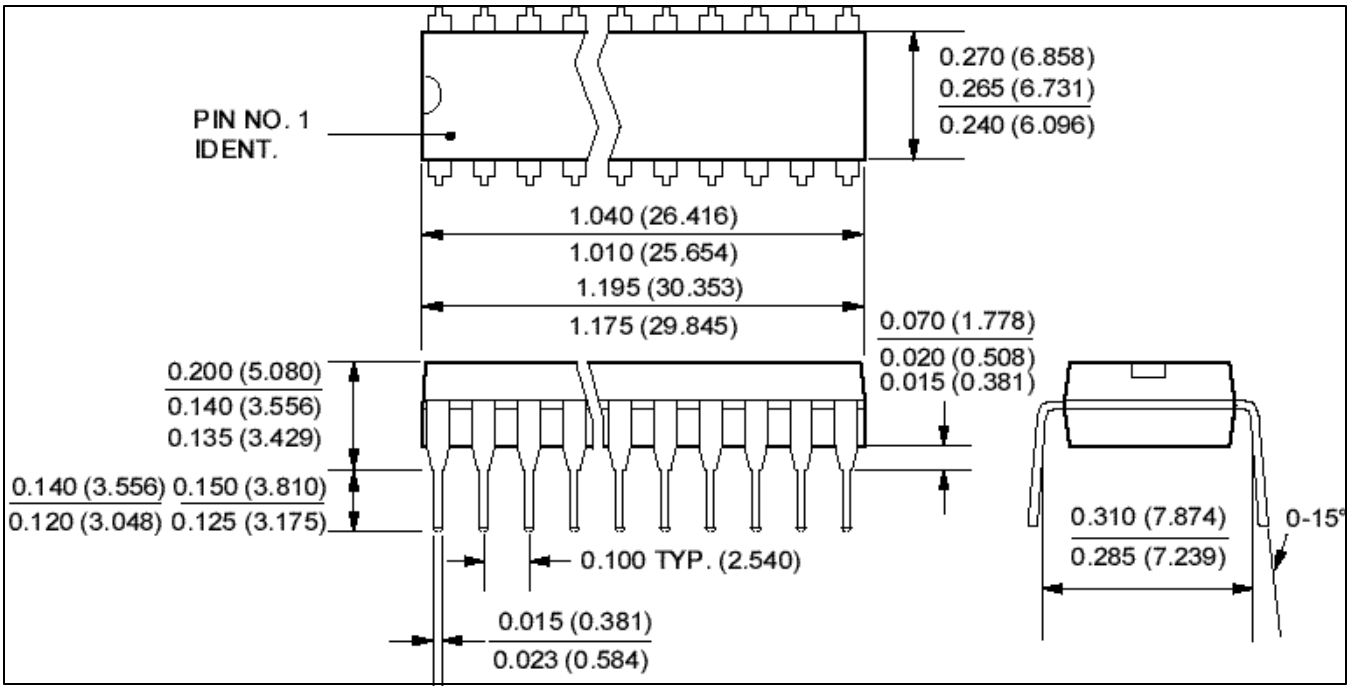
PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Idd	Supply Current				20	mA
Vol	Output Logic 0					
	Iol = 8 mA				0.5	V
	Iol = 1 mA				0.4	V
Voh	Output Logic 1					
	Ioh = -4 mA		VDD-1.0			V
	Ioh = -1 mA		VDD-0.5			V
Vih	Input Logic 1		2.0			V
Voh	Input logic 0				0.8	V
Zin	Analog Input Impedance (Input between VDD and AGND)		$\frac{100K}{30pF}$			Ω
Lin	Digital Input Current (Input between VDD and DGND)		-50		50	µA

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°, VDD = 5V ± 10%)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
F	Frequency for Detect Tolerance		±(0.015 xFo + 5)			Hz
A	Amplitude for Detect	each tone	-25		0	dBm
			0.123		2.191	Vpp
AN	Amplitude for no Detect				-35	dB
					0.039	Vpp
TW	Twist Tolerance	$TW=\frac{high\ tone}{low\ tone}$	-6		+6	dB
T3	Third MF Tone Reject Amp	relative to highest Amplitude tone	-15			dB
N60	60 HZ Tolerance	not more than one error in 2500 10-digit calls	81			dBm
			0.777			Vpp
N180	180 HZ Tolerance	same as above	68			dBm
			0.174			Vpp
Nn	Noise Tolerance[1]	same as above			-20	dB
NI	Impulse Noise Tolerance[2]	same as above			+12	dB

NOTES: 1. C-message weighted. Measured with respect to highest amplitude tone.
2. With noise tape 201 per PUB 56201. Measured with respect to highest aplitude tone.

MECHANICAL SPECIFICATIONS

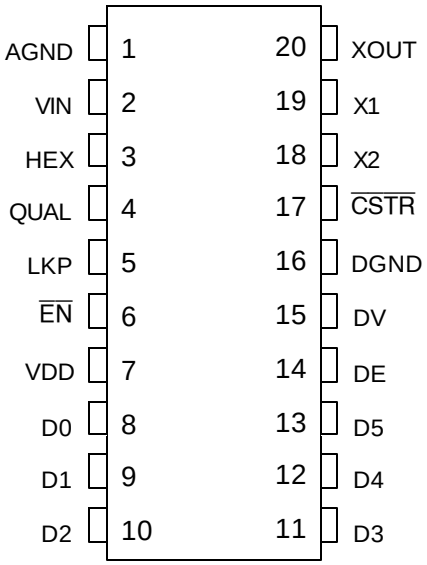


20-Pin DIP

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



20-Pin DIP
78A207

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGING MARK
78A207 20-Pin Plastic DIP	78A207-CP	78A207-CP

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