DSLAM

DSLAM REFERENCE DESIGN: CORE CARD

RELEASED

Issue 4

December 2000

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REVISION HISTORY

Issue No.	Issue Date	Details of Change
4	December 2000	Replaced “metadriver” with “VORTEX Chipset Driver” for consistency with software driver documents. Updated LVDS hot swap explanation and cell transfer, which may be affected by setting OCAEN bit in register 0x0A of the S/UNI-DUPLEX. Register write sequence is required to enable OCAEN at the very end of the chipset activation. The sequence is already implemented with the VORTEX Chipset Driver on CD-ROM Ver 3.0.
3	September 2000	Document rewritten and updated for Issue 3. Updated schematics Issue 3. Included PCB layer plots. Added test results from FTP on Core Card Issue 3. Updated BOM. Added appendix with software example.
2	December 1999	Paper design errata-document. This Reference Design Issue 2 has no Core Card PCB manufactured.
1	August 1999	First Issue. Core Card Issue 1 build.

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1. OVERVIEW

The purpose of the Reference Design document set is to assist engineers in designing their products using the PMC-Sierra VORTEX chipset.

The DSLAM Reference Design is composed of these four main documents:

- DSLAM Reference Design: System Design
- DSLAM Reference Design: Core Card
- DSLAM Reference Design: WAN Card
- DSLAM Reference Design: Line Card

The *DSLAM Reference Design: System Design* document provides an overview of the DSLAM Reference Design system architecture. The remaining documents describe the functionality and implementation specific details for each individual card.

This document specifically describes the design for the DSLAM Core Card. A block diagram illustrates the Core Card design. A description is then given for the functional blocks of the design. A detailed implementation description then follows. The appendixes contains additional information, such as, schematics, bill of material, and CPLD VHDL source.

2. DSLAM CORE CARD FEATURES

The Digital Subscriber Line Access Multiplexer (DSLAM) Core Card features:

- ATM traffic policing and traffic shaping
- Small-scale traffic management (switching) with the S/UNI-APEX
- A high-speed Low Voltage Differential Signal (LVDS) interface that:
    - Provides data rates up to 200Mb/s
    - Allows manual selection of transmission over a backplane or through cables.
    - Supports one-to-one (1:1) protection switching
- Support for clock synchronization to either the DS-3 network or the line side interface
- Front panel LEDs to indicate:
    - Power supply status
    - LVDS signal status
- On-board hot swap controller to monitor the current flow onto the board for live insertion and extraction
- Compact PCI (cPCI) compatibility

3. TYPICAL DSLAM APPLICATION WITH CORE CARD

Figure 1 shows a typical application for the S/UNI-DUPLEX, S/UNI-VORTEX, S/UNI-APEX, and the S/UNI-ATLAS.

Figure 1. DSLAM Reference Design Shelf Architecture

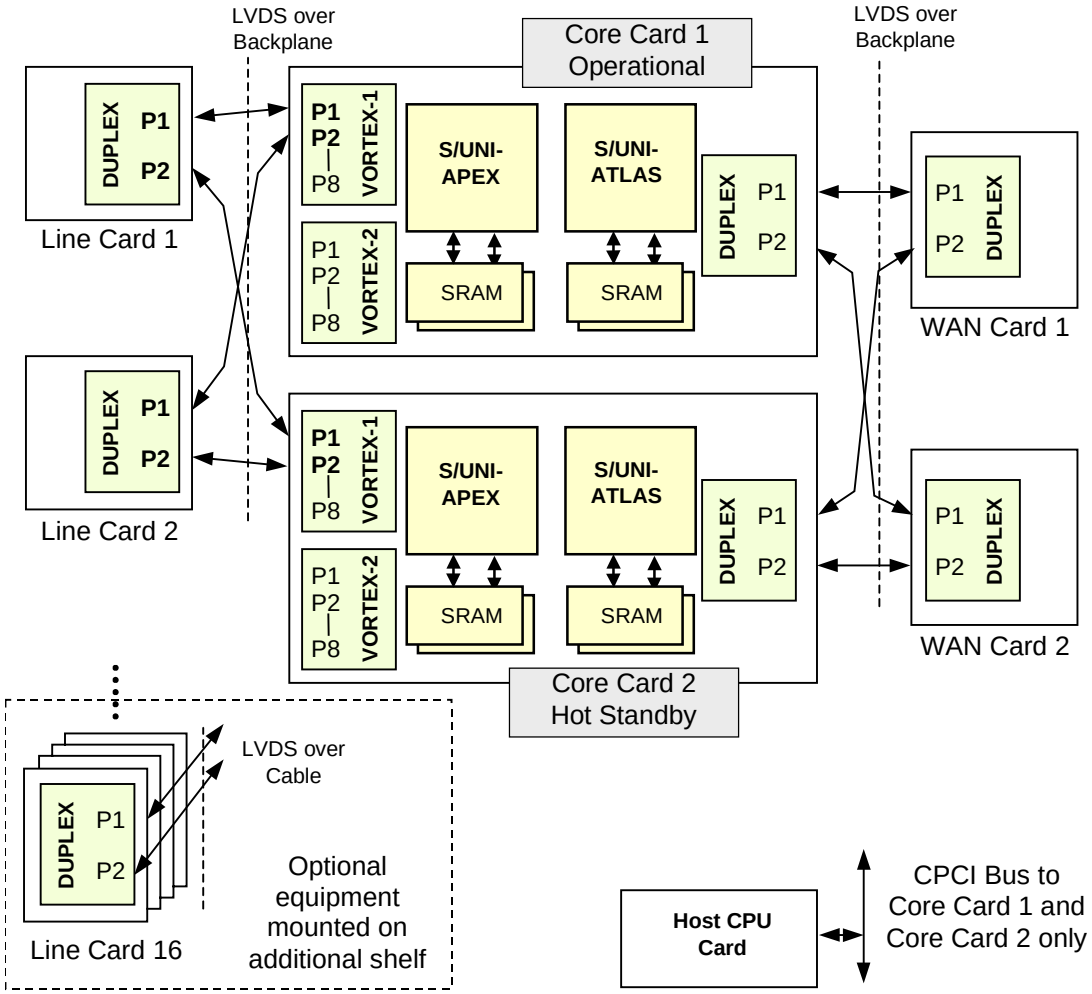


Figure 1 shows two Core Cards in protective mode. The lower card is the hot stand-bycard that allows one-to-one backup for the operating Core Card.

Also, this block diagram shows a DSLAM development shelf that is equipped with a custom LVDS-backplane, two Line Cards, two WAN Cards, and two Core Cards. A single host CPU card controls Core Cards only. Additional Line Cards can be mounted on a separate shelf with LVDS over cables. Line Cards and WAN Cards, built for the DSLAM Reference Design, have an embedded microprocessor without communication to the cPCI bus.

3.1. Compact PCI (cPCI) Development Shelf

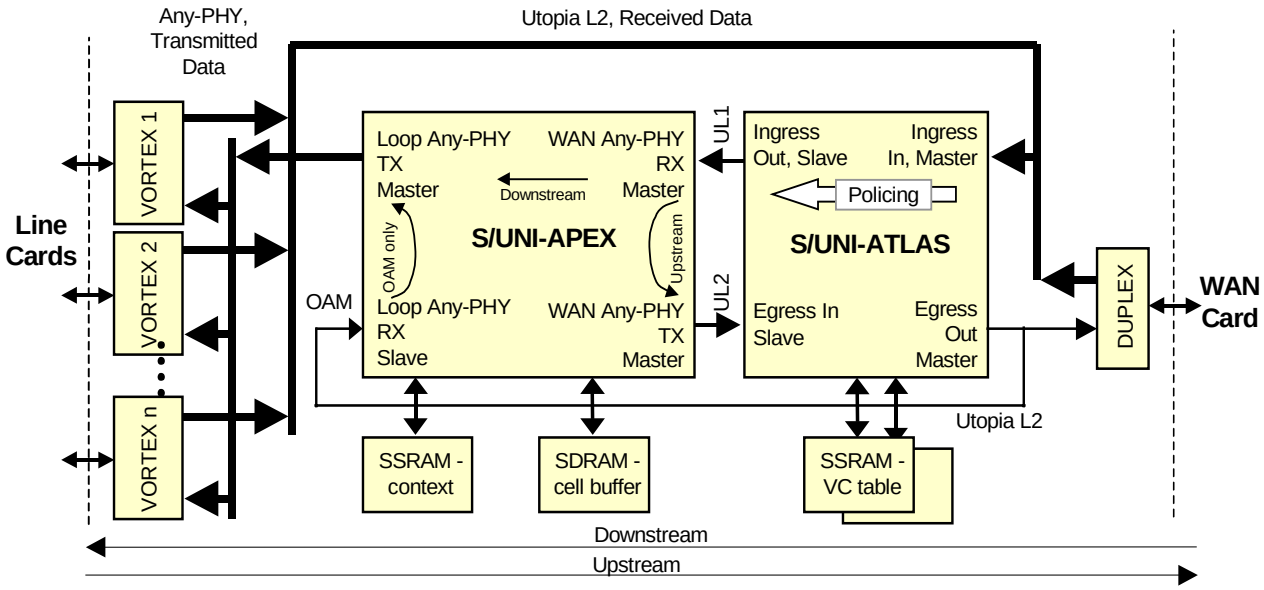
The DSLAM Reference Design for the Core Card is based on a cPCI shelf allowing standardization of interfaces and physical card forms. A custom-made LVDS-backplane is developed demonstrating the LVDS interface functioning over the backplane. LVDS can also be connected with cables through the front plate connectors. The shelf-to-shelf LVDS is implemented using the front plate connectors exclusively. Two Core Cards are used to provide a hot stand-by, as required by the Telcos.

The basic DSLAM development shelf is an 8-slot entity. A 16-slot shelf can be also supported with a single Reference Design Core Card (with an optional hot stand-by card for protection switching).

3.2. DSLAM Reference Design Core Card Architecture

Figure 2 shows the DSLAM Reference Design and Core Card Reference Design that is built around a single S/UNI-ATLAS architecture.

Figure 2. The Core Card Architecture



The S/UNI-APEX and S/UNI-ATLAS are the core of the design. The downstream and upstream cells are interfaced to the S/UNI-ATLAS through the same *Ingress In, Master*port. The *Loop Any-PHY RX, Slave* port on the S/UNI-APEX is connected to WAN direction *Egress Out, Master* allowing OAM cell flow (RDI from the S/UNI-ATLAS towards downstream). The S/UNI-APEX switches cells to *Loop Any-PHY TX, Master* or to *WAN Any-PHY TX, Master* ports as required per

cell destination. The Core Card interface to the Line Cards is through a set of S/UNI-VORTEX devices. The Core Card interface to the network is through the S/UNI-DUPLEX, which provides an LVDS link to the WAN Card.

In the upstream direction, the S/UNI-ATLAS takes cells from the Line Cards and performs a look-up, based on the PHY number, VPI, and VCI that are used to identify the associated connection. Once the connection is identified, the cell is processed according to the configuration of the connection. In this application, the S/UNI-ATLAS performs the header translation, per-PHY and per-VC policing, performance monitoring, and fault management. Prepend and postpend are used to navigate the cell.

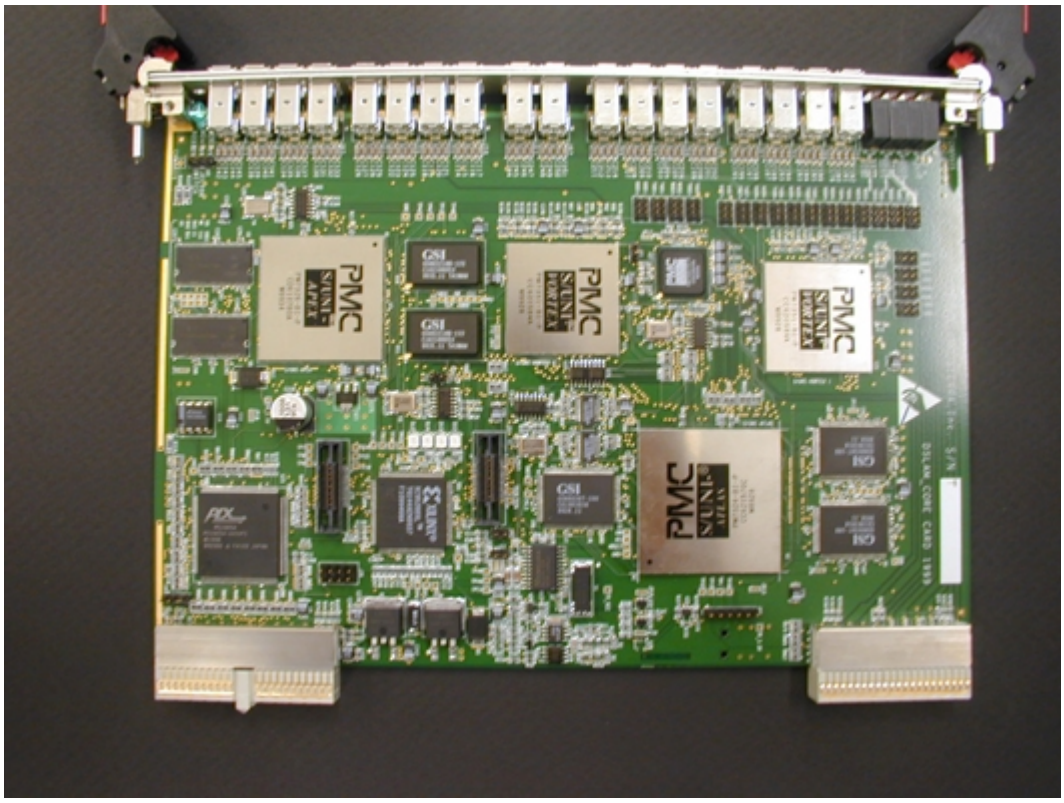
In the downstream direction, the S/UNI-ATLAS accepts the cells coming from a WAN Card and a direct look-up is performed to identify the connection. The cell is then processed according to the configuration in the context table for that connection (cell is tagged). The header translation and OAM processing can be done at the ingress. The tagged cell is sent to the S/UNI-APEX *WAN Any-PHY RX, Master* port. The S/UNI-APEX puts the cell into a queue and sends it to either *Loop Any-PHY TX, Master* or *WAN Any-PHY TX, Master* ports. The tag determines the port. If the cell destination is loop side, then the cell goes through the *Loop Any-PHY TX, Master* port to one of the S/UNI-VORTEX multiplexers, where the destination channel matches the tag number. The cell is passed to one of 32 queues for transmission by the appropriate PHY.

The AIS cell coming from the loop (upstream) arrives at the S/UNI-ATLAS *Ingress In* port. The S/UNI-ATLAS generates the RDI cell with the tag that corresponds to the port where the AIS cell arrived. The RDI cell is sent to the *Egress Out* port and then arrives at the S/UNI-APEX slave port, *Loop Any_PHY RX*, only if the tag matches the loop side destination. The S/UNI-APEX puts the RDI cell into a queue and sends the cell through the *Loop Any-PHY TX, Master* port to one of the S/UNI-VORTEX multiplexers, where the destination channel matches the tag number.

The network management entity has to assign unique port (channel) numbers to all S/UNI-DUPLEX and S/UNI-VORTEX devices attached to the Utopia L2 bus.

The Core Card picture is shown in Figure 3 below.

Figure 3. Core Card Top View



4. CORE CARD FUNCTIONAL EXPLANATION

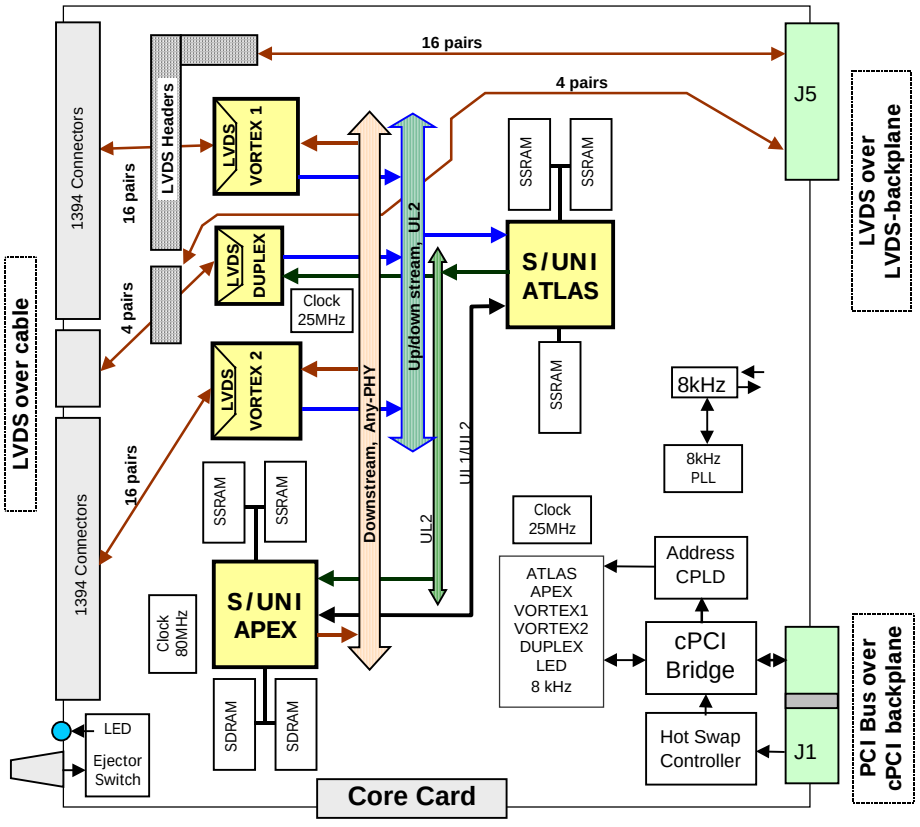
4.1. Core Card Block Diagram

This section briefly describes the Core Card block diagram.

4.1.1. Block Diagram Drawing

Figure 4 shows the Core Card layout block diagram.

Figure 4. Core Card Block Diagram



The block diagram shows the PMC Sierra chipset associating with RAMs, clocks, PCI bridge, and CPLD. LVDS connectors at the front and at the back of the Core Card allow an interface to the high-speed LVDS signals (up to 200 Mbps). The PCI bus and power (+5 V and +3.3 V) are connected through J1. A system synchronization 8 kHz clock (stratum clock) can be interfaced at the internal headers.

4.1.2. VORTEX Chipset

Five chips shown in the block diagram above create a single entity called *VORTEX chipset*, including the S/UNI-ATLAS, S/UNI-APEX, S/UNI-DUPLEX, and S/UNI-VORTEX. The VORTEX chipset, and Core Card as well, provides ATM traffic policing (S/UNI-ATLAS), ATM cell traffic management (S/UNI-APEX), and ATM cell multiplexing (S/UNI-VORTEX and S/UNI-DUPLEX).

In the downstream direction, the S/UNI-APEX sends data to the S/UNI-VORTEX and then to the Line Card(s) through the PMC-Sierra Any-PHY interface. The Any-PHY interface supports a bandwidth of up to 800 Mb/s and allows for 2048 channel addressing. The data format is an ATM cell with a prepended single address word.

On the user (loop) side, the Core Card provides an interface through the S/UNI-VORTEX-1 or S/UNI-VORTEX-2 to the Line Cards. On the network side, the Core Card provides an interface through a S/UNI-DUPLEX to the WAN Card. Both interfaces are LVDS type with data transfer rates up to 200 Mb/s.

The S/UNI-ATLAS provides traffic policing and OAM functionality. A single entry port to the S/UNI-ATLAS of both upstream and downstream cells (specific to this Reference Design) provides easy traffic policing - the S/UNI-ATLAS implements that function in the Ingress direction only.

The VORTEX chipset is described in more details later in this document.

4.1.3. LVDS Interface

The Core Card provides an interface for the LVDS from the front plate or from the LVDS-backplane. The LVDS interface at the front panel allows access to eight ports on the S/UNI-VORTEX-1, eight ports on the S/UNI-VORTEX-2, and two ports on the S/UNI-DUPLEX. LVDS over the backplane provides an interface to eight ports on the S/UNI-VORTEX-1 and two ports on the S/UNI-DUPLEX. Space limitations prevent all LVDS ports of the S/UNI-VORTEX-2 from being accessible at the back connector J5. The LVDS connectors were chosen to be an IEEE Firewire type that supports a data rate in excess of 200 Mb/s.

The LVDS drivers, receivers, copper traces, and connectors are designed to work in 50/100 ohm environment. Individual trace and driver is designed for 50 ohm characteristic impedance. The differential LVDS lines at the receiver inputs are loaded with external 100 ohm resistors.

More on LVDS can be found in sections 4.2, 9.2, 9.3 and 10 in this document.

4.1.4. PCI Bridge

The Core Card does not have an on-board microprocessor. The PCI bus host processor card provides an interface to the Core Card through a cPCI bridge device, which only uses a read/write (burst) register sequence and interrupt service. The cPCI bus does not carry payload data, which enables the host CPU to maintain all DSLAM cards through the cPCI bus without burden of ATM traffic over cPCI. If required, cells can be inserted into traffic through the cPCI interface.

The hot swap compatible PCI bridge (PLX PCI9054) is used as the PCI bus interface. The bridge operates in multiplexed mode on the local bus side. The PCI9054 provides an interface to a CPLD for address decoding (chip enable).

The local bus speed is set at 25 MHz, which allows the microprocessor interface on all devices to run at the optimum speed.

The PCI9054 requires a serial EEPROM (SEEP) to boot on power-up (or reset).

4.1.5. Hot Swap Controller

The hot swap controller LTC1645, and discrete components are used to make the Core Card hot swap compatible. This device is accompanied with the LTC1326 supply voltage monitor and reset line generator.

4.1.6. Ejector Handle and LED

The ejector handle has a built-in microswitch that toggles when the ejector changes position. The activity is detected by the cPCI bridge, which in turn notifies the host CPU about the status change. A blue LED signals the card's "not-ready-yet" status upon insertion or the card's readiness for removal. NOTE: This functionality requires specific software driver, which is not supported by the PMC-Sierra VORTEX Chipset Driver. Also, the host CPU card must have hardware provision to detect activities on the ENUM# line.

4.1.7. CPLD

A CMOS Programmable Logic Device (CPLD) is used to provide address decoding, LED latches, interrupt latches, and 8 kHz clock routing. The Xilinx XC95144 was chosen for this design.

The CPLD is in-circuit programmable through a header connector.

4.1.8. RAMs

The S/UNI-ATLAS and the S/UNI-APEX need fast RAMs to buffer large amounts of data.

The S/UNI-APEX needs both SDRAM and SSRAM. Both RAMs operate at 80 MHz. The Reference Design shows oversized RAMs due to chip availability and system verification purposes. The Core Card cell throughput can be supported with smaller RAM sizes. The cell buffer SDRAMs are at 16 MBytes in two integrated circuits. The context memory NBT (ZBT) SSRAM is shown as 4 MBytes that use two integrated circuits. Also, RAM size depends on availability of RAM chips at the time the Core Cards are assembled.

The S/UNI-ATLAS needs two sets of RAM for VC* look-up tables on Ingress and Egress directions. Those RAMs are SSRAMs working at 50 MHz. The Reference Design for S/UNI-ATLAS is supported with enough SRAM for 16 k connections at the Ingress and Egress. The Egress uses one 128 k x 36 SRAM (36-bit wide data bus). The Ingress uses one bank of two 128 k x 36 SRAMs to make up the 72 bit wide data bus. The S/UNI-ATLAS must interface with synchronous flow-through SRAMs (non-pipelined).

*/ VC – Virtual Connection. This refers either to Virtual Path Connection (VPC) or Virtual Channel Connection (VCC) within a physical link.

4.2. DSLAM High-Speed LVDS Serial Interface

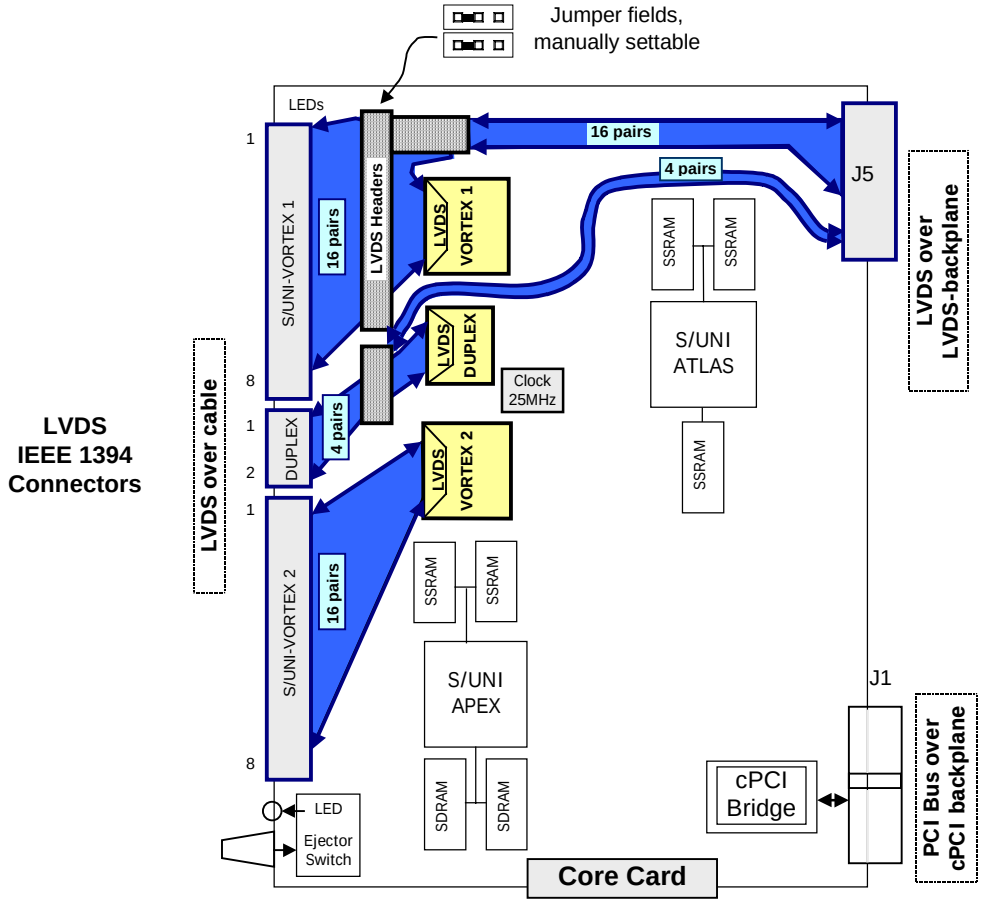
The S/UNI-DUPLEX and S/UNI-VORTEX provide backplane interconnection through 100 to 200 Mb/s serial LVDS links. All cells flown to and from Core Card, and cells processed on the Core Card are concentrated on these high-speed links. Clock is not transmitted to avoid clock skew issues, and the receiver recovers the clock from the incoming data.

For more information on the high-speed LVDS link, see DSLAM system design document [1].

4.2.1. Example of LVDS Routing on Core Card

The Core Card provides an LVDS interface to both the LVDS-backplane and to the front panel. Block diagram, shown in Figure 5, highlights components that support LVDS on the Core Card.

Figure 5. LVDS on Core Card



Manually settable header fields are used to direct LVDS flow. The setup must be done before the card is inserted into the DSLAM shelf.

S/UNI-VORTEX-1 and the S/UNI-DUPLEX can provide an interface to J5 or to the front panel. S/UNI-VORTEX-2 provides an interface to the front panel only. The total number of LVDS traces to J5 (and running on the LVDS-backplane) is 40. This large number of high-speed connections may create crosstalk on the cPCI connector. Separating “hot” lines with ground pins can minimize this crosstalk.

The LVDS traces to the front plate connectors are relatively long. Care must be taken to avoid crosstalk to/from digital lines. The front panel connectors are the FireWire type (IEEE 1394), designed to handle differential signals up to 400Mb/s. Other low cost solutions, such as UTP-5 RJ-45 type connectors, are physically too wide to support eighteen ports.

4.2.2. LVDS Transmitters vs. Hot Swap

The LVDS interface is fully hot swap compatible. The LVDS transmitters can stay active or can be turn off (disabled) on live cards, while another card is hot plugged in. For example, the transmitter disable function is executed on the S/UNI-DUPLEX by writing register 0x05 with value 0x30. The S/UNI-VORTEX registers 0x095, 0x0B5, 0x0D5, 0x0F5, 0x115, 0x135, 0x155 and 0x175 disable LVDS transmitter per HSS link by writing 0x08. After inserted card is operable, writing *zero* to appropriate bits in corresponding registers can activate the transmitters.

IMPORTANT: Proper register write sequence is required to ensure cell transfer over the LVDS interface and Utopia bus. The sequence is implemented in the VORTEX Chipset driver files vcs_api1.c and dpx.c. It is important to make sure the S/UNI-DUPLEX OCAEN bit in register 0x0A stays disabled until S/UNI-ATLAS polling is enabled. The OCAEN is set to 1 at the very last write, enabling cell transfer from the S/UNI-DUPLEX at that interface. The above sequence applies to the card that is initialized after power up and also to any card that has interface setup changed. Software designers are required to observe sequencing in their drivers.

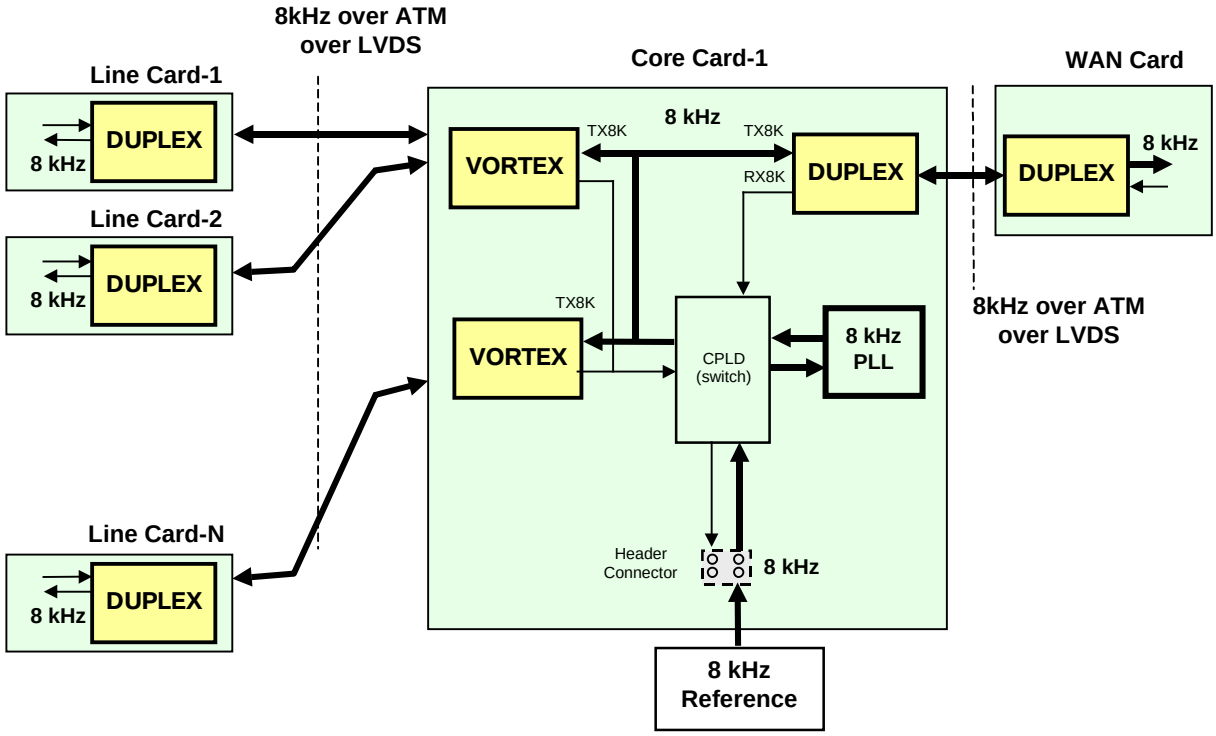
More on LVDS can be found in sections 9.2, 9.3 and 10 in this document.

4.3. 8kHz Interface

The S/UNI-DUPLEX and the S/UNI-VORTEX provide a mechanism for transporting an 8 kHz time stamp over the LVDS connection. This 8 kHz signal is

used to synchronize the whole network with a single reference clock. Figure 6 shows an example of the 8 kHz DSLAM network synchronization.

Figure 6. Example of 8kHz Clock Flow on Core Card



The 8 kHz signal is entered and received to/from the S/UNI-VORTEX or S/UNI-DUPLEX at the dedicated pins TX8K or RX8K. The time reference is encoded in the third byte of the prepend attached to a modified ATM cell transmitted over the serial high-speed LVDS connection.

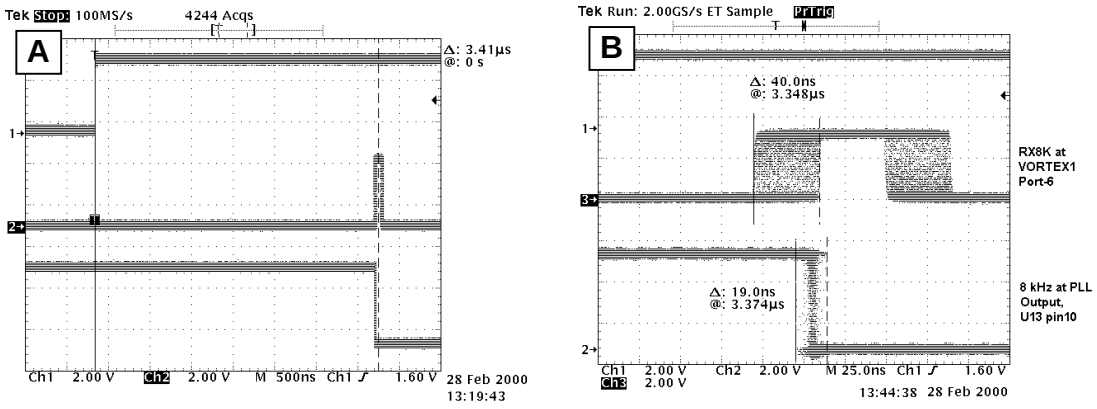
A brief description of the circuit is as follows. The 8 kHz clock can be fed to the system at different points – through the Core Card, WAN Card, or Line Cards. The highlighted flow shows 8 kHz distributed from the Core Card. The 8 kHz time stamp is encoded in cells sent by the S/UNI-VORTEX and S/UNI-DUPLEX on the Core Card and then to the S/UNI-DUPLEX on the Line Card and WAN Card. The WAN Card filters out encoding jitter through the 8 kHz PLL, before it is used for further synchronization. The DSLAM Reference Design Line Card can derive 8 kHz time stamp and feed into the Comets. The Comet has an internal 8 kHz dejittering circuit; therefore, cards have no additional 8 kHz PLL.

The Core Card 8 kHz path is controlled through the cPCI bridge and a CPLD.

The received 8 kHz clock on the S/UNI-VORTEX / S/UNI-DUPLEX pin RX8K is a pulse that lasts 16 clock cycles on the clock at the LVDS connection. If LVDS is at 200 MHz, then the pulse is 16 x 5 ns = 80 ns long and repeats at 125 us (8 kHz).

Figure 7 shows an example of an oscilloscope captured time reference that has been recovered on the Core Card.

Figure 7. Example of Received 8 kHz Time Reference



Graph A shows the edge of the 8 kHz reference clock inserted to the S/UNI-VORTEX, received time reference pulse at the S/UNI-DUPLEX RX8K output pin, and resynchronized 8 kHz clock at the PLL output.
Graph B shows jitter on the received time reference pulse and edge of the 8 kHz square wave at the PLL output. Attenuated edge jitter is approximately 19 ns, which can be converted to approximately 0.00015 UI peak-to-peak.

For more information about the DSLAM 8 kHz clock distribution, see the DSLAM system design document [1].

Protection switching, executed in our lab, showed no adverse affect on the 8 kHz clock phase and frequency synchronization. For more information about network synchronization and phase-frequency shift, see the DSLAM system design document [1] and also in [9], [16], and [17].

5. CORE CARD CHIPSET OVERVIEW

This section briefly describes the DSLAM chipset.

5.1. PM7324 S/UNI-ATLAS

The S/UNI-ATLAS is the PMC-Sierra standard product that implements the following ATM Layer functions:

- OAM processing, according to the ITU-T I.610 1995 and 1998 living list.
- Header Translation on full VPI/VCI address range.
- Prepend and postpend tagging.
- Cell rate policing according to ITU-T I.371 using the Generic Cell Rate Algorithm.
- GFR Policing according to ATM Forum's Traffic Management 4.0 1998 living list.
- Per-PHY queuing to prevent head-of-line blocking.

The S/UNI-ATLAS performs both ingress and egress functionality. The ingress side has a SCI-PHY level 2 (Utopia L2) interface at the input, and a SCI-PHY level 1 (Utopia L1) interface at the output. Cells coming into the S/UNI-ATLAS from a PHY are identified according to the PHY ID, VPI, and VCI using a binary search process. The cells are processed according to the information stored in context RAM for the particular connection. Cells may also be copied to the microprocessor cell interface for external processing.

The egress port has a SCI-PHY level 2 interface at both the input and output interface. The connection is identified (using a direct lookup process) by the PHY ID, VPI, and VCI, and processed according to the information in external RAM for the particular connection. Like the ingress port, cells can be copied to the microprocessor cell interface for external processing. The software, VORTEX Chipset Driver that controls the Reference Design Core Card, sets the cell header remapping in the S/UNI-ATLAS. The S/UNI-ATLAS is configured and controlled through a generic 16-bit asynchronous microprocessor bus.

The S/UNI-ATLAS is implemented in low power 3.3 Volt CMOS technology. The microprocessor and JTAG interfaces are 5 Volt/ 3.3 Volt tolerant, while all other interfaces are 3.3 Volt only. The S/UNI-ATLAS is packaged in a 432-pin SBGA package.

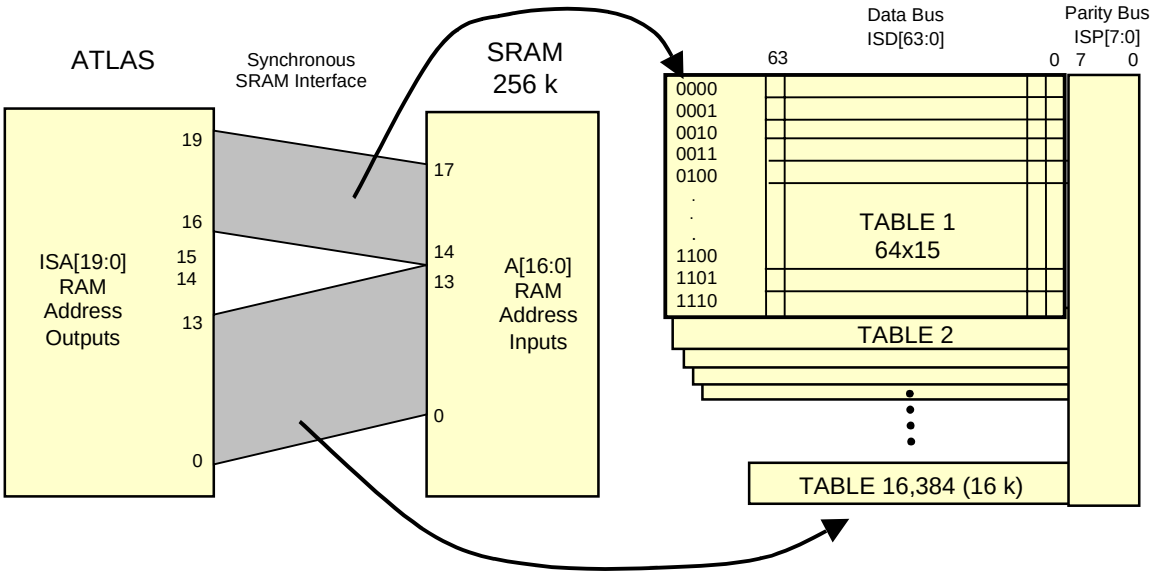
For a more detailed description of the S/UNI-ATLAS, see the S/UNI-ATLAS Datasheet, PMC-971154 document [4].

5.1.1. Ingress SRAM

The Ingress VC Table is stored externally to the S/UNI-ATLAS in SRAM (Static RAM). The ingress SRAM data bus is 72 bits wide (8 bytes plus byte parity), with an address space of 20 bits (1 M). This creates enough context address space for 64 k VCs. The entire SRAM space does not have to be populatedr. If fewer than 64 k VCs are required or a subset of the S/UNI-ATLAS features are used, then the SRAM may be saved. The Ingress VC Table rows marked as 1011, 1100, 1101, and 1110 may be skipped. (In some isolated cases, mostly with older RAMs, glue logic may be required.)

Figure 8 shows an example of a connection of a Synchronous SRAM 20-bit wide address interface on the S/UNI-ATLAS into a 256 k 17-bit wide address SRAM. This configuration allows 16 k of VC Tables. The figure also shows addressing structure of a VC Table.

Figure 8. S/UNI-ATLAS SRAM VC Table Addressing

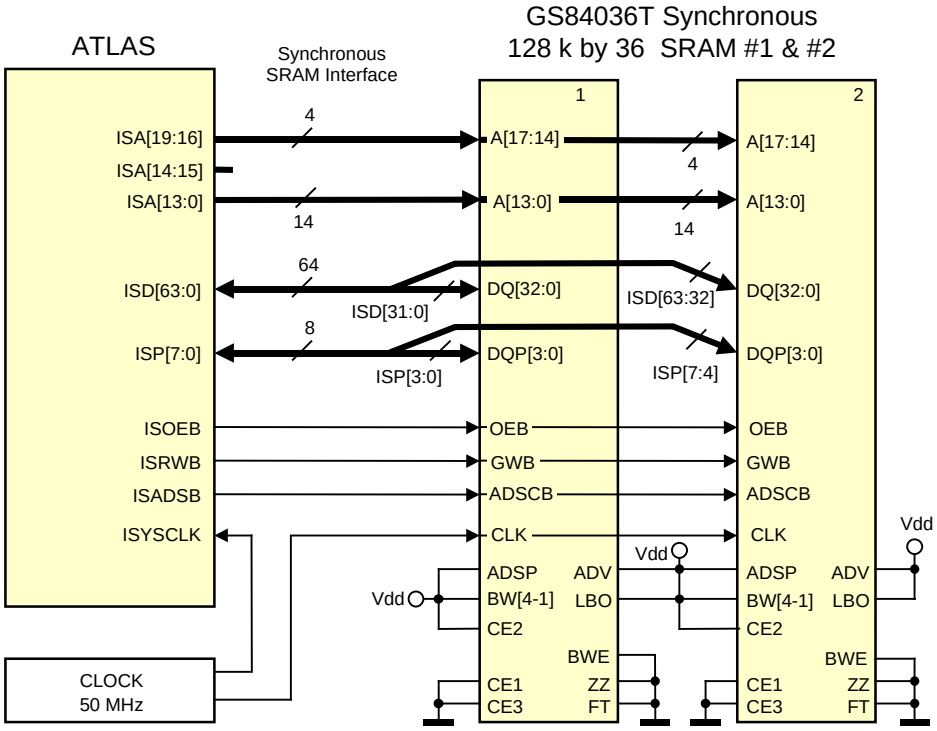


The four most significant bits in the ISA bus, ISA[16:19] *must always* be connected. Those bits point to a data row in the VC Table. The least significant portion of the address space can be used as required for each application. The above example uses 14 bits (ISA[13:0]) for the table address. The address space in the example allows addressing for 2^{14} (16 k) VC Tables. Bits 14 and 15 are unconnected.

The total RAM space required for the above example is calculated as follows: (64 + 8) x 15 x 16384 = 17,694720 bits. Two 256 k 36-bit wide RAM devices allow storage of 262,144 x 36 x 2 = 18,874,368 bits. This is provided using one bank of two 256 k by 36 SSRAMs to make up the 72-bit wide data path. As there is only one bank of SSRAM, there is no address decode necessary.

The Reference Design uses two GS88036T 256 k by 36 Synchronous SSRAMs manufactured by GSI Technology, Inc. A 100-pin TQFP package was chosen. Figure 9 shows the Ingress S/UNI-ATLAS to the SSRAM interface.

Figure 9. VC Ingress S/UNI-ATLAS-SSRAM Connection



For more information about how other configurations can be implemented, see the appendix in the S/UNI-ATLAS data sheet document, *Interfacing SSRAM to the S/UNI-ATLAS*. The appendix describes SSRAM configurations and several examples. The appendix also lists SSRAMs from various manufacturers that are compatible with the S/UNI-ATLAS and with this design in particular. For the S/UNI-ATLAS, synchronous flow-through (non-pipelined) SSRAMs must be used.

5.1.2. Egress RAM

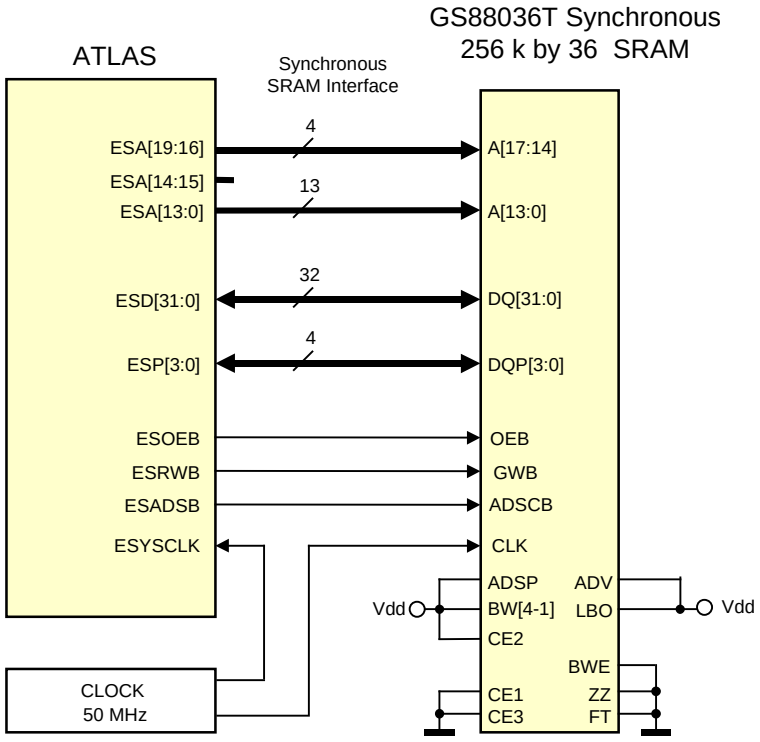
The Egress VC Table is stored external to the S/UNI-ATLAS in SSRAM. The addressing structure is similar to the ingress addressing shown in Figure 8. The egress SSRAM data bus is 36 bits wide (4 bytes plus byte parity), with an address space of 20 bits (1 M). This provides for 64 k connections, as with the Ingress VC Table. If fewer than 64 k connections are required or a subset of S/UNI-ATLAS features are used, then SRAM may be saved.

The Core Card Reference Design has enough SRAM to support 16 k connections at the egress port. This is provided using one 256 k by 36 SRAM (1 MB). As there is only a single SSRAM, no address decode is necessary. For the S/UNI-ATLAS, synchronous flow-through, non-pipelined SSRAMs must be used.

The Reference Design uses a GS88036B 256 k by 36 Synchronous SRAM manufactured by GSI Technology, Inc. (in a 100-pin TQFP package).

Figure 10 shows the egress S/UNI-ATLAS – SSRAM interface.

Figure 10. VC Egress S/UNI-ATLAS-SSRAM Connection



The four most significant bits in ESA bus, ESA[16:19] *must always* be connected.

For more bus termination and signal integrity examples, see section 11 in this document.

5.2. S/UNI-APEX

5.2.1. Functional Description

The PM7326 S/UNI APEX is a full duplex ATM traffic management device, that provides cell switching, per-VC queuing, traffic shaping, congestion management, and hierarchical scheduling for up to 2048 loop ports and up to four WAN ports.

The S/UNI APEX provides per-VC queuing for 64K VCs. A per-VC queue may be allocated to any Class of Service (COS), within any port, in either direction (ingress or egress path). Per-VC queuing enables PCR or SCR per-VC shaping on WAN ports and greater fairness of bandwidth allocation between VCs within a COS.

The S/UNI APEX provides three level hierarchical scheduling for port, COS, and VC level scheduling. There are two, three-level schedulers—one for the loop ports and one for the WAN ports. The three-level scheduler for the WAN ports provides:

- Weighted Interleaved Round Robin (WIRR) scheduling across the four WAN ports that enables bandwidth allocation selection between the ports.
- Priority Fair scheduling across the four COSs within each port. This class scheduler is a modified priority scheduler that allows minimum bandwidth allocations to lower priority classes within the port. Class scheduling within a port is independent of activity on all other ports.
- Three types of VC schedulers. VC scheduling within a class is independent of activity on all other classes
    - Shaped fair queuing is available for four classes. If the COS is shaped, each VC within the class is scheduled for emission based on its VCs shaping rate. During class congestion, the VC scheduler may lower a VC rate in proportion to a normalization factor calculated as a function of the VC rate and the aggregate rate of all active VCs within the class.
    - Weighted Interleaved Round Robin scheduling in which weights are used to provide fairness between the VCs within a class.

- Frame continuous scheduling where an entire packet is accumulated before it is transferred to a class queue.

The three-level scheduler for the loop ports provides weighted Interleaved Round Robin (WIRR) scheduling. This scheduling, across the 2048 loop ports, enables bandwidth allocation selection between the ports and ensures that minimal PHY layer FIFOing is required to support a wide range of port bandwidths. Supported port bandwidths are from 32 kb/s to 52 Mb/s.

Priority scheduling across the four COSs within each port. Class scheduling within a port is independent of activity on all other ports.·

VCs within a class are scheduled with a Round Robin scheduler or Frame Continuous scheduling. VC scheduling within a class is independent of activity on all other classes. Shaping is not supported on loop ports.

The S/UNI APEX forwards cells through tail of queue enqueuing and head of queue dequeuing (emission), where tail of queue enqueuing is controlled by the VC context record and subject to congestion control, and head of queue dequeuing is controlled by the three level hierarchical schedulers. The VC context record allows for enqueuing to any queue associated with any port and supports full switching from a port to port.

The S/UNI APEX supports up to 256 k cells of shared buffering in a 32-bit wide SDRAM. Memory protection is provided through an inband CRC on a cell by cell basis. Buffering is shared across direction, port, class, and VC levels. The congestion control mechanism provides guaranteed resources to all active VCs, allows sharing of available resources to VCs with excess bandwidth, and restricts buffer allocation on a per-VC, per-class, per-port, and per-direction basis. The congestion control mechanism supports PPD and EPD on a CLP0 and CLP1 basis across per-VC, per-class, per-port, and per-direction structures. EFCI marking is supported on a per-VC basis. Congestion thresholds and packet awareness is selectable for each connection.

The S/UNI APEX provides flexible capabilities for signaling, management, and control traffic. Four independent uP receive queues exist where both cell and AAL5 frame traffic may be enqueued for termination by the uP. A staging buffer is also provided enabling the uP to enqueue both the cell and AAL5 frame traffic to any outgoing queue. AAL5 SAR assistance is provided for AAL5 frame traffic to and from the uP. AAL5 SAR assistance includes the generation and checking of the 32-bit CRC field and the ability to reassemble all the cells from a frame in the VC queue before placement on the uP queues. Any or all of the 64 k VCs may be configured to be routed to/from the uP port. Any or all of the VCs configured to be routed to/from the uP port may also be configured for AAL5 SAR assistance

simultaneously. OAM cells may be routed optionally (per-VC selectable) to a uP receive queue or switched with the user traffic. CRC10 generation and checking is optionally provided on OAM cells to and from the uP.

The S/UNI APEX maintains cell counts of CLP0 and CLP1 cell transmits on a per-VC basis. Global CLP0 and CLP1 congestion discards are also maintained. Various error monitoring conditions and statistics are accumulated or flagged.

The uP has access to both the internal S/UNI APEX registers and the context memory, as well as diagnostic access to the cell buffer memory.

The S/UNI APEX provides a 16-bit wide Any-PHY compliant loop side master/slave interface that supports up to 2048 ports. Egress cell transfers across the interface are identified through an inband port identifier prepended to the cell. To accept the cell, the slave devices must match the inband port identifier with their own port ID or port ID range. Per port egress flow control is executed through a 12-bit address polling bus to which the appropriate slave devices respond with out-of-band per port flow control status. Ingress cell transfers across the interface is executed through a combination of UTOPIA L2 flow control polling and device selection for up to 32 slave devices. The Any-PHY loop side interface may be reconfigured as a standard single port 16-bit wide Any-PHY or UTOPIA L2 compliant slave interface. The 16-bit prepends are supported optionally on both ingress and egress for cell flow identification, enabling use with external address resolution devices, switch fabric interfaces, or other layer devices.

The S/UNI APEX provides an 8- or 16-bit Any-PHY or UTOPIA L2 compliant WAN side master interface that supports up to four ports. The 16-bit prepends are supported optionally on both ingress and egress for cell flow identification, enabling use with external address resolution devices, switch fabric interfaces, or other layer devices.

The S/UNI APEX provides a 32-bit microprocessor bus interface for signaling, control, cell, and frame message extraction and insertion, VC Class and port context access, control and status monitoring, and configuration of the IC. Microprocessor burst access is supported for registers, cell and frame traffic..

The S/UNI APEX provides a 36-bit SSRAM interface for context storage that supports up to 4 MB of context for up to 64 k VCs and up to 256 k cell buffer pointer storage. Context Memory protection is provided with 2 bits of parity over each 34-bit word.

The total number of cells, the total number of VCs, support for address mapping, and shaped fair queuing is limited to the amount of context and cell buffer

memory available. Table 1 shows the most common combinations of memory and features.

TABLE 1. Feature Set as a Function of Memory Capacity

Context Memory Size ZBT SSRAM	Cell Buffer Memory Size SDRAM	# VC	# Cell Buffers	Address Mapping Support	Shaping Support
1 MB	4 MB	16 k	64 k	Yes	No
2 MB	4 MB	16 k	64 k	Yes	Yes
2 MB	4 MB	64 k	64 k	No	No
4 MB	16 MB	64 k	256 k	Yes	Yes

NOTE: The table may not correspond to the final settings on the Core Card due to RAM availability and other reasons. Designers should follow the RAM size recommendations outlined in the above table and in the calculations presented in document [12].

The Reference Design Core Card supports the layout for 4 MB of Context Memory SSRAM and 16 MB of Cell Buffer SDRAM, thus allowing 64 k of VCs and 256 k of buffered cells. The maximum RAM size was chosen for evaluation purposes and interface verification. However, due to RAM availability, the Core Card may be populated with smaller size NBT RAM. Board inspection is required to determine actual RAM size. The RAM interfaces are described in following sections.

The S/UNI-APEX provides facilities to enable sparing capability with another S/UNI-APEX device. The facilities enable a *warm standby* capability, in which connection setup between the two devices can be maintained identically but some cell loss occurs at the point of device swapping. The facilities do not include a cell-by-cell lock step between the two S/UNI-APEX devices. To avoid any cell replication, queues in the *spare* S/UNI-APEX are kept empty, causing all queued traffic in the *active* S/UNI-APEX to be lost at the point of switch over. Since connection setup is maintained identically between the two S/UNI-APEX devices, switch over can happen instantaneously allowing you to avoid connection timeout or teardown issues.

The S/UNI-APEX facilities provided are the disable and filter control bits in the Receive and Transmit Control register. These control bits are asserted in the spare S/UNI-APEX to ensure the queues remain empty until swapping is initiated. Alternatively, asserting only the Filter enable bits allow signaling and control traffic continuity to be maintained to the spare S/UNI-APEX. This enables

datapath integrity testing on the spare plane and ensures control communications paths to the spare plane are usable.

5.2.2. Context Memory SSRAM Interface

The S/UNI-APEX context memory SSRAM interface can be configured for two types of synchronous RAMs: *Late Write* or *Zero Bus Turnaround*™ (also known as NBT). The Core Card is assembled with a pipelined ZBT/NBT SSRAM. Schematic and board layout support optional placement of a RAM, up to 2 Mbytes each with address lines CMA<19..0> connected. Also, the layout supports the RAM core supply at 2.5 V for GS8162Z18 (the pinout is preliminary at the time this document is created, and pinout verification is advised). The GS162Z18 option requires zero-ohm resistor that strap 2.5 V to the CORE1 rail. Other RAMs from Samsung and possibly from IDT and Cypress may be placed with minimum rework on the board. Schematic and layout, of the Core Card Reference Design Issue. 3, supports only GSI GS882Z18 NBT RAM without any strapping. RAMs are set in a single bank that consist of two 512 M x 18 ZBT SRAMs (1 MByte each) and provide 2 MB of SSRAM memory.

The SSRAM bus is clocked at 80 MHz. Signal integrity simulation and timing simulation was done to derive design guidelines. Serial termination resistors are inserted in data path to attenuate backreflections and improve signal integrity. For more examples on bus termination and signal integrity, see Section 11, *Bus Termination Examples*, in this document.

The S/UNI-APEX SSRAM address bus CMA[19:0] is connected with all lines that allow an address up to 1,048,576 (1 M). CMCEB is used to control chip selection on RAMs.

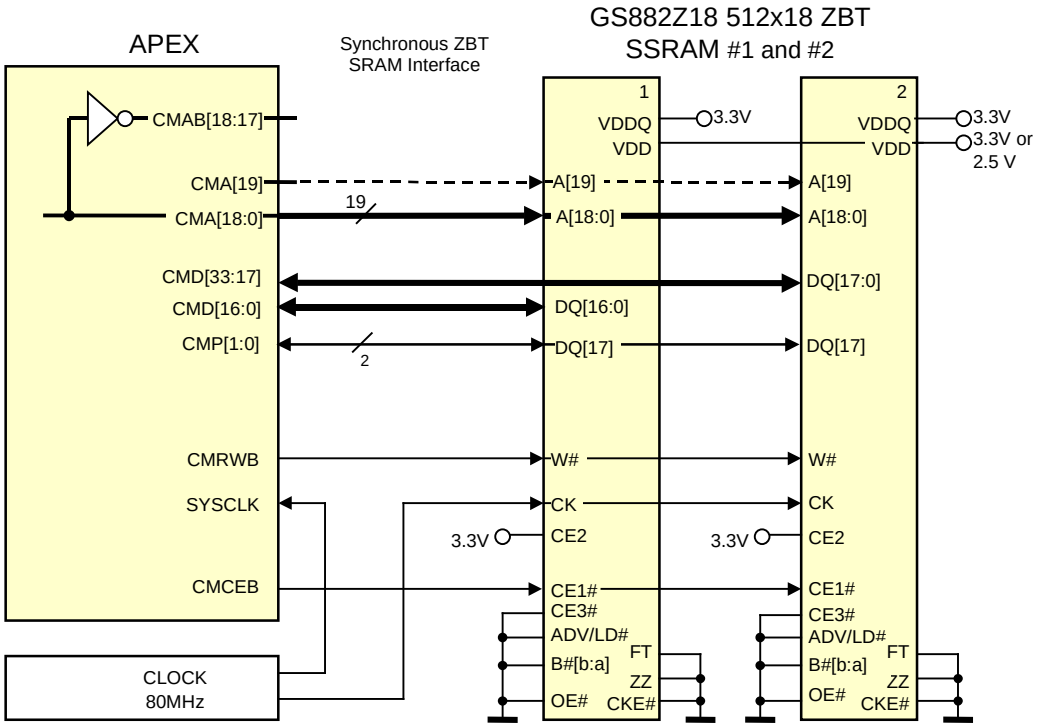
The data bus CMD[33:0] is split into lower and upper chunks and connected to respective SSRAM devices. Each 17-bit wide segment is associated with a parity bit CMP[0] or CMP[1], which are connected to the corresponding DQ[17:0] 18-bit wide ports on the SSRAM devices. The S/UNI-APEX generates the parity bit , which is stored into RAM.

The OE# inputs on the SSRAM is tied to ground. The read/write line CMRWB determines if the data bus is in a read or write cycle. For more information about bus timing, see Section 11, *Bus Termination Examples*, in this document.

If the S/UNI-APEX detects a parity error, the two parity bits protecting the 34-bit data bus can trigger an interrupt at the S/UNI-APEX. Parity check generation can be used to detect data corruption in highly reliable data transfer protocols or networks.

Figure 11 shows the S/UNI-APEX to the SSRAM interface.

Figure 11. Dual Bank Configuration for ZBT SSRAM



For examples of a generic interface to SSRAM, see the S/UNI-APEX data sheet.

The Core Card schematic Issue 3 on page 9 shows an optional core supply with 2.5 V for larger NBT SSRAMs. The board is laid out with a copper cutout underneath the RAMs, allowing a 3.3 V or 2.5 V supply with different resistors placement on assembly line. The Core Card printed circuit board Rev. 3 is assembled with a 3.3 V version of NBT SSRAM. The designer should evaluate the availability of RAMs, and possibly choose to eliminate the 2.5 V supply by shorting the copper cutout to 3.3 V.

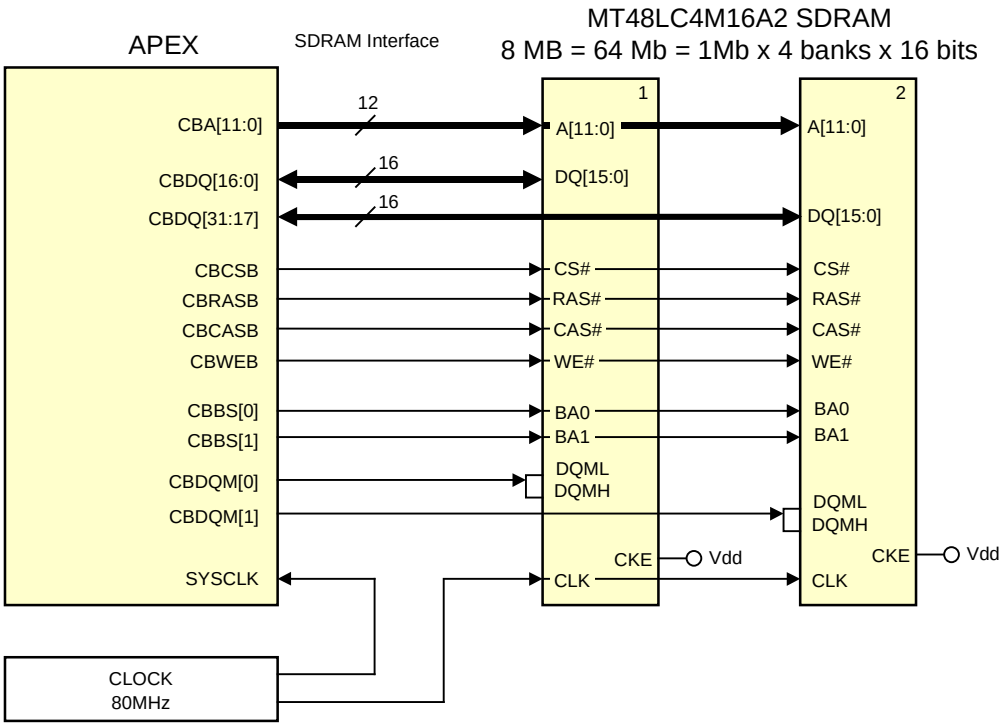
5.2.3. Cell Buffer SDRAM Interface

The Reference Design shows the S/UNI-APEX with 16 MB of SDRAM for queued cell buffering. The SDRAM buffer consists of a single bank with two RAMs for a 32-bit wide data path that provides room for up to 64 k cells. The SDRAMs are Micron's MT48LC4M16A2TG 8 MB (size derived from 1 Mb x 16 x 4 banks = 64 kb = 8 MB).

The S/UNI-APEX allows CRC-16 check on the first 60 bytes in per-cell basis of the data from the SDRAM. If an error occurs, an interrupt is sent to the microprocessor.

Figure 12 shows an example of a 16 MB SDRAM.

Figure 12. Single Bank SDRAM 4 MB for 64 k Cells



The data mask signals CBDQM[1:0] at the S/UNI-APEX control the read/write cycle on the CBDQ[31:0] bus.

The S/UNI-APEX and SDRAMs run at 80 MHz for the Core Card. Bus termination and signal integrity examples are shown in this document in Section 11, *Bus Termination Examples*,

5.3. S/UNI-VORTEX

The PM7351 S/UNI-VORTEX is a monolithic integrated circuit typically used with its sister device, the S/UNI-DUPLEX, to implement a point-to-point serial backplane interconnect architecture.

Multiple S/UNI-VORTEX devices can reside on a common cell processing card beside a traffic management device. The traffic management device exchanges

cells with the S/UNI-VORTEX through a 16-bit wide SCI-PHY or Any-PHY interfaces (bus). The flow control is affected across this interface through cell available signals that the S/UNI-VORTEX generates. In the downstream direction, the traffic management device can poll for the availability of a buffer for each logical channel. In the upstream direction, an indication is provided whether one or more cells are queued in the S/UNI-VORTEX for transfer.

Each S/UNI-VORTEX can be connected to eight Line Cards through high-speed 100 to 200 Mb/s serial links. Each upstream link has its own queue. If a queue becomes nearly full, a flow control indication is sent downstream. In the downstream direction, each logical channel has a dedicated cell buffer to avoid head of line blocking. The serialization of cells from the cell buffers is throttled by flow control information sent from the line card through the upstream high-speed link.

A microprocessor port provides access to internal configuration and monitoring registers. That port can also be used to insert and extract cells in support of a control channel.

LVDS INTERFACES, BOTH DIRECTIONS:

- Eight independent four-wire LVDS serial transceivers, each operating at up to 200 Mbps across PCB or backplane traces or across up to 10 meters of four-wire twisted pair cabling for inter-shelf communications.
- Usable bandwidth (excludes system overhead) of 186 Mbps, for each direction of each LVDS link.
- Fully integrated LVDS clock synthesis and recovery. No external analog components are required.

RECEIVE DIRECTION:

- Weighted round-robin multiplex of cell streams from the eight LVDS links into a single cell stream that is transferred to the parallel bus under control of the bus master.
- LVDS link and S/UNI-VORTEX identifiers that are added to each cell (along with the PHY identifier already added by S/UNI-DUPLEX) for use by the ATM layer to identify the cell source.
- Back-pressure that is sent to the far end to prevent an overflow of the receiver FIFO.

TRANSMIT DIRECTION

- Per-PHY and microprocessor port back-pressure that are used on each of the eight links to prevent the overflow of downstream buffers.

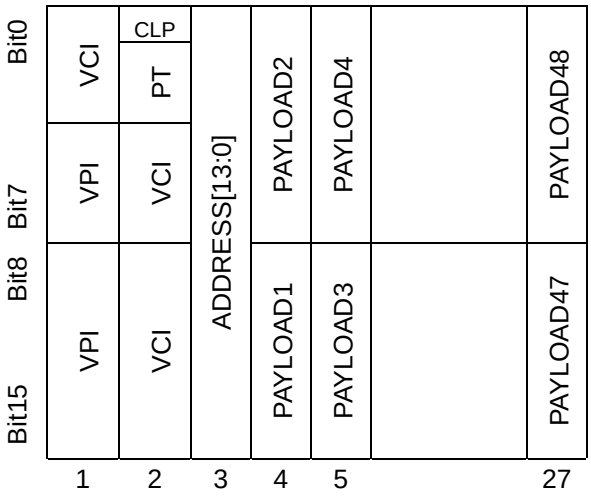
- Device polling that provides Utopia-like TCA status for 264 PHYs (includes 8 control channels), based on back-pressure from the LVDS links.
- Cell transfer, where the bus master adds a PHY address to each cell through a 12-bit identifier. The S/UNI-VORTEX decodes and accepts the cells for its links, based on software-configured base addresses.

PARALLEL BUS INTERFACE:

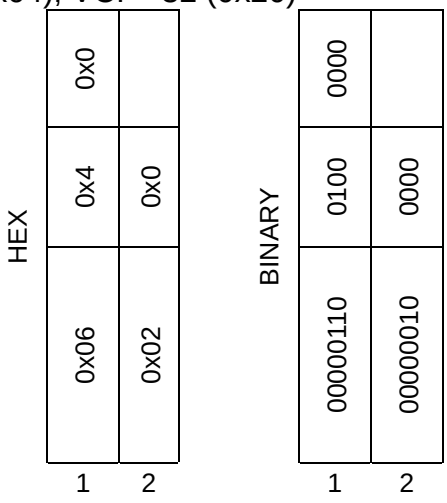
- Both directions: 16-bit wide, 50 MHz maximum clock rate, bus slave.
- Cells transferred to the bus - Utopia L2 compatible with optional expanded length cells. The cell appears as from a single PHY, with a cell prepend that identifies the source PHY ID of each cell. Alternatively, Utopia L2 compliance is supported by placing the PHY ID inside the UDF/HEC fields of a standard ATM cell.
- Cells received from the bus. The Any-PHY bus is similar to Utopia L2, however with optional expanded length cells and expanded addressing capabilities. The S/UNI-VORTEX appears to the bus master as a 264-port, multi-PHY device (eight links, each with 32 PHYs & a communication channel). The PHY address is added as the cell prepend or optionally in the HEC/UDF field when standard length cells are desired.

Example of a 16-bit wide UTOPIA L2 cell is shown below.

Utopia L2 Cell



VPI/VCI example: VPI = 100 (0x64), VCI = 32 (0x20)



Core Card software driver applications sets UL2 bus to have word 3 overwritten with logical channel ID from S/UNI-VORTEX and phy ID from S/UNI-DUPLEX.

MICROPROCESSOR INTERFACE

- 8-bit data bus, 8-bit address bus.
- Provides read/write access to all configuration and status registers.
- Provides CRC32 calculation and cell transfer registers to support an embedded microprocessor-to-microprocessor communication channel over the LVDS link.

5.4. S/UNI-DUPLEX

The PM7350 S/UNI-DUPLEX is a monolithic integrated circuit typically used for traffic concentration within a DSLAM. The device is ATM specific. It exchanges contiguous 53 byte cells with PHY devices. The PHY interface can be either clocked serial data or SCI-PHY/Any-PHY.

A clocked serial data configuration of up to sixteen channels is supported. Cell alignment is established through HCS (Header Check Sequence) delineation. The cell payload is scrambled and descrambled with a $x^{43} + 1$ polynomial. Rate adaptation is performed through idle cell insertion and extraction. Each PHY interface has a dedicated four-cell FIFO in both upstream and downstream directions.

All cell streams are multiplexed into a high-speed serial stream. Each S/UNI-DUPLEX can connect to two 100 to 200 Mb/s Low Voltage Differential Signal (LVDS) serial links. The internal transmit clock is synthesized from a lower frequency reference run at 1/8 of the line rate. An extended cell format provides four extra bytes for the encoding of flow control, timing reference, PHY identification, and link maintenance information. A redundant link is provided to allow connection to two cell processing cards.

A microprocessor port provides access to internal configuration and monitoring registers. The port may also be used to insert and extract cells in support of a control channel.

The S/UNI-DUPLEX is typically used with its sister device, the S/UNI-VORTEX, to implement a point-to-point serial backplane interconnect architecture.

For more information about S/UNI-DUPLEX, see the S/UNI-DUPLEX Datasheet.

5.5. CPCI Bridge

This section briefly introduces the cPCI bridge functionality.

5.5.1. PCI9054 PCI Bridge

To interface the VORTEX chipset residing in the Core Card to the host CPU residing in slot 1 of the cPCI shelf, a PCI-to-Local-bus bridging device is required. The device chosen for this Reference Design is the PLX PCI9054 PCI Bus Master I/O Accelerator Chip. Some features that were deciding factors in becoming the bridge of choice for this Reference Design are:

- PCI v2.2 compliant 32-bit 33 MHz Bus Master Interface Controller that enables PCI Burst Transfers up to 132 Mbytes/second
- General Purpose Bus Master Interface featuring an advanced Data Pipe Architecture™ which includes two DMA engines, programmable Target and Initiator data transfer modes and PCI messaging functions
- PCI v2.2 Power Management Spec compatible
- Flexible +3.3 V, +5 V Tolerant Local Bus operation up to 50 MHz
- 32-bit multiplexed, or non-multiplexed local bus supporting 8-, 16-, and 32-bit peripheral and memory devices
- CompactPCI hot-swap capability

Since the S/UNI-APEX requires a multiplexed bus, for this Reference Design, the PCI 9054 bridge is programmed to perform in a 32-bit multiplexed mode (J mode). The fact that the S/UNI-APEX is a 32-bit device, the S/UNI-ATLAS is a 16-bit device, and the S/UNI-VORTEX and S/UNI-DUPLEX are both 8-bit devices adds complexity to the local bus, on which they all reside. While the local bus can support 8-, 16-, and 32-bit devices, for this Reference Design, the PCI 9054 operates solely in 32-bit mode. (For more information, see section 8.4.)

5.5.2. SEEP Basics

The PCI 9054 provides a serial EEPROM (SEEP) port for loading configuration information on power-up and reset. The SEEP is programmed with address space boundaries for the VORTEX chipset and the Core Card IDs. The CPLD is used with the PCI9054 to provide address decoding and microprocessor port control for the DSLAM chips being accessed from the PCI bus. For more information about SEEP, see sections 8.6 and 8.7.
Examples of data reading on reset are shown in section 16 *APPENDIX C: EXAMPLE OF SEEP READING ON RESET* in this document.

6. SIGNAL FLOW ON THE CORE CARD IN BRIEF

6.1. Upstream Direction

The following process refers to the VORTEX Chipset Driver defaults or test routines, for example, the cells on Utopia L2 into the S/UNI-ATLAS Ingress are 27 words with the ID written into the HEC/UDF word.

Cells that originate from a Comet or PHY device on the Line Cards and are destined for the WAN Card are manipulated in the following manner:

- Upstream cells are received by the PHY and buffered until the S/UNI-DUPLEX reads them. As a cell is read from the PHY, the S/UNI-DUPLEX writes the originator PHYID[4:0]—or microprocessor ID, in the case of the embedded Inband Communication Channel (ICC)—into the LVDS data structure and sends the cell through the LVDS serial link to its corresponding S/UNI-VORTEX on both the active and stand-by Core Cards.
- The S/UNI-VORTEX receives cells by servicing its eight links in a simple weighted round-robin fashion. As the S/UNI-VORTEX reads cells from the high-speed serial link, it inserts into the HEC/UDF field the ADDR[13:0], which contains its own hardwired S/UNI-VORTEX ID VADR[4:0] (ADDR[13:9]), the high speed LINKID[2:0] (ADDR[8:6]), and the logical channel ADDR[5:0]. At this point, cells are available to the Scy-PHY/UL2 bus that connects the S/UNI-VORTEX to the S/UNI-ATLAS. (software test routines generate cells which are Utopia L2 compatible.)
- After an upstream cell is read in by the S/UNI-ATLAS, it will use the PHYID, LINKID, and VORTEX IDs to perform a lookup function that results in a short connection (or switch) tag being inserted into the HEC/UDF before passing it to the S/UNI-APEX. The S/UNI-APEX uses the tag to directly address the context and control information pertaining to the cell. The present test routines (supplementing VORTEX Chipset Driver) translate the header in the S/UNI-ATLAS.
- The S/UNI-APEX provides per-VC congestion control, buffering, and queuing, and provides switching and traffic shaping into four high-speed WAN up-link ports. Upstream traffic is passed from the S/UNI-APEX back through the S/UNI-ATLAS Egress. The S/UNI-ATLAS first provides counting and OAM functionality. Then the S/UNI-ATLAS transfers the data onto the Core Card’s S/UNI DUPLEX to transmit over the LVDS serial link onto the WAN Card.

- The S/UNI-DUPLEX on the Core Card first writes the destination PHY ID (3:0) (or EIC) into all cells. Then the S/UNI-DUPLEX transmits them to the S/UNI DUPLEX that resides on the WAN Card. The upstream traffic received by the WAN Card's S/UNI-DUPLEX is passed onto the card's S/UNI-QJET, which frames the data into DS3 format and sends it out over the appropriate (one of four) DS3 link.

6.2. Downstream Direction

The following process refers to the software driver defaults or test routines, for example, the cells on Utopia L2 into S/UNI-ATLAS Ingress are 27 words with the ID written into the HEC/UDF word.

Cells that originate from the WAN and are destined for a Line Card or PHY device are manipulated in the following manner:

- Data received by the WAN Card's four DS3 links is passed to the S/UNI-QJET which multiplexes the data, and sends it to the WAN Card's S/UNI-DUPLEX for transmission to the Core Card over the high-speed serial link. The WAN Card's S/UNI-DUPLEX writes the originator PHY ID (3:0) into the LVDS data structure before transmitting data to the CORE card.
- Downstream data received by the Core Card's S/UNI-DUPLEX is passed to the S/UNI-ATLAS. The cells proceed through the S/UNI-ATLAS and onto the S/UNI-APEX, where all ATM layer functions are performed on the cells. The S/UNI-APEX appends to all PHY-destined cells a unique 12-bit address that identifies the destination S/UNI-VORTEX, LINK, and PHY IDs (or S/UNI-VORTEX, LINK, and the EIC). The data is then placed on the ANY-PHY bus that connects the S/UNI-VORTEX devices to the ATM layer of the DSLAM shelf. The present test routines (supplementing Chipset Driver) translate header in the S/UNI-ATLAS.
- The 12-bit address is used by the S/UNI-VORTEX devices that are connected to the ANY-PHY bus to determine whether or not a cell placed on the bus is destined for them; if they are, then the cell should be read.
- Downstream cells received by the S/UNI-VORTEXes are stripped of the prepended address segment. The S/UNI-VORTEX writes the destination PHY ID into the LVDS data structure and sends cells across the appropriate LVDS serial link (7:0) to the corresponding S/UNI-DUPLEX device that resides on the Line Card.
- The Line Card's S/UNI-DUPLEX device, after receiving cells from the high-speed serial interface, strips the prepended bytes from the cells and sends the data to the appropriate PHY (or to the microprocessor in the case of the ICC).

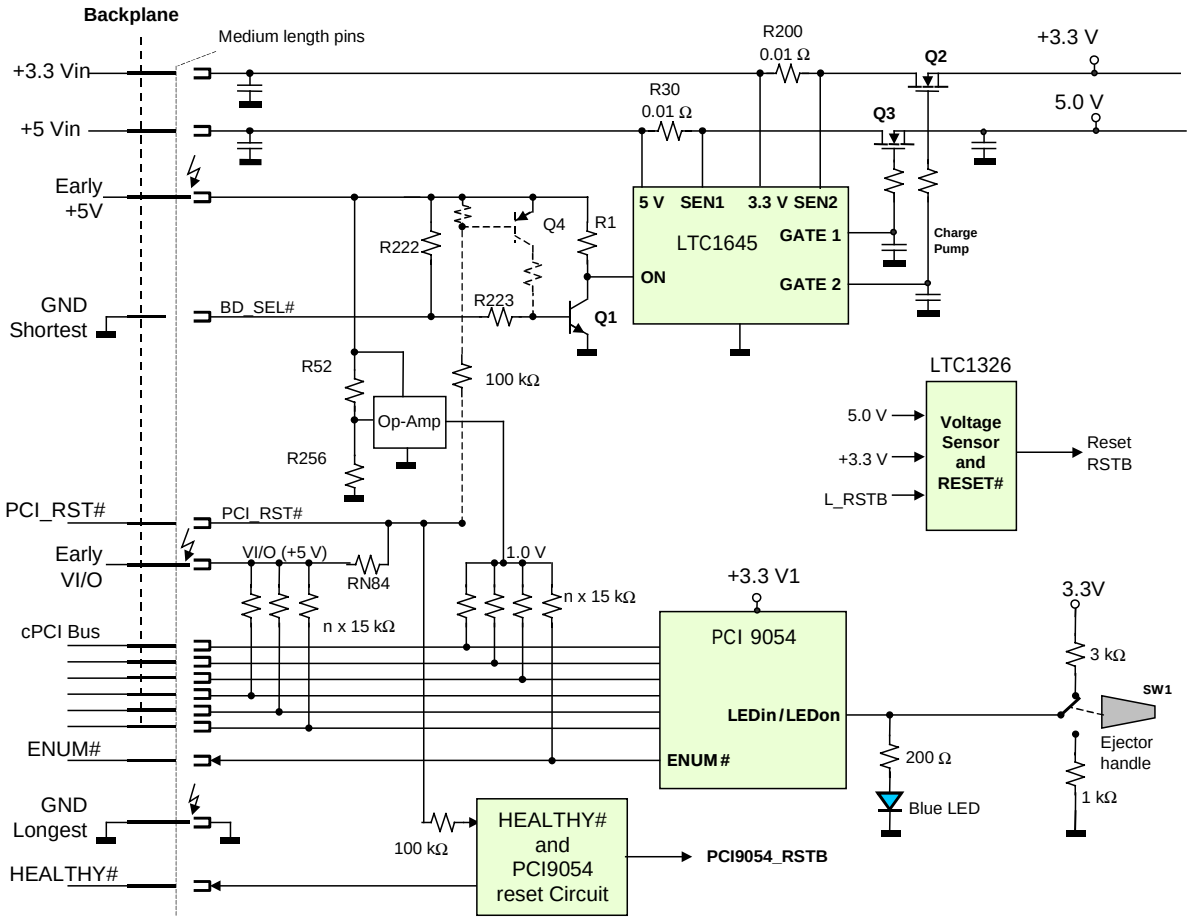
7. HOT SWAP

The Core Card has been designed to be hot-swap compatible. The Hot Swap Specification [19] states: “The basic purpose of the Hot Swap addition to CompactPCI is to allow the orderly insertion and extraction of boards without adversely affecting system operation.”

7.1. cPCI and Power Rail Hot Swap

The Core Card uses a hot-swap compatible cPCI bridge, PLX PCI9054, and a hot-swap controller, the Linear Technology LTC1654. The cPCI connector is assembled with three different length pins, as required by the Hot Swap Specification [19]. The supporting circuitry is also carefully designed to not impair the hot-swap ability. Figure 13 shows an example of the hot-swap circuit.

Figure 13. Example of a Hot-Swap Circuit



The above figure shows that the card is about to be placed into the shelf. The first three mating pins are: the longest GND (ground), the longest +5V (if cPCI is +5 V environment), and long VI/O. The longest +5V pin is also called *early 5 V*. In a 3.3 V environment, it is referred to as *early 3.3 V*. The early VI/O polarizes some of the cPCI bus pins with +5V through 15 kohm resistors. The early +5V flows into a network of resistors and transistors. The current is limited to few mA. The
Op-Amp, biased with the resistive divider R52/R256, provides about 1.0 V of the precharging voltage to the selected cPCI bus interface lines through n x 15 kohm resistors. Immediately after the early +5 V and GND pins are connected, the current flows through resistors R222 and R223, forcing transistor Q1 to saturate and hold the *ON* pin on LTC1645 at *low*. That activity keeps the *GATE1* and *GATE2* pins on the swap controller at low voltage and in turn keeps both MOSFET transistors opened (off).

Card insertion proceeds, and some milliseconds later, the medium length pins on the J1 connector (most of the pins) mate with the cPCI backplane. The *+5 Vin* line connects to: Vcc on LTC1645, and transistors Q2 and Q3 (through R30 and R200).

When the card is pushed deep into the connector, finally the shortest pin (*BD_SEL#*) connects ground to the node with resistors R222 and R223. That activity turns off Q1 and allows the *ON* pin to go *high*. The LTC1645 starts internal timer, and at the same time starts ramp voltage at the *GATE1/2* pins. After about 50 ms, the *GATE1/2* voltage turns on transistors Q30 and Q200 gradually, limiting the inrush current. Eventually, *GATE1/2* goes above 12 V (controlled with internal pump charge) and turns transistors Q30 and Q200 completely on.

The reset and voltage supervising device LTC1326 senses +5 V and 3.3 V going above the predefined threshold, triggering the internal timer, which sets RSTB high after about 200 ms. The LTC1326 device also allows two additional control lines triggering reset at the RSTB line. One of the lines is connected through a resistor to the cPCI reset line PCI_RST#. The other line is connected to the PCI9054 reset output, allowing for software reset on the local bus.

At this point, the +3.3 V is supplied to the PCI9054 cPCI bridge. The PCI9054 sets *ENUM#* (open drain active low) signaling to the host CPU, indicating that a new card is inserted. The *ENUM#* line stays low until the host processor toggles the bit in the internal register at the PCI9054 bridge. If the ejector handle is fully closed and the microswitch is activated, and if the host card RESET (PCI_RST#) is activated and released, the *ENUM#* line goes from low to high.

If the “PCI_RST#” is asserted (held low) by the host processor card (while the card is inserted or at any time), then the LTC1326 keeps *RSTB* asserted. Optionally, the *PCI_RST#* can be connected through a 100 kohm resistor to the base of the P-channel transistor Q4. If the *PCI_RST#* is asserted, then the Q4 turns on and forces the current through a resistor and the base of transistor Q1. This keeps Q1 saturated, and the LTC1645 via both MOSFETs cuts off +5 V and 3.3 V to the card. If the card is already powered, the assertion of the *PCI_RST#* turns off transistors Q30 and Q200 and cuts off supply voltage to the rest of the circuit – a sort of a very hard reset.

NOTE: the serial 0.01 ohm resistor and copper traces in +3.3 V path gives over 35 mV drop at sensing pins at LTC1645. That may create hypersensitivity to small glitches, as the threshold level on sensing pins on LTC1645 is about 50 mV. Designers should observe voltage drop and adjust resistor value to have sensing voltage less than ½ of the threshold (or add RC filtering elements). If LTC1645 on the Core Card triggers too often, then resistor can be temporary shorted.

The toggling switch SW1 through the front panel ejector handle initiates the card removing software sequence. The PCI9054 sets *ENUM#* to low and informs the host CPU that the card is about to be removed. The blue LED remains turned off (dark) until the host CPU confirms it is safe to remove the card; at this point, the blue LED is turned on. The supply voltage removal is a reversed action of the insertion with the very first pin (*BD_RST#*) disconnected. That action forces Q1 to saturate and the *ON* pin to go low. The *GATE1/2* voltages are turned off. In turn, transistors Q30 and Q200 are off as well. The turn-off ramps are uncontrolled and abrupt.

An accidentally toggled ejector handle may trigger software action. If the ejector handle is returned to its operating position, the system may detect it and start the boot-up procedure, as if the card had just been inserted.

NOTE: Hot-swap action requires software, which is not supported with this release of the Reference Design board level driver. Also, the host processor card must support the detection of ENUM# activity for the software hot swap.

7.2. LVDS Hot Swap

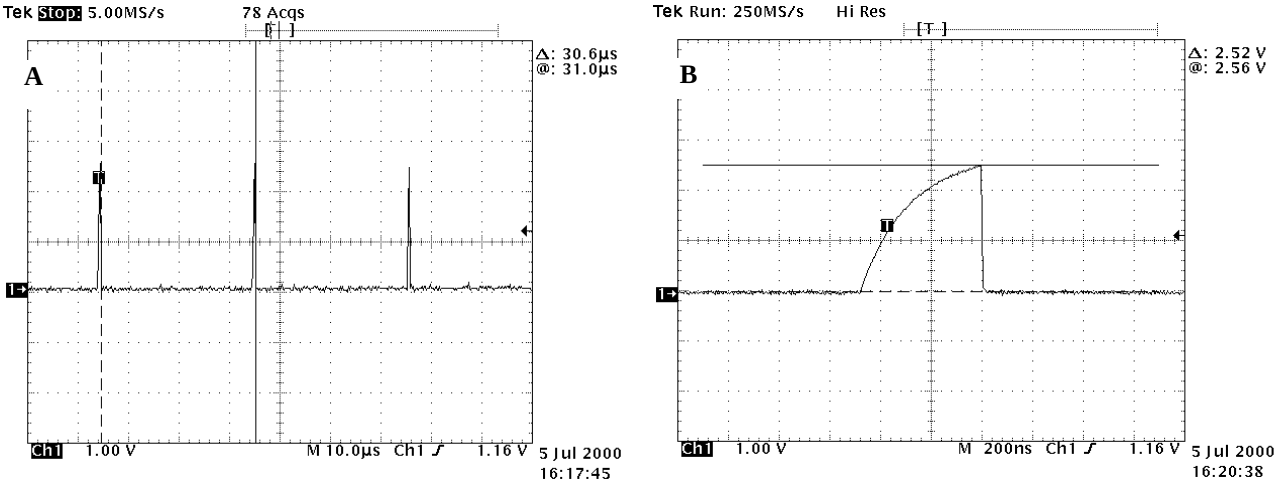
The LVDS interface is fully hot swap compatible. Proper register write sequence is required to ensure cell transfer on the LVDS and Utopia bus. The sequence is implemented in the VORTEX Chipset driver files vcs_api1.c and dpx.c. The most important is to make sure the OCAEN bit in register 0x0A stays disabled until S/UNI-ATLAS polling is enabled. The OCAEN is set to 1 in the as the very last

write, allowing cell transfer from the S/UNI-DUPLEX at that interface. Software designers are required to observe sequencing in their drivers.

7.3. Blue LED and Microswitch Control

The LEDON/LEDIN, pin 53 on PCI9054 (LED_SWITCH\I), is continuously sampled to detect the position of the microswitch. Figure 14 shows the sampling signal.

Figure 14. LED_SWITCH\I Line Siganl



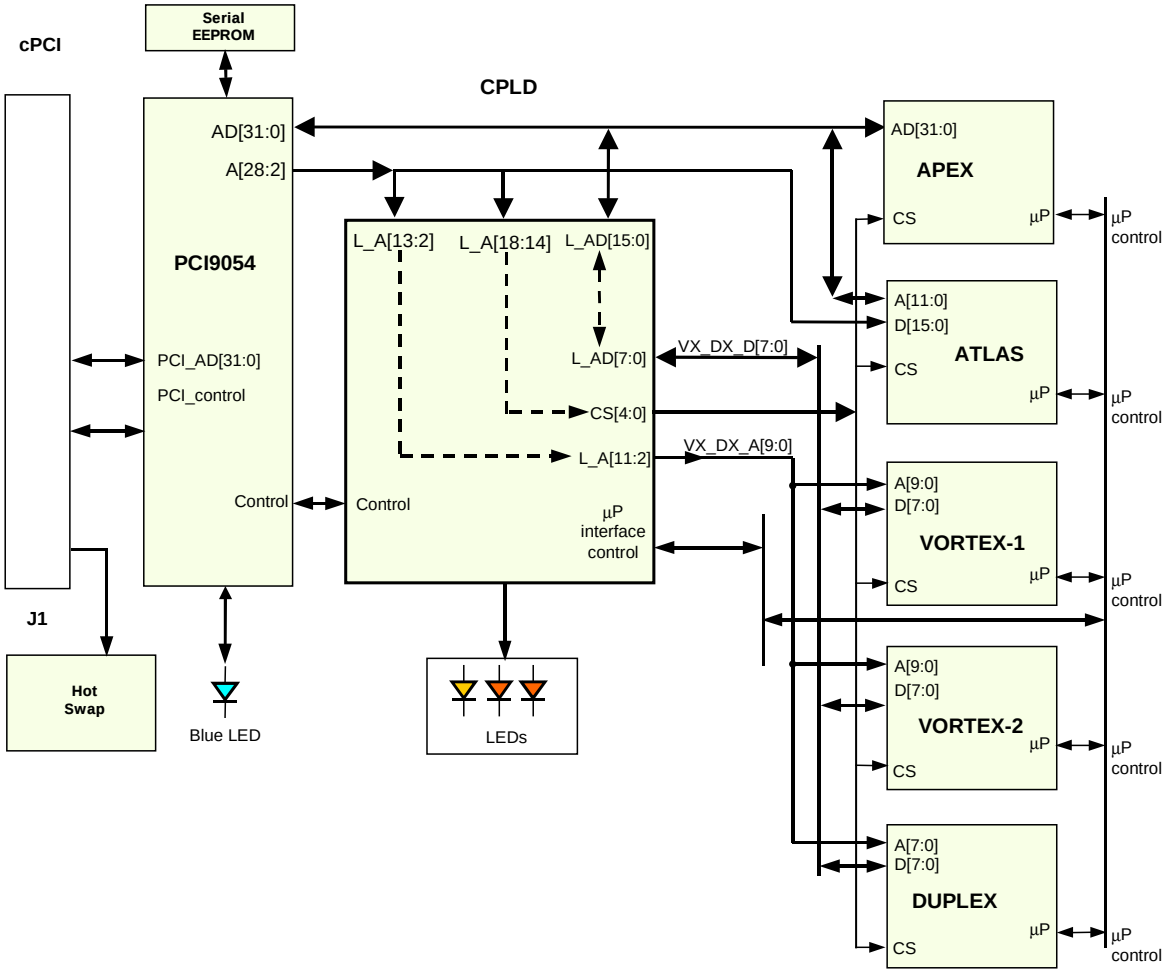
Graphs A and B show a sampling signal output by PCI9054 pin53 LEDON/LEDIN (schematic signal LED_SWITCH\I), captured at TP115 (R233). The microswitch must be in a position where the 3 kohm pull-up resistor (R243), is connected to the LED_SWITCH\I line. Internal to PCI9054 capacitor is charged with that resistor, making time constant of about 200 ns – derived from graph “B” above. The internal capacitor can be calculated at about 60 pF. If resistor is disconnected, the sampling pulses disappear.

8. CPCI INTERFACE, PCI BRIDGE AND CPLD

8.1. Control Interface Block Diagram

Figure 15 shows the block diagram for the cPCI and local bus microprocessor interface on all chips.

Figure 15. cPCI and Local Bus Microprocessor Interface



The 32-bit multiplexed PCI_AD[31:0] ADRESS/DATA bus connects through 10 ohm resistors from the J1 connector to the PLX PCI9054 bridge. The PCI side of the PCI9054 is described in the data book (the PCI interface is beyond the scope of this document). Throughout the Core Card test procedures, problems relating to the PCI interface were not experienced. Proper layout and component soldering assured flawless access to the cPCI bus. Some problems were related

to the size of the SEEP, which must be 4 kbit (for example, NM93CS66). Also, the VORTEX Chipset Driver must match the data stored in the SEEP, must read registers on each chip properly, and verify chip revision. As of July 2000, the chipset revision is as follows: S/UNI-DUPLEX rev. B, S/UNI-VORTEX rev. B, S/UNI-APEX rev. B, and S/UNI-ATLAS rev. D. Designer should check if available devices have other revision numbers.

The local bus side is described as follows. The bridge is set to Multiplexed Bus Mode, as required by the S/UNI-APEX, which operates only with a multiplexed bus (address and data on the same bus). The remaining devices have the microprocessor interface option to work in both the multiplexed and non multiplexed modes. For this Reference Design, those devices operate in non-multiplexed modes. Part of the Core Card board address and data are run through the CPLD, allowing a more balanced load on the local bus LAD[31:0]. The LAD[31:0] bus connects directly from the PCI9054 to the S/UNI-APEX microprocessor address/data port. Bits LAD[15:0] connect also to CPLD and to the S/UNI-ATLAS microprocessor data port. On the S/UNI-VORTEX1, S/UNI-VORTEX2, and S/UNI-DUPLEX, bits LAD[7:0] are routed to the data ports through the CPLD. A direct connection from the PCI 9054 to the local devices creates uneven loads and trace lengths for different bus lines—with the highest capacitance load and the longest traces on lines LAD[7:0] (all devices), and the lowest at LAD[31:16] (S/UNI-APEX only). For this reason, lines LAD[7..0] are routed through the CPLD. Also, proper resistive termination placed along the bus lines helps with signal integrity, as shown later in this document. Signal integrity issues, such as, edge distortion and overshoot, can corrupt data and/or prevent the bus from operating at the maximum speed.

The PCI9054 has an additional dedicated address bus LA[28:2] that allows chip select CS[4:0] to be stable during data cycles and during burst read/writes (no address latch needed). The LA[28:2] bus is split in two sections: lower LA[13:2] for register address and higher LA_SEL[4:0] for chip select. The LA[13:2] is routed directly to the S/UNI-ATLAS microprocessor address port and to the CPLD. The CPLD connects some of those lines to the S/UNI-DUPLEX and S/UNI-VORTEX microprocessor address ports. The LA[28:2] address does not include the least significant two bits. Those two bits are used as byte indicators when accessing an 8-bit wide address. For 32-bit addresses, all addresses are expected to be long-word aligned, making the least significant two bits always *00*. More on local bus is shown in section 8.4.

The CPLD receives data and address lines from the PCI9054,not only for buffering purposes, but also for reading and writing of the CPLDs internal registers. The CPLD also provides additional control lines to and from all DSLAM chips.

8.2. PCI Bridge – CPLD Interface

The PCI9054, with the CPLD, have the job of providing an interface to five VORTEX chipset devices that reside on the Core Card, and to the host processor card that reside at slot 1 of the cPCI shelf. The VORTEX chipset connects to the local bus for which the PCI9054 is the Bus Master. The microprocessor ports of each devices are partially fed by the CPLD. The other portions of the microprocessor interfaces are fed directly from the PCI9054, for example, the address and data at S/UNI-APEX and S/UNI-ATLAS.

The CPLD receives all local control signals from the PCI9054 and the address lines required for device decoding. The CPLD is programmed to provide all necessary functions to the DSLAM devices' microprocessor ports. These functions include chip select, read data, write data, interrupt, and burst for those devices that support bursting –(in this Reference Design, only the S/UNI-APEX).

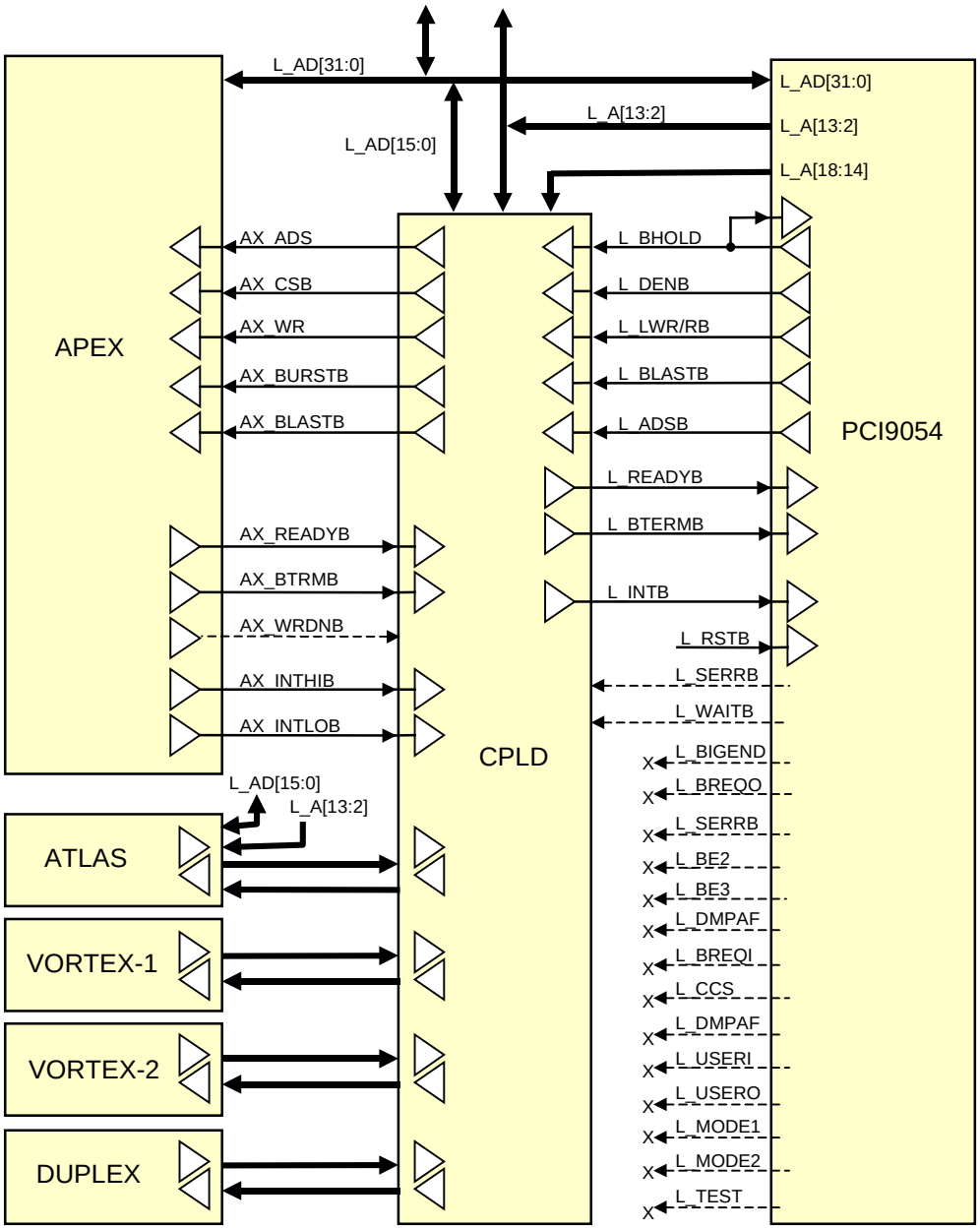
The host processor card initiated transfer is serviced by the PCI 9054, which receives instructions and passes the control signals and address/data lines to the CPLD. The CPLD decodes the address and supplies the correct control signals to the DSLAM device being accessed.

8.3. Major Control Lines Between S/UNI-APEX, CPLD and PCI9054 Interface

The PCI9054 provides address/data bus, local address bus, and a set of control lines on the local side. The CPLD plays a key role in creating proper signaling on the multiplexed bus.

Figure 16 shows the address, data buses and control lines for the S/UNI-APEX and other devices.

Figure 16. S/UNI-APEX, CPLD, and the Local Bus Microprocessor Interface



The block diagram shows the detailed connections to the S/UNI-APEX and general connections to other devices. The PCI9054 provides numerous control lines. The active signals, L_HOLD, L_DENB, L_LWR/RB, L_BLASTB, and L_ADSB are connected to the CPLD. Two additional lines L_SERRB and

L_WEITB are also connected but not used for the CPLD logic. CPLD outputs three control lines: L_READYB, L_BTERMB, and L_INTB terminated at the PCI9054 bridge. The L_INTB line is a combined interrupt from all devices. The AX_BURSTB line is connected from CPLD to the S/UNI-APEX, and it is always asserted when accessing the S/UNI-APEX. Other control lines are not used and may have pull-up or pull-down resistors.
For more information about S/UNI-ATLAS, S/UNI-VORTEX, and S/UNI-DUPLEX interfaces, see the schematics.

Examples of the signal timing are shown in section 17 *APPENDIX D: LOCAL BUS TIMING EXAMPLES* in this document.

8.4. Address Mapping

In the Reference Design, there is a local bus on which a 32-bit device (S/UNI-APEX), a 16-bit device (S/UNI-ATLAS), and 8-bit devices (S/UNI-DUPLEX and S/UNI-VORTEX) reside. This constraint provides two possibilities:

- To use the 9054 ability to provide a dynamic interface to a 32-bit PCI bus to 8-, 16-, and 32-bit local busses. While this option would have maximized memory efficiency on the CPU side, it also would have increased the design's complexity, in both hardware and software.
- To treat all devices as if they were 32 bit devices (the option chosen for this Reference Design). The CPU assigns a 32-bit address space to all devices. For 8-bit devices, 24 bits of every CPU word are ignored. For the 16-bit device, half of all CPU words are ignored. The major fault with this design choice is the waste of CPU memory. However, because the DSLAM chipset does not require a large amount of memory space, this design choice is acceptable, given that it reduces the design's complexity.

Address translation works as follows. For a 32-bit local bus, the PCI9054 expects all addresses to be word (32-bit) aligned, causing all addresses to end with *00*. As a result, the PCI9054 does not even provide the lowest two address bits on the local address bus (LA<28:2>). To accommodate this, every local address is mapped to a word-aligned boundary on the CPU side, that is, register 0011b on the S/UNI-DUPLEX is addressed as 1100b on the CPU side. Because the third S/UNI-DUPLEX register is mapped to the twelfth CPU register, several CPU registers are unused. This corresponds to the ignored bits mentioned in the previous paragraph. The same register on the local bus is derived in hex as 0x03 * 4 = 0x0C and with the offset specific to this Reference Design, it becomes the S/UNI-DUPLEX address 0x1400C.

8.5. PLX PCI9054 Address Spaces

The PCI9054 offers three separate local address spaces, which can be programmed individually to offer 8-, 16-, or 32-bit accesses, burst capability, wait states, etc. If this design had used different local bus widths for the different designs, all three-address spaces would have been necessary. The three-address spaces are not necessary because all the devices are treated as 32-bit devices. For this Reference Design, a one-address space is used for all devices.

8.6. Card ID Number

The Card ID number stored in the SEEP may change with the progress of the programming work. It is recommended to remove SEEP, and place in a programmer and read content.

TABLE 2 shows application-specific Card ID numbers, stored in the SEEP.

TABLE 2. DSLAM PCI Card ID Codes

SEEP Version	Device	00h Device ID	02h Vendor ID	44h Subsystem ID	46h Subsystem Vendor ID
Preliminary*	-	0022h	5056h	000Dh	5056h
SP	Unconfigured PLX 9054	9054h	10B5h PLX	2350h DSLAM Core Card Kit	11F8h PMC-Sierra

*/ Some Core Cards may have preliminary SEEP load. Also, the SP version has the Class Code set to 0x0600, for a PCI bridge.

The present version of ID load is described as follows. The 10B5 hex is the PLX registered vendor ID. The 11F8 hex is the PMC-Sierra registered vendor ID. Subsystem ID 2350 hex is unregistered ID for the Core Card Kit.

8.7. Serial EEPROM Load Registers

The PLX 9054 can be initialized to a large extent by reading the data from its serial EEPROM (SEEP) port during initialization. Reading the data from the SEEP is equivalent to directly writing to the 9054 configuration registers through the CPU.

The DSLAM Reference Design Core Card includes a SEEP for this purpose. Table 3 shows the SEEP Load Registers' contents.

TABLE 3. PLX 9054 Serial EPROM Load Registers

SEEP Offset	Description	PLX 9054 Register Bits Affected	Setting
0h	Device ID	PCIIDR[31:16]	9054h
2h	Vendor ID	PCIIDR[15:0]	10B5h
4h	Class Code	PCICCR[23:8]	0600h
6h	Class Code / Revision	PCICCR[7:0] / PCIREV[7..0]	0000h
8h	Maximum Latency / Minimum Grant	PCIMLR[7:0] / PCIMGR[7:0]	0000h
Ah	Interrupt Pin / Interrupt Line Routing	PCIIPR[7:0] / PCIILR[7:0]	0100h
Ch	MSW of Mailbox 0	MBOX0[31:16]	0000h
Eh	LSW of Mailbox 0	MBOX0[15:0]	0000h
10h	MSW of Mailbox 1	MBOX1[31:16]	0000h
12h	LSW of Mailbox 1	MBOX1[15:0]	0000h
14h	MSW of Range for PCI to Local Address Space 0	LAS0RR[31:16]	FFFEh
16h	LSW of Range for PCI to Local Address Space 0	LAS0RR[15:0]	0000h
18h	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 0	LAS0BA[31:16]	0000h
1Ah	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 0	LAS0BA[15:0]	0001h
1Ch	MSW of Mode/DMA Arbitration Register	MARBR[31:16]	0100h
1Eh	LSW of Mode/DMA Arbitration Register	MARBR[15:0]	0000h
20h	MSW of EPROM write Protected Area	PROT_AREA [15:0]	0030h
22h	LSW of Local Miscellaneous Control Register / LSW of Local Bus Big/Little Endian Descriptor Register	LMISC[7:0] / BIGEND[7:0]	0500h
24h	MSW of Range for PCI-to-Local Expansion ROM	EROMRR[31:16]	0000h
26h	LSW of Range for PCI-to-Local Expansion ROM	EROMRR[15:0]	0000h
28h	MSW of Local Base Address (Remap) for PCI-to-Local Expansion ROM	EROMBA[31:16]	0000h
2Ah	LSW of Local Base Address (Remap) for PCI-to-Local Expansion ROM	EROMBA[15:0]	0000h
2Ch	MSW of Bus Region Descriptors for PCI-to-Local Bus Accesses	LBRD0[31:16]	4200h
2Eh	LSW of Bus Region Descriptors for PCI-to-Local Bus Accesses (including local bus width - 32)	LBRD0[15:0]	0043h

SEEP Offset	Description	PLX 9054 Register Bits Affected	Setting
30h	MSW of Range for Direct Master-to-PCI	DMRR[31:16]	0000h
32h	LSW of Range for Direct Master-to-PCI	DMRR[15:0]	0000h
34h	MSW of Local Base Address for Direct Master-to-PCI Memory	DMLBAM[31:16]	0000h
36h	LSW of Local Base Address for Direct Master-to-PCI Memory	DMLBAM[15:0]	0000h
38h	MSW of Local Bus Address for Direct Master-to-PCI I/O Configuration	DMLBAI[31:16]	0000h
3Ah	LSW of Local Bus Address for Direct Master-to-PCI I/O Configuration	DMLBAI[15:0]	0000h
3Ch	MSW of PCI Base Address (Remap) for Direct Master-to-PCI	DMPBAM[31:16]	0000h
3Eh	LSW of PCI Base Address (Remap) for Direct Master-to-PCI	DMPBAM[15:0]	0000h
40h	MSW of PCI Configuration Address register for Direct Master-to PCI I/O Configuration	DMCFGA[31:16]	0000h
42h	LSW of PCI Configuration Address register for Direct Master-to PCI I/O Configuration	DMCFGA[15:0]	0000h
44h	Subsystem ID	PCISID[15:0]	2350h
46h	Subsystem Vendor ID	PCISVID[15:0]	11F8h
48h	MSW of Range for PCI to Local Address Space 1	LAS1RR[31:16]	FFFEh
4Ah	LSW of Range for PCI to Local Address Space 1	LAS1RR[15:0]	0000h
4Ch	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	LAS1BA[31:16]	0000h
4Eh	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	LAS1BA[15:0]	0000h
50h	MSW of Bus Region Descriptors (Space 1) for PCI –to-Local Accesses	LBRD1[31:16]	0000h
52h	LSW of Bus Region Descriptors (Space 1) for PCI –to-Local Accesses	LBRD1[15:0]	0040h
54h	MSW of Hot Swap Control	Reserved	0000h
56h	LSW of Hot Swap Control / Hot Swap Next Capability Pointer	HS_NEXT[7:0] / HS_CNTL[7:0]	4C00h
58h – 100h	Blank	-	FFFFh

An example of the source code for the SEEP. (NM93CS66) is shown below. The bold characters are entries from the above table. The fields 58h to 100h are not highlighted to make it easily readable (those fields are all FFFFh).

```
:020000020000FC
:10000000905410B5060000000000001000000000027
:10001000000000000FFFE0000000000101000000E1
:10002000003005000000000000000004200004316
:10003000000000000000000000000000000000C0
:10004000000000000235011F80000000000000FD
:10005000000000400000400FFFFFFFFFFFFFFFF1C
:10006000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFA0
:10007000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF90
:10008000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF80
:10009000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF70
:1000A000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF60
:1000B000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF50
:1000C000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF40
:1000D000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF30
:1000E000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF20
:1000F000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF10
:10010000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF
:10011000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFEF
:10012000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFDF
:10013000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFCF
:10014000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFBF
:10015000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFAF
:10016000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF9F
:10017000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF8F
:10018000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF7F
:10019000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF6F
:1001A000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF5F
:1001B000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF4F
:1001C000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF3F
:1001D000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF2F
:1001E000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF1F
:1001F000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF0F
:00000001FF
```

8.8. CPLD

The CPLD is used for address decoding and load balancing on the local bus, 8 kHz clock routing, LED control latches, and interrupt logic. The interrupts from each device can be presented to the host CPU on a single read cycle, speeding up interrupt servicing.

8.8.1. Local Bus Memory Map

TABLE 4 shows the local bus memory map.

TABLE 4. Local Bus Memory Map

ADDRESS [16..0]	Description
0x00000 – 0x00A00	S/UNI-APEX registers
0x04000 – 0x04008	CPLD registers for interrupts, LEDs and 8 kHz routing (offset 0x4000)
0x08000 – 0x0A000	S/UNI-ATLAS registers (offset 0x8000)
0x0C000 – 0x0C804	S/UNI-VORTEX-1 registers (offset 0xC000)
0x10000 – 0x10804	S/UNI-VORTEX-2 registers (offset 0x10000)
0x14000 – 0x1420C	S/UNI-DUPLEX registers (offset 0x14000)

Address range for the S/UNI-APEX is 0xA00 as per datasheets. Multiplying register numbers by 4 and adding offset derives address range for all other devices. The address range per each device is the highest specified in the corresponding data sheets for the present chip revisions.
Example: S/UNI-VORTEX highest register 0x201 * 4 = 0x804, with offset → 0xC804;
S/UNI-ATLAS, highest register 0x800 * 4 = 0x2000, with offset → 0xA000.

DSLAM software driver prevents accessing address that is higher than specified in the data sheets per each chip.

Chip select is done with the PCI9054 address LA[16..14], which are bundled with a couple of more bits into LA_SEL<4:0> (as shown on the schematic on page 12). For the above devices, the address ports (registers address) on the devices are wired to the address bus using bits LA<13..2> (directly or through the CPLD). The two least significant bits are ignored, due to a 32-bit long word of four bytes on the address and data bus. Address mapping is necessary to treat all local devices as 32-bit devices on the PCI side. (See section 8.4.) Address to each device is incremented by one bit, with bits LA_SEL[2:0] on the chip address bus.

The CPLD registers 0x04000, 0x4004 and 0x04008 support interrupts, LEDs, and 8 kHz routing. Reprogramming is possible, depending on the designer's needs.

The DSLAM chipset has assigned memory space of up to 0x14FFC (decimal 86012).

8.8.2. CPLD Registers

This section briefly describes CPLD registers. Each register is 16-bit wide.

TABLE 5. Interrupt Register 0x4000

Bit	Type	Function	Default
15	R/W	Reserved	0
14	R/W	Reserved	0
13	R/W	S/UNI-DUPLEX INT Enable	0
12	R/W	S/UNI-VORTEX-2 INT Enable	0
11	R/W	S/UNI-VORTEX-1 INT Enable	0
10	R/W	S/UNI-ATLAS INT Enable	0
9	R/W	S/UNI-APEX INTLO Enable	0
8	R/W	S/UNI-APEX INTHI Enable	0
7	R/W	Reserved	0
6	R/W	Reserved	0
5	R	S/UNI-DUPLEX INT	0
4	R	S/UNI-VORTEX-2 INT	0
3	R	S/UNI-VORTEX-1 INT	0
2	R	S/UNI-ATLAS INT	0
1	R	S/UNI-APEX INTLO	0
0	R	S/UNI-APEX INTHI	0

Bits 8 through 13 can be set to logic *1*, enabling the corresponding interrupt. If enabled, then any active interrupt from the VORTEX chipset pulls low the interrupt output pin on the CPLD, which is connected to pin LINTB on the PCI9054. Bits 0 through 5 are set to logic *1* asynchronously by interrupt lines from each device.

NOTE: The CPU sets bits 8-13. The CPLD logic sets bits 0-5 (based on connected VORTEX chipset interrupt lines) allowing a single read from the CPLD to determine device interrupt.

Example of possible LED assignment is shown in TABLE 6 below.

TABLE 6. LED Register 0x4004

Bit	Type	Function	Default	Notes	
15	R/W	Reserved	0		
14	R/W	Reserved	0		
13	R/W	Operating Mode – Status LED (yellow)	0	LED D4	Status
12	R/W	Reset and microprocessor interface (red)	0		
11	R/W	S/UNI-VORTEX-1 LCD	0	LED D5	Line 1-8
10	R/W	S/UNI-VORTEX-1 LCD	0		
9	R/W	S/UNI-VORTEX-1 LOS	0		
8	R/W	S/UNI-VORTEX-1 LOS	0		
7	R/W	S/UNI-VORTEX-2 LCD	0	LED D6	Line 9-16
6	R/W	S/UNI-VORTEX-2 LCD	0		
5	R/W	S/UNI-VORTEX-2 LOS	0		
4	R/W	S/UNI-VORTEX-2 LOS	0		
3	R/W	S/UNI-DUPLEX Port-2 LCD	0	LED D7	WAN
2	R/W	S/UNI-DUPLEX Port-2 LOS	0		
1	R/W	S/UNI-DUPLEX Port-1 LCD	0		
0	R/W	S/UNI-DUPLEX Port-1 LOS	0		

Bits 0 through 11 set red LEDs on the front panel for loss of signal (LOS) or loss of cell delineation (LCD) on the corresponding LVDS receivers. Alarms have to be detected by the host processor through interrupts and written to the CPLD register 0x4004. If the Core Card is in operating mode, bit 13 may be written 1/0 at about two times per second. If the Core Card is in stand-by mode, bit 13 may be *1* and *Status* LED is lit steadily. If the Core Card is malfunctioning, bit 13 is *0* and LED is turned off.

NOTE: VORTEX Chipset Driver does not have the alarm LED control implemented. Also, on reset, the internal CPLD programming turns *on* all LEDs to for visual inspection, and later, the software script should turn the LEDs *off*. Check LED behavior for programming.

Designer may program LEDs as needed.

TABLE 7. 8 kHz Routing Register 0x4008

Bit	Type	Function	Default
15	R/W	Reserved	0
14	R/W	Reserved	0
13	R/W	Reserved	0
12	R/W	Reserved	0
11	R/W	Reserved	0
10	R/W	Reserved	0
9	R/W	Reserved	0
8	R/W	Reserved	0
7	R/W	Reserved	0
6	R/W	Reserved	0
5	R/W	Reserved	0
4	R/W	Reserved	0
3	R/W	Reserved	0
2	R/W	Clock to PLL [1]	0
1	R/W	Clock to PLL [0]	0
0	R/W	PLL output to all TX8K	0

Bit 0 = 0. All 8 kHz inputs TX8K on S/UNI-VORTEX-1, S/UNI-VORTEX-2, and S/UNI-DUPLEX are fed from the J65 header 8 kHz input. No PLL in the signal path.

Bit 0 = 1. All 8 kHz inputs TX8K on S/UNI-VORTEX-1, S/UNI-VORTEX-2, and S/UNI-DUPLEX are fed from the 8 kHz PLL. The source of the signal to the PLL input is determined with bits 1 and 2.

Bit-1 = 0 and **bit-2 = 0.** Clock to PLL from the S/UNI-DUPLEX pin RX8K
Bit-1 = 1 and **bit-2 = 0**. Clock to PLL from the S/UNI-VORTEX-1 pin RX8K
Bit-1 = 0 and **bit-2 = 1.** Clock to PLL from the S/UNI-VORTEX-2 pin RX8K
Bit-1 = 1 and bit-2 = 1, reserved.

The 8 kHz output header J72 is fed with 8 kHz from J65 if Bit0 = 0 or from PLL output if Bit0 = 1.

Notes on Register Bits:

1. Writing values into unused register bits has no effect. To ensure software compatibility with future versions of the product, unused register bits should be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero, therefore, unused register bits should be masked off by the software when they are read.

2. All configuration bits that can be written into can also be read back. This allows the processor that controls the Core Card to determine the programming state of the block.

3. Writeable register bits are cleared to logic zero on reset, unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect the CPLD operation, unless otherwise noted.

8.8.3. Alarms And Interrupts

Interrupts from each device are fed into the CPLD, and are derived by the host processor card through the cPCI bridge INTA# line. The interrupt-causing device can be determined by a single read of the CPLD register instead of five reads from the DSLAM chipset. Alarms can be read directly from devices also.

8.8.4. 8 kHz Channel

Figure 6 shows how the CPLD supports routing of the 8 kHz signal to and from any port.

8.8.5. Address Decoding and Chip Enable

The CPLD supports dynamic (no latching) address decoding and generation of *chip enable* signals. Those signals are routed to each chip individually.

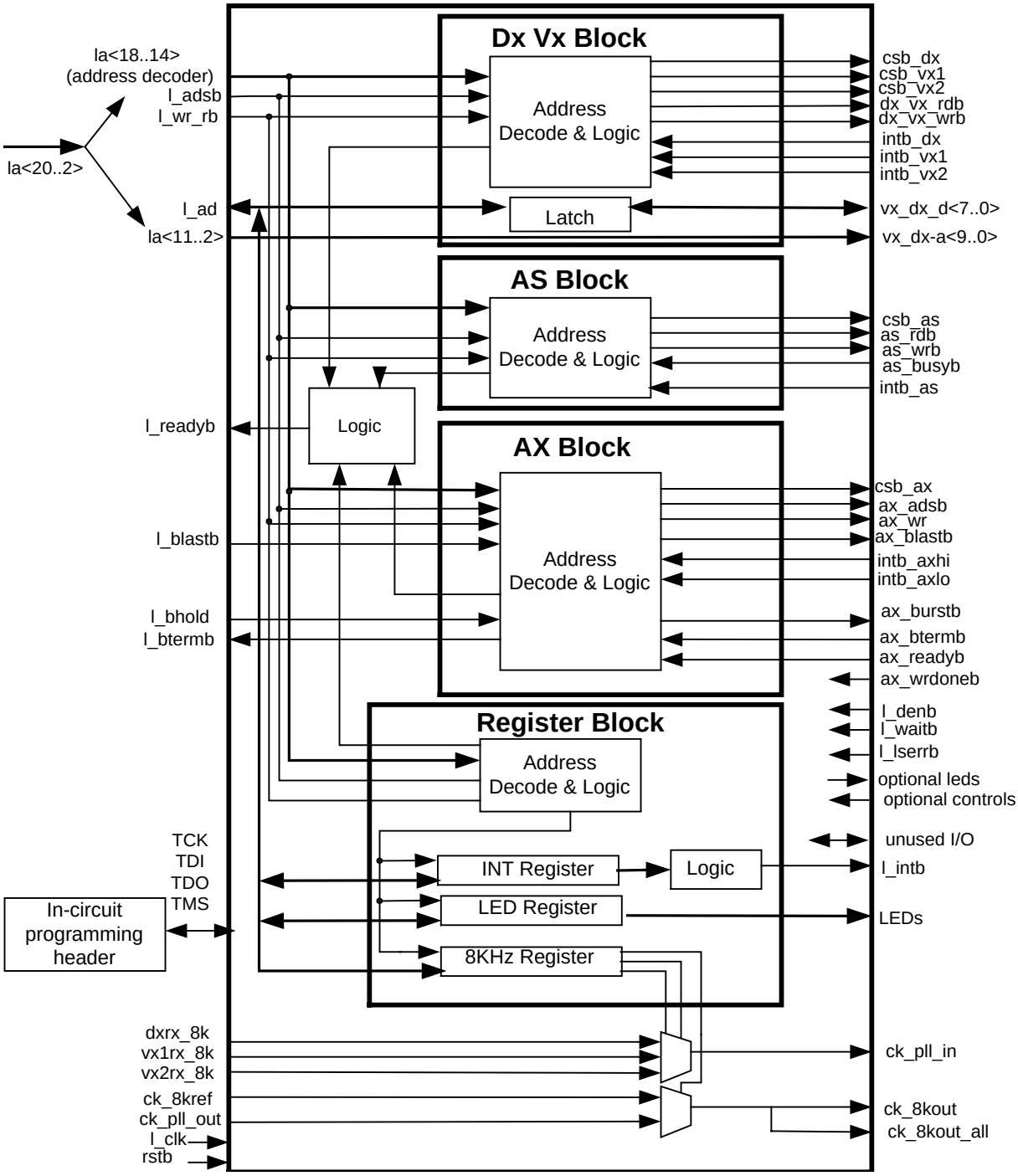
8.8.6. CPLD Type

The CPLD used in this Reference Design is the Xilinx XC95288 with 288 microcells (registers). The data bus width is 32 bits for the S/UNI-APEX, 16 bits for the S/UNI-ATLAS and CPLD, and 8 bits for the S/UNI-VORTEX and S/UNI-DUPLEX. For a preliminary VHDL source code for the CPLD, see Section 0.

8.9. CPLD Block Diagram

Figure 17 shows the CPLD block diagram.

Figure 17. CPLD Block Diagram



9. CONNECTORS ON CORE CARD

9.1. CPCI Connectors

9.1.1. J1 on Core Card

The J1 connector, that mates with P1 on the 3U high cPCI backplane, provides power to the Core Card. The connector provides the PCI bus interface, which is connected to the PCI9054 bridge.

The J1 connector has to provide the hot-swap capability. The connector senses the staggered pins on insertion and removal of the Core Card from the DSLAM-shelf. The serial MOSFET transistors control the power rails.

Connector J1 follows the pinout recommendation found in documents [18] and [19].

9.1.2. J2, J3, and J4 on Core Card

The J2, J3, and J4, the cPCI-scheme connectors, are not populated on the Core Card.

The J3 connector on a card that is placed into the DSLAM development shelf may collide with a metal rail that runs across the LVDS-backplane.

9.1.3. J5 on Core Card

System Design document [1] shows the J5 pinout.

The J5 connector terminates LVDS from the S/UNI-VORTEX-1 and S/UNI-DUPLEX. Those ports provide an interface to the WAN and Line Cards through the LVDS-backplane.

NOTE: All connectors that mate with the backplane follow the cPCI backplane scheme. The Core Card uses J1 and J5 connectors only. The J2, J3, and J4 names are retired to avoid confusion and to bring uniform connector naming.

9.2. LVDS Interface on the LVDS-backlane

The LVDS interface to the LVDS-backplane is provided through the J5 connector exclusively. The Core Card mates with the custom LVDS-backplane at slot 5 and slot 6.

9.3. LVDS Interface on the Front Panel

The LVDS interface on the front panel is provided through the IEEE 1394 FireWire connectors. Total of eighteen connectors with AC coupling allows access to high-speed ports at S/UNI-VORTEX-1, S/UNI-VORTEX-2 and S/UNI-DUPLEX. See section 10 *LVDS INTERFACE* for more information.

9.4. CPLD Programming Interface on J34

The CPLD programming interface is provided through the J36 header connector. For more information about connections, see the schematics on page 13

Additional Xilinx programming cable with a programming head is required for downloading code into the CPLD. The programming software can be downloaded from the Xilinx web site

WARNING: Take caution while handling cables and maintaining boards. Most interfaces may not have ESD discharge protection.

9.5. 25 MHz Output on J45

The recovered clock on the high speed LVDS is divided by eight, and it is output at the S/UNI-DUPLEX pin E11 RCLK (at TTL level). The J45 connector is for test purposes only.

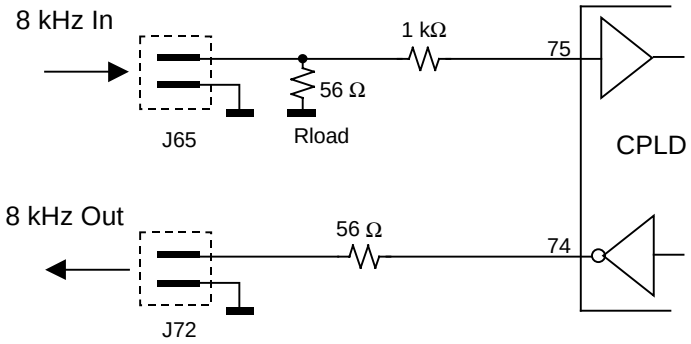
9.6. RESET Header J64

The J64 header allows hardware reset to all VORTEX chipset devices (excluding PCI9054). For normal operation a shunt must be placed on pins 1 and 2. When the strap is placed on J64 pins 2 and 3, the RSTB local reset line to is asserted. That also forces HEALTHY# pin *high*.

9.7. 8 kHz Interface on J65 and J72

The 8 kHz interface on the Core Card is accessible on the board only. Header connectors are provided, with J65 for 50 ohm TTL level input and J72 for TTL level output (+3.3 V CMOS logic equivalent). Figure 18 shows the 8 kHz interface Core Card.

Figure 18. 8 kHz Interface



9.8. JTAG Interface on J66

The JTAG interface on the Core Card is accessible on the board through the header connector J66. The JTAG daisy-chain is connected for the VORTEX chipset only. The JTAG interface is provided but not tested. For more information about the connections, see the schematics on page 12.

9.9. Mictor Connectors J70 and J71

The purpose of the J70 and J71 high density Mictor connectors is to allow board troubleshooting and CPLD development. The connectors are optional and may not be populated on all boards.

9.10. Clock Control Header J73

The J73 header must be open for normal operation. This header shuts down 25 MHz local bus clock. Do the strapping with the global reset on J64, while the CPLD is being programmed. Make sure the strap is removed after programming. (The Core Card doesn't misbehave during CPLD programming, even with the local bus 25 MHz clock running and without the RSTB asserted.)

9.11. Optional Reset to CPLD Header J74

The purpose of J74 is disconnecting the optional global reset to CPLD. The header is not populated.

9.12. Ejector Handle Switch Header TP115

Molex header TP115 allows the connection of the ejector micro-switch cable with the board and PCI9054.

The microswitch toggles when the front panel ejector changes position, and notifies the PCI9054 and the host CPU about the status change.

9.13. Miscellaneous Test Points

The Core Card allows the placement of additional headers on multiple test points, that are distributed throughout the board. Those headers may not be populated.

NOTE: the TWRENB line is wrongly labeled as TPRTY. See schematic page 8. The TPRTY is at TP86.

10. LVDS INTERFACE

The connector pinout and interface circuit is briefed in this section.

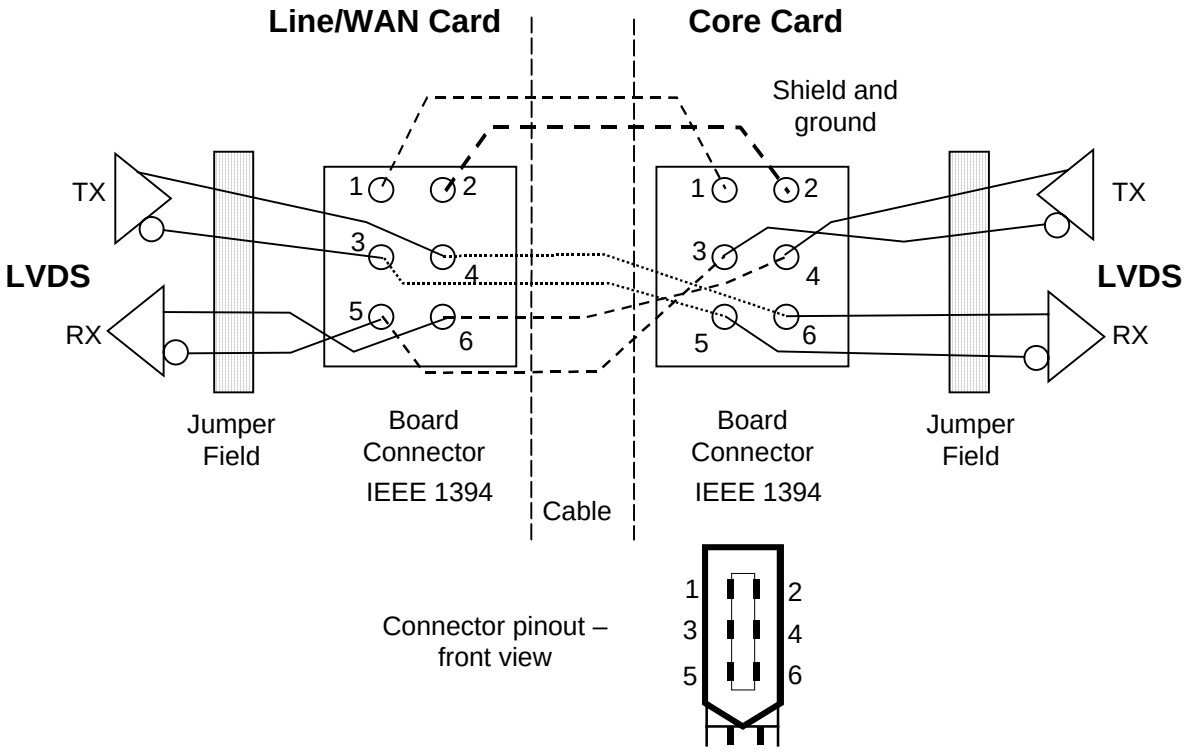
All connectors that mate with the backplane follow the cPCI backplane population option — J1, J2, J3, J4, and J5. The Core Card uses J1 and J5 connectors only.

The LVDS interface to the custom LVDS-backplane is provided exclusively through connector J5. The Core Card mates with the custom LVDS-backplane at slot 5 and slot 6.

10.1. LVDS Front Panel Interface

The IEEE 1394 cable is wired with pins swapped on each end. This type of wiring requires matching pinouts on the Core Card and the Line/WAN Card. Figure 19 shows the LVDS connector pinout on the DSLAM cards.

Figure 19. LVDS Pinout on DSLAM Cards



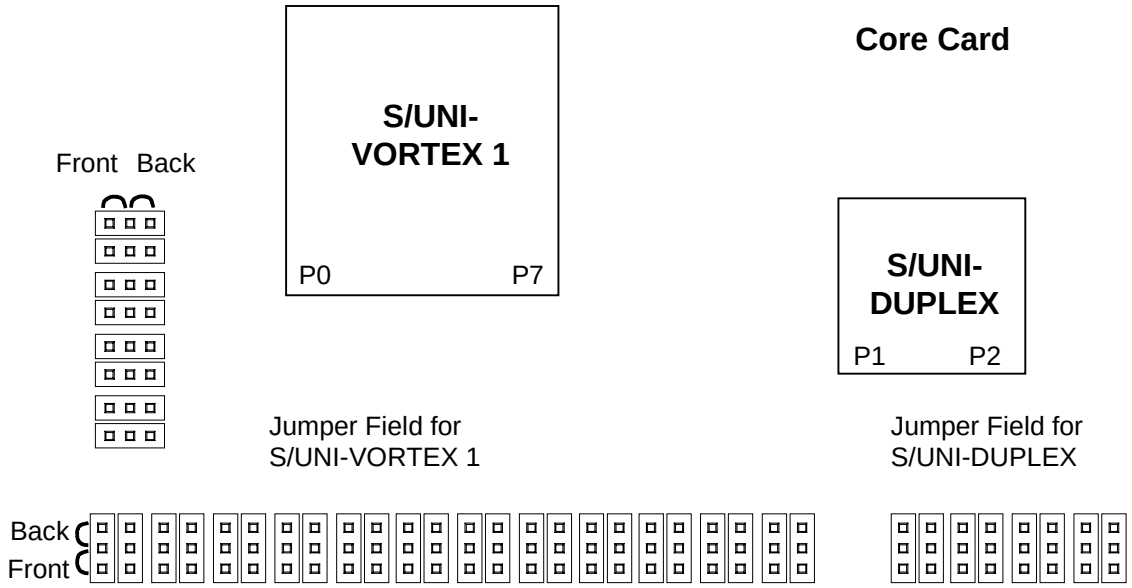
The pinout is functional only. The physical interface has serial capacitors 1.0 uF (or 0.22 uF) on input and output. Inputs are biased with the resistive divider and

line termination. Capacitors are permanently soldered without the bypass option. The Line and WAN Cards have transformer coupling, which can be modified for capacitor coupling through de-soldering only. Jumper fields allow for a front panel or backplane interface.

The total count of the LVDS interfaces on the Core Card is eighteen. The total count of connectors occupies the entire front panel, preventing placement of other connectors (like 8 kHz stratum clock). The S/UNI-VORTEX-1 port P[0] through P[7] and S/UNI-DUPLEX port P1 and P2 can be wired to the front panel and to the LVDS-backplane through the *Jumper Field*. The S/UNI-VORTEX-2 port P[0] through P[7] are wired to the front panel only. The LVDS copper lines routing was shown earlier in Figure 5.

Figure 20 shows the LVDS header straps.

Figure 20. LVDS Header Straps



A total of 40 shunts are needed for all LVDS ports. Headers and shunts are on a 2 mm grid.

ESD Protection on LVDS Ports

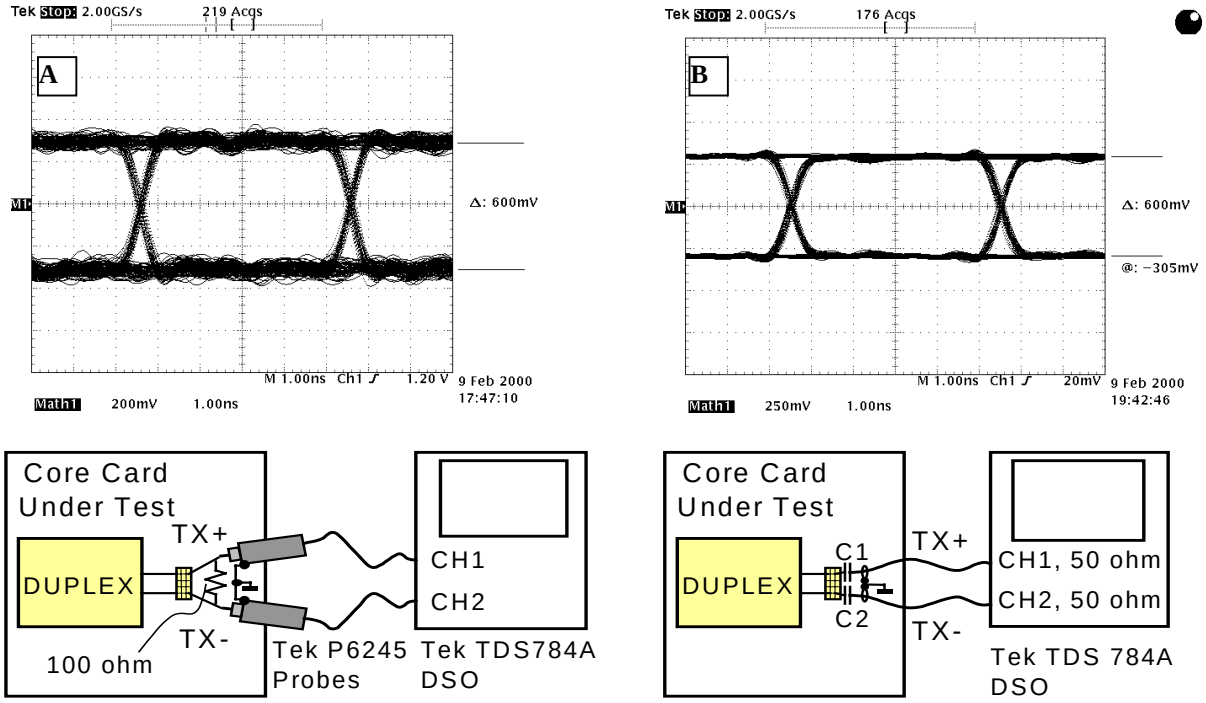
The LVDS is inherently unprotected for ESD with capacitor coupling on the Core Card interface. The Line and WAN Cards may have transformer coupling that withstand ESD discharge.

Take caution when handling cables and maintaining boards.

10.2. LVDS Eye Pattern at Jumper Field Tests

We have investigated LVDS signal integrity, and the results are presented below. The eye pattern on the transmitted LVDS signal is captured with the TEK TDS784 oscilloscope in differential mode. The signal was connected with two setups. The first one used high frequency probes, and the second one used short 50 ohm cables. Figure 21 shows the test results.

Figure 21. Wave Shapes with a Single Active LVDS Transmitter



Graph A shows S/UNI-DUPLEX LVDS transmitting the waveform at the header connector, measured with high frequency oscilloscope probes. The waveform is terminated with the 100 ohm resistor, and the signal is probed with Tek P6245, <1 pF, 1 Mohm, 1.5 GHz probes.

Graph B shows the waveform obtained by direct connection with 50 ohm coaxial cables into 50 ohm oscilloscope inputs. Serial capacitors must be inserted, because direct termination into 50 ohm to ground overloads the transmitter and corrupts the LVDS signal. Both cases use the differential math function CH1–Ch2.

Signal integrity measured with oscilloscope probes is inappropriate for this application. The signal shows excessive *waves* or back reflections, which may lead to a false conclusion about signal quality. The correct measurement is to terminate the signal directly into the oscilloscope using short coaxial cables and AC coupling.

Transmitted data pattern is of random type with very low baseline wander, as needed for signal integrity tests.

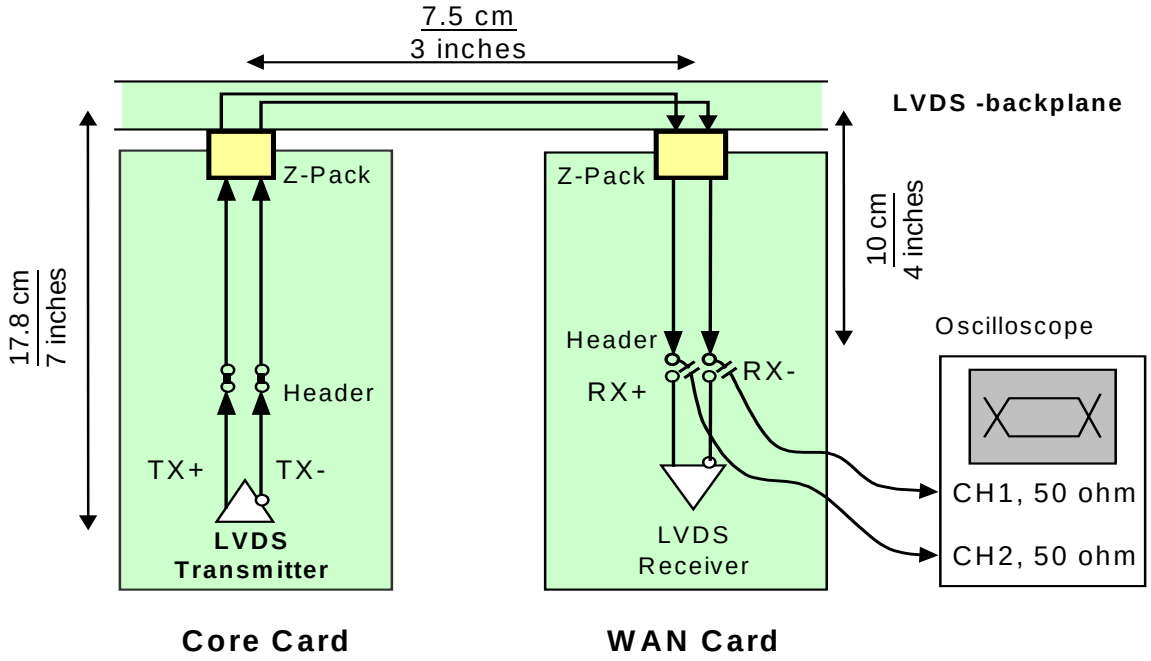
The waveforms look different with transformer coupling, as implemented for the Line Card and WAN Card.

10.3. LVDS Eye Pattern over LVDS-Backplane Tests

The LVDS interface to the custom LVDS-backplane is provided exclusively through connector J5. The Core Card mates with the LVDS-backplane at slot 5 and slot 6.

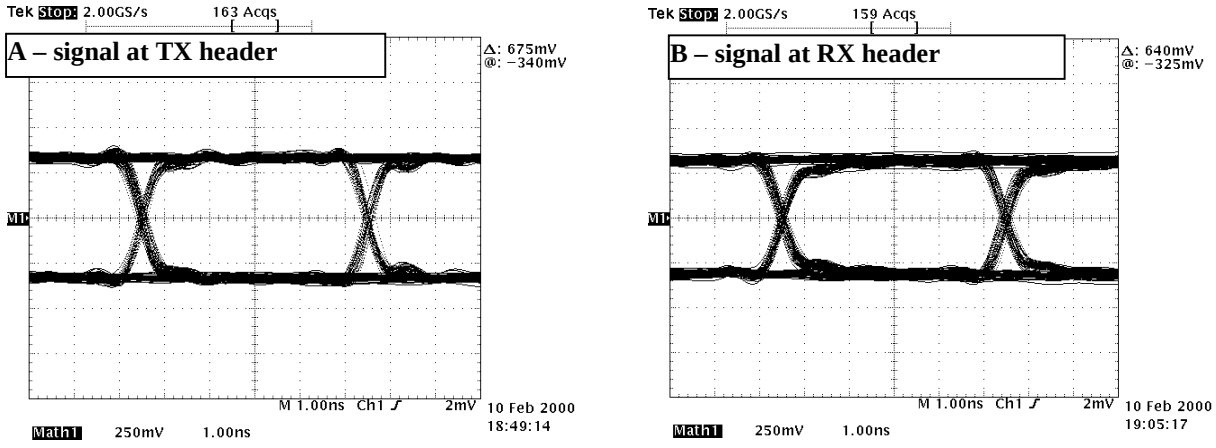
In the LVDS backplane test, the Core Card is placed into the DSLAM test shelf with the LVDS-backplane, and eye pattern is measured at the header on the Core Card and then on the WAN Card. The Core Card is placed at slot 5 and the WAN Card at slot 8. Figure 22 shows the total length of trace, which is about 35.5 cm or 14 inches.

Figure 22. LVDS Over Backplane Test Connections



The signal goes through two header connectors and two Z-pack, 2 mm cPCI connectors, before it is connected with a short 50 ohm coaxial cable into the 50 ohm oscilloscope inputs. AC coupling is maintained with serial capacitors. Figure 23 shows eye patterns at the transmitter header and at the receiver header.

Figure 23. LVDS at Core Card and Line Card with LVDS backplane



The LVDS-backplane attenuates the LVDS signal from 675 mV to 640 mV, which results in 0.5 dB (or 5 %) amplitude attenuation. Some near-edge distortions are

amplified and are more visible after running the signal over the backplane. The overall signal is of a very good quality and allows easy reclocking. A possible reason for back reflections is a small miscalculation of the differential pair impedance. The board was designed with 50 ohm per trace, as it would be a single line. Due to the coupling effect, the virtual impedance of the pair is changed and is not 100 ohm any more. Also, the differential pair goes into two coax cables, creating additional impedance discontinuity. The measurement techniques need further evaluation.

NOTE: Double AC termination on the LVDS path may cause baseline wander if not designed properly. Excessive baseline wander together with long cables may cause bit errors. Designers may investigate solution with AC coupling on one card only, or use large capacitor coupling – about 1 uF. Also, metallic loopback executed for test and troubleshooting is very susceptible to double AC coupling and may cause misleading data corruption. With metallic loopback the LVDS data goes four times through AC coupling aggregating baseline wander problem.

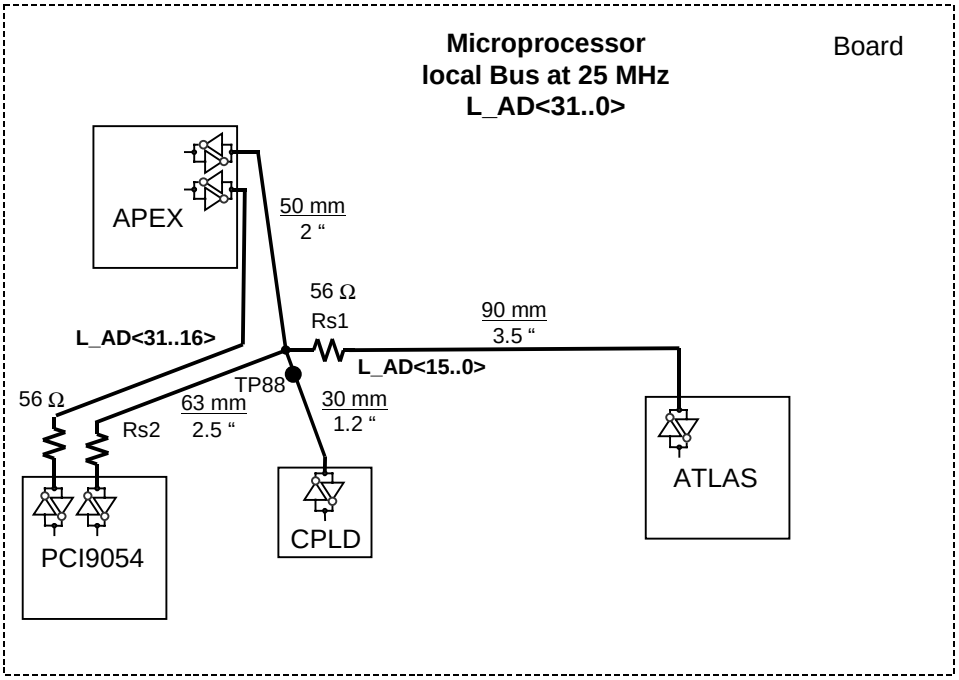
11. BUS TERMINATION EXAMPLES

This section briefly describes the bus termination method on various buses that are present on the Core Card. Proper digital line termination is critical for signal integrity and timing. Termination may prevent data corruption caused by a large signal overshoot. The overshoot may create current flow into silicone and internal silicone crosstalk, which is very difficult to detect. See document [5] for more on signal integrity.

11.1. Microprocessor Bus Termination

Figure 24 shows the local microprocessor bus termination.

Figure 24. Microprocessor Bus Termiantion



The measurements, done on the Core Card board Rev. 1, show a very large overshoot on the signal edges. After reviewing termination options, it was determined that placing the termination resistor, Rs1, at the L_AD<15..0> bus joint towards the longest branch at the S/UNI-ATLAS was optimal. Placement was based on signal integrity simulation and verified through a test. The second resistor, Rs2, was already placed next to the PCI9054 and is optional. The upper half, L_AD<31..16>, connects between PCI9054 and S/UNI-APEX only, and it has the Rs2 termination. The termination Rs1 placement at the central T-joint of

the bus is due to the bi-directional nature of the bus, where any device can drive the digital line.

Figure 25 shows examples of the bus signal.

Figure 25. Examples of Signal Integrity on uP Bus

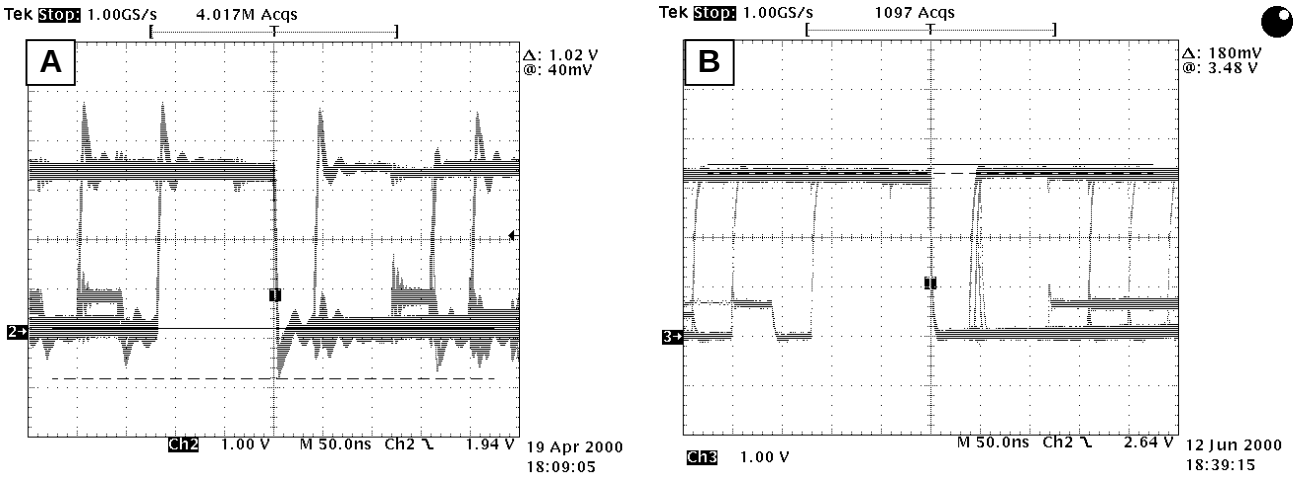


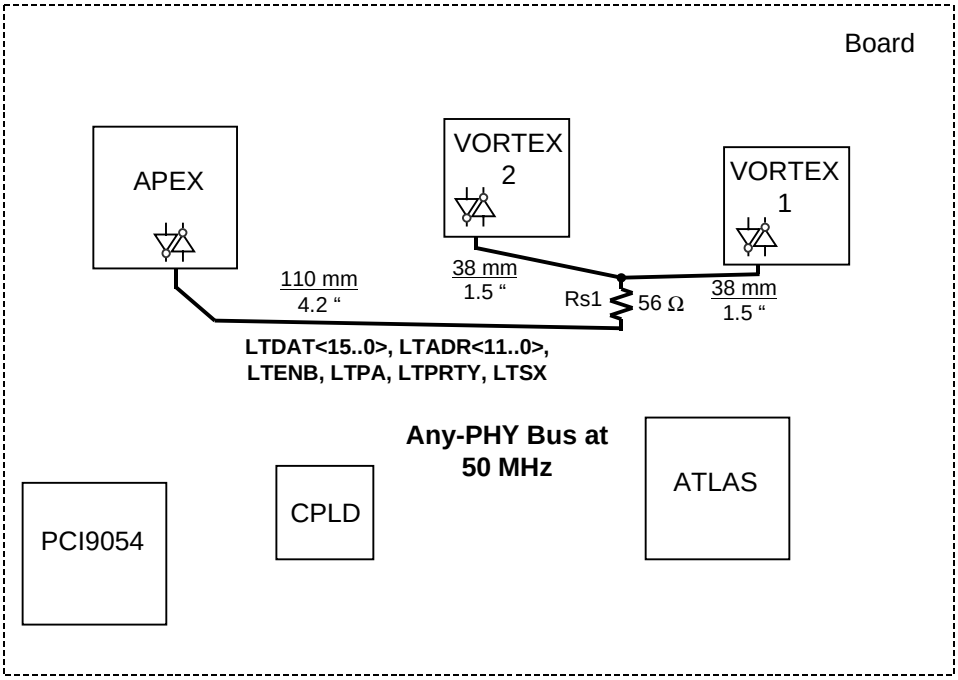
Figure A shows the bus signal without termination resistors. Figure B shows the bus signal, L_AD<0>, measured on TP88 with the termination resistors distributed as presented in Figure 24 earlier. Signal overshoot reaches over one volt on both the positive and negative edges on the non-terminated bus. Serial termination resistors completely eliminate the overshoot.

It is strongly recommend to have proper termination resistors on the microprocessor bus. It is common practice to terminate the Utopia, Scy-PHY, and RAM buses and to leave the microprocessor bus non-terminated. Usually, the microprocessor bus is physically the largest one on the board, reaching throughout all major components on the PCB. With edges in the nanosecond range, back reflections can reach well above clamping diode range, causing the uncontrolled current flow into silicone. We observed in our lab that a significant overshoot causes data corruption that was very difficult to troubleshoot. In the worst case scenario, board redesign with serial termination resistors, is the only solution.

11.2. Downstream Any-PHY Bus Termination

Figure 26 shows the Any-PHY bus termination.

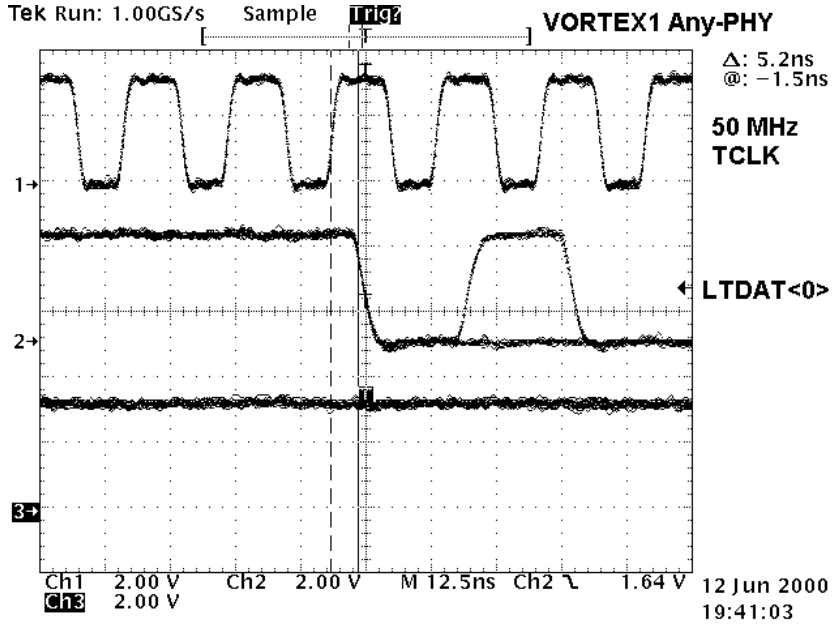
Figure 26. Any-PHY Bus Termiantion



Signal simulation, done prior to the board layout, helped to find the best position for the termination resistor. Simulation pointed to T-joint as the optimal placement for the resistor. Both directions of data flow have the same T-joint termination placement.

Figure 27 (below) shows an example of signal integrity on LTDAT<0> at the S/UNI-VORTEX-1.

Figure 27. Example of Signal Integrity Downstream at VORTEX-1

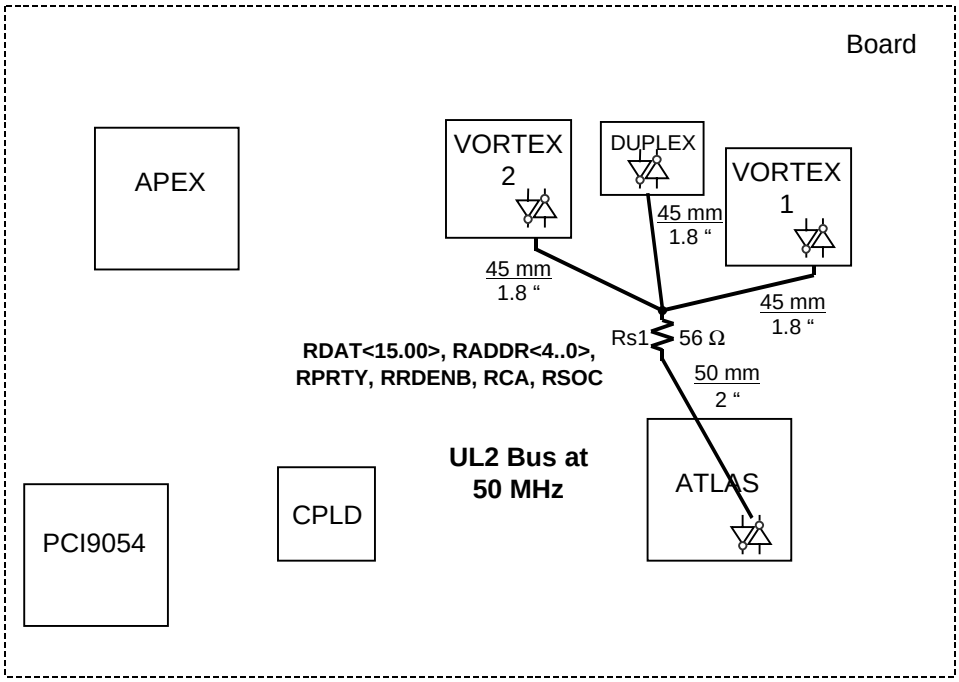


The timing shows about 5.2 ns margin on hold time, while writing data to the S/UNI-VORTEX-1 on Any-PHY bus.

11.3. Upstream/Downstream UL2 Bus Termination

Figure 28 shows the upstream/downstream UL2 bus termination with the S/UNI-VORTEX1, S/UNI-VORETEX2, S/UNI-DUPLEX, and S/UNI-ATLAS.

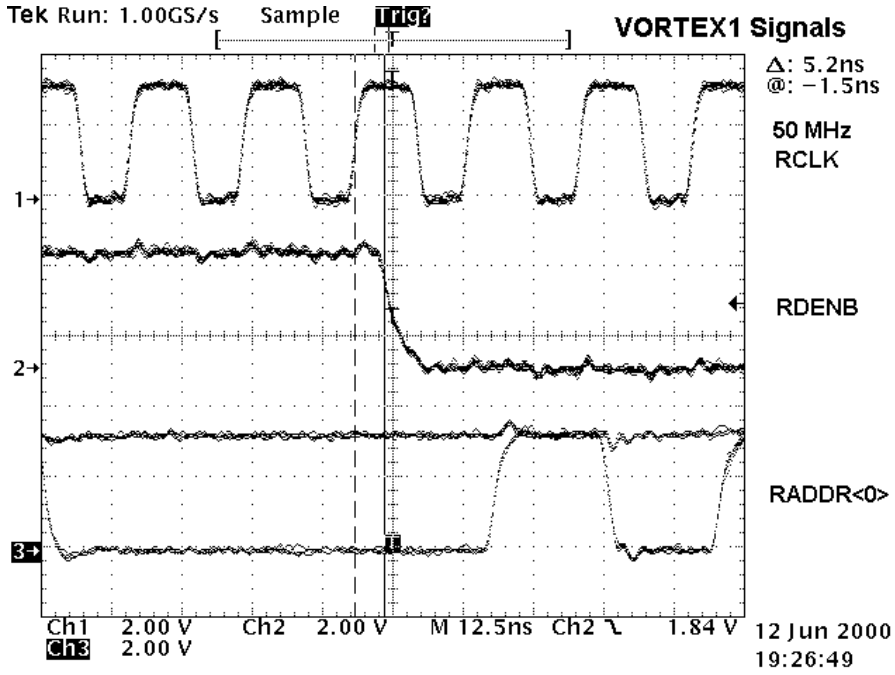
Figure 28. Upstream/Downstream UL2 Bus Termination



The signal simulation shows T-joint as the optimal placement for the serial termination resistor. The simulation was done before board layout. Both directions of the data flow have the same T-joint termination placement. The best solution for the split trace length is to keep it symmetrical. In this case, the branches are at about 45 mm (or 1.8 inch) each.

Figure 29 shows an example of signal integrity on LTDAT<0> at the S/UNI-VORTEX-1.

Figure 29. Example of Signal Integrity Upstream at VORTEX-1

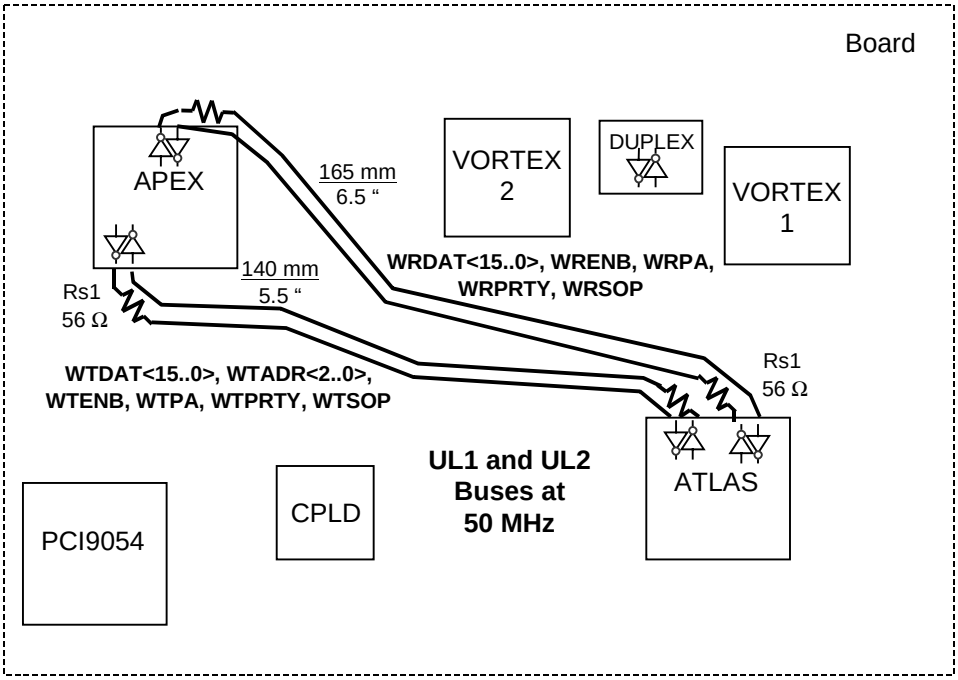


The timing shows about 5.2 ns margin on hold time on RDENB. Also, the appropriate timing margin exists on the RADDR<0>. This is the SCY-Phy/UL2 bus at the S/UNI-VORTEX-1.

11.4. S/UNI-APEX – S/UNI-ATLAS Bus Termination

Figure 30 shows the UL1 and UL2 buses, between the S/UNI-ATLAS and S/UNI-APEX, that are terminated with serial resistors.

Figure 30. S/UNI-APEX – S/UNI-ATLAS Bus Termiantion

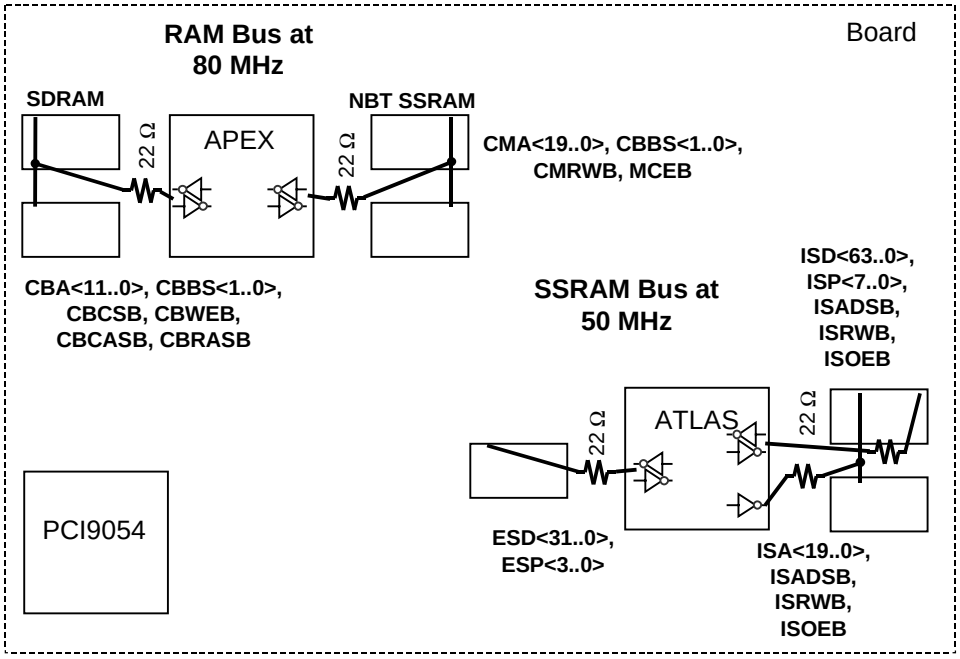


The signal simulation shows the best placement near the source of the digital signal. The simulation was done before board layout.

11.5. RAM Bus Termination

Figure 31 shows an example of the S/UNI-APEX and S/UNI-ATLAS RAM bus termination.

Figure 31. RAM Bus Termiantion

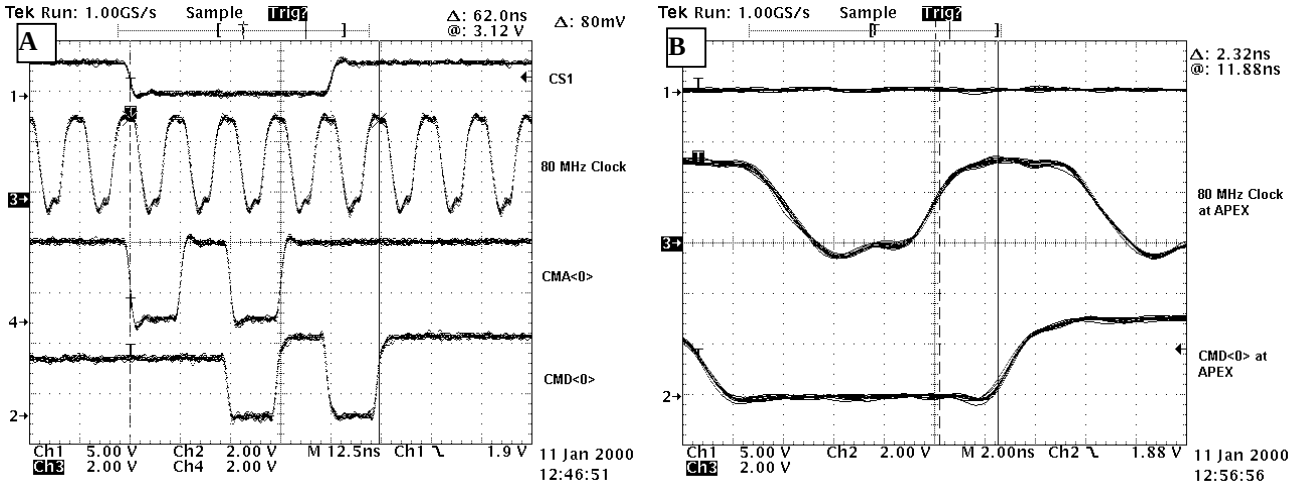


Due to space limitations, the termination resistors are placed at the layout convenience and may not be at the best termination position. Typically, address lines and control lines connected to more than two inputs are placed with termination resistor near the signal source. The S/UNI-ATLAS has serial resistors at the data lines ESD<31..0>, ESP<3..0>, ISD<63..0>, and ISP<7..0> that connect point-to-point only, due to observed overshoots on the data edges.

The following pages provide examples of the RAM bus signal captured with a digital oscilloscope.

Figure 32 shows the waveforms at the S/UNI-APEX and the NBT SSRAM.

Figure 32. Waveforms at S/UNI-APEX at 80 MHz

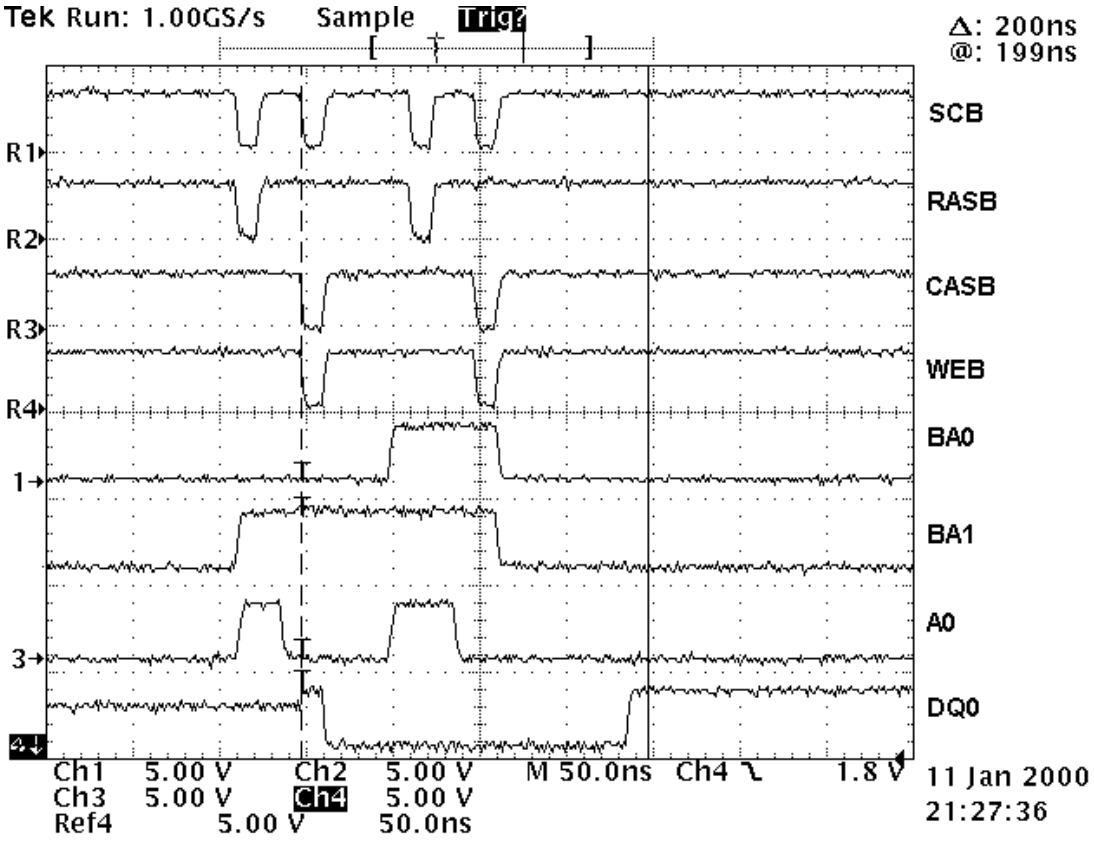


Graphs A and B show curves that are derived through accumulation of ten consecutive reads from the ZBT SSRAM. The signal integrity is appropriate for this interface. The timing margin, shown in graphB, at about 2.3 ns leaves plenty of room for 0.7 ns hold time specified in the S/UNI-APEX data sheets.

Some room on the signal integrity improvement exists on clock waveforms. Other type of buffer and termination resistors may help reduce the overshoot.

Figure 33 shows the waveforms at the S/UNI-APEX and the SDRAM.

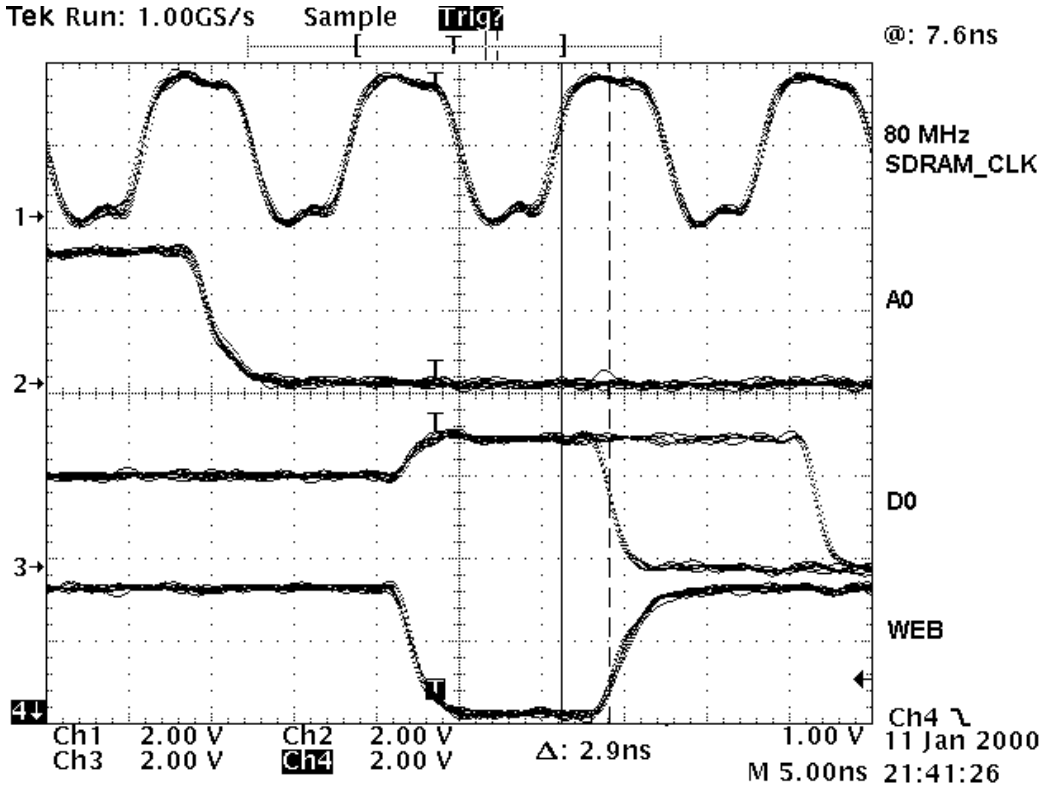
Figure 33. Waveforms at SDRAM at 80 MHz



The trace descriptions (next to the right edge of the graph above) apply to the SDRAM pinout shown on the Core Card SDRAM schematics. The clock signal is not shown in the above figure. The oscilloscope captured digital signals show 16 consecutive write cycles to the SDRAM executed by the S/UNI-APEX. The DQ0 trace between 200 ns cursors shows the binary data pattern 1000000000000001 written to the SDRAM.

Figure 34 shows the zoomed pattern with clock and timing margins and also shows the waveforms at the S/UNI-APEX and the SDRAM.

Figure 34. Waveforms at SDRAM at 80 MHz



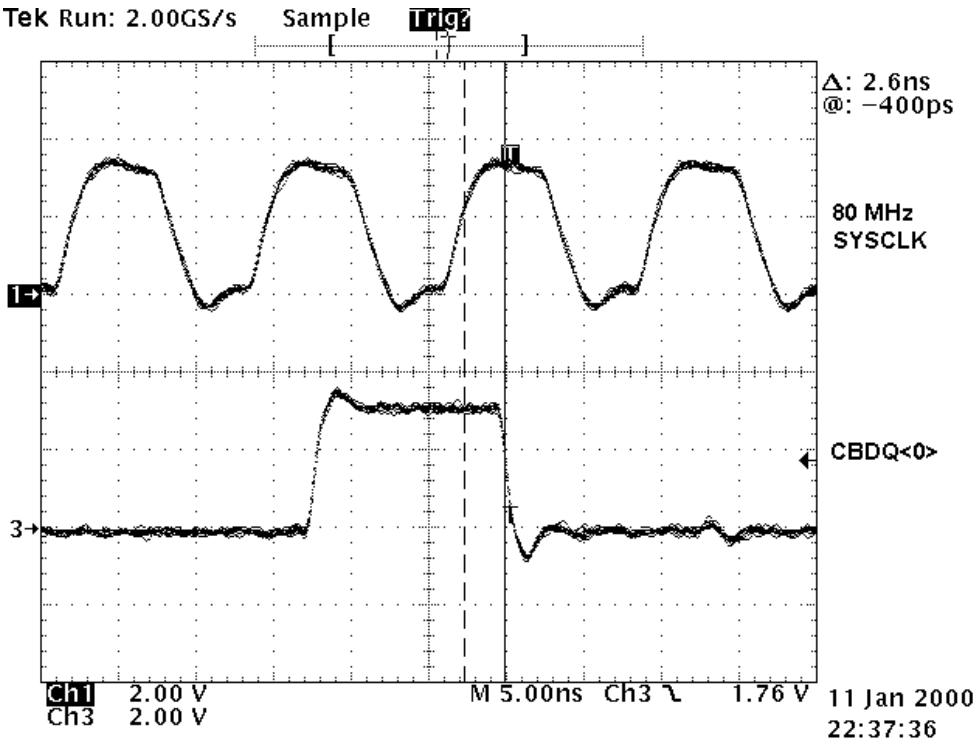
The digital lines shown above are:

- A0 – address to SDRAM
- D0 – data to SDRAM
- WEB – write enable to SDRAM.

The oscilloscope is triggered with the WEB signal. The timing shows about a 2.9 ns margin that is enough for the 1.0 ns hold time for the 100 MHz SDRAM (as specified in the Micron™ data sheets).

Figure 35 shows the data flowing from the SDRAM to the S/UNI-APEX.

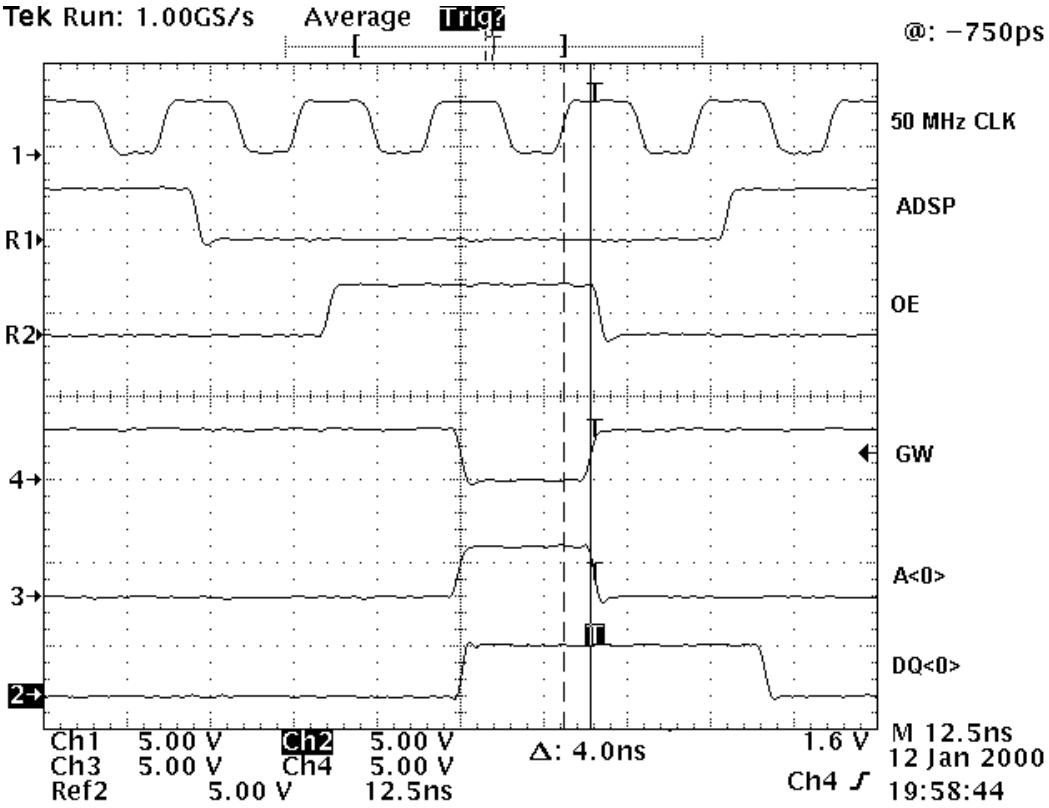
Figure 35. Waveforms at S/UNI-APEX at 80 MHz



The digital line, CBDQ<0>, is the data at the S/UNI-APEX coming from the SDRAM. The clock at the S/UNI-APEX pin SYSCLK is about 2.6 ns ahead of the data, leaving enough margin, with a 0.7 ns hold time specified in the S/UNI-APEX data sheets.

Figure 36 shows the write to SSRAM (from the S/UNI-ATLAS). The interface runs at 50 MHz.

Figure 36. Waveforms at SSRAM at 50 MHz



The figure shows digital signals captured during a single write to SSRAM, executed by the S/UNI-ATLAS. The signal integrity is appropriate for this interface. The timing margin at SSRAM is about 4.0 ns, which leaves plenty of room for the 0.5 ns hold time specified in the SSRAM data sheets.

12. HARDWARE

This section briefly introduces some hardware issues related to the Core Card.

12.1. Card Form

The Core Card form factor complies with the PICMG 2.0 Revision 2.1 CompactPCI standard described in document [18].

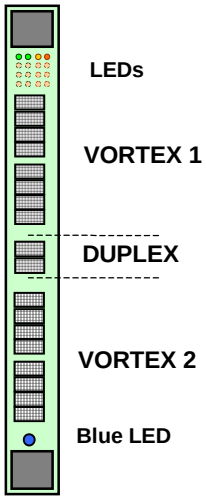
The Core Card form factor complies with the *Hot Swap Specification*, PICMG 2.1 Revision 1.0 standard, described in document [19].

12.2. Front Plate on Core Card

The front plates on the Core Card have dimensions specified in the cPCI document [18].

Figure 37 shows an example of the Core Card front plate.

Figure 37. Front Plate for Core Card



Core Card Front Plate

The Core Card is equipped with 18 IEEE 1394 connectors. The top eight connectors support the S/UNI-VORTEX-1 LVDS. The center pair supports the S/UNI-DUPLEX LVDS. The lower eight connectors support the S/UNI-VORTEX-2 LVDS.

The top four rows of the LEDs show the basic status of the Core Card. The blue LED supports software action when the card is inserted and removed.

The aluminum front plates are labeled with silkscreen. Labels identify the connectors, LEDs, card type, and manufacturer (PMC-Sierra, Inc.).

12.3. LEDs On the Front Plate

The DSLAM Cards are equipped with a set of LEDs. The basic set of four LEDs provides visual information about power lines and the basic condition of the microprocessor interface to all components. The basic LEDs are:

- +5 V, green – indicates a presence of +5 V
- +3.3 V, green – indicates a presence of +3.3 V
- uP, red – may not be implemented in the Chipset Driver applications routines. The preferred functionality is that *ON* indicates trouble at the uP (power-up boot).
- Status, yellow – is not implemented in Chipset Driver. The preferred functionality is that *flashing* indicates an operating Core Card, *steady* indicates a hot stand-by Core Card, and *turned off* indicates a malfunctioning Core Card. The LED flashes two times per second.

The preferred functionality for additional red LEDs is not implemented in the Chipset Driver. The LEDs are intended to indicate a loss of signal (LOS) and a loss of cell delineation (LCD) on the S/UNI-DUPLEX (from the WAN Card) interface. Possible alarms are described as:

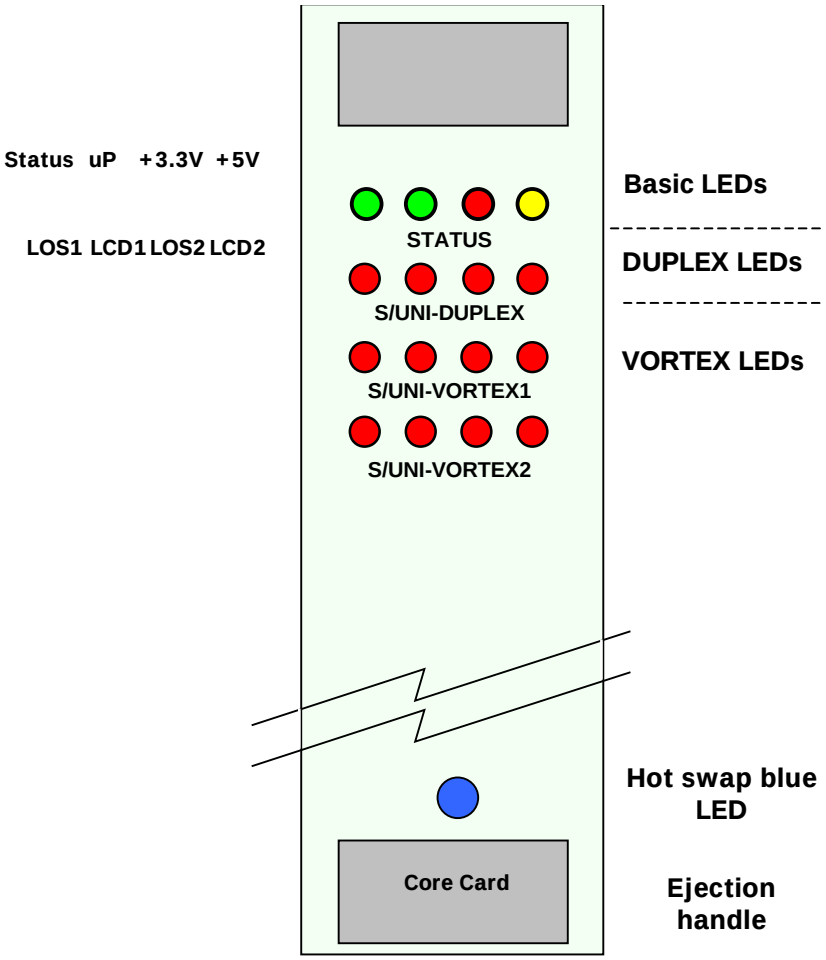
- LOS1, red – loss of signal at the S/UNI-DUPLEX LVDS RXD1 Port[1]
- LCD1, red – loss of cell delineation at the S/UNI-DUPLEX LVDS RXD1 Port[1]
- LOS2, red – loss of signal at the S/UNI-DUPLEX LVDS RXD2 Port[2]
- LCD2, red – loss of cell delineation at the LVDS RXD2 S/UNI-DUPLEX Port[2]

The preferred functionality for LEDs in the next two rows is showing the status of the LVDS on both the S/UNI-VORTEX-1 and the S/UNI-VORTEX-2.

The cPCI specification requires that the blue LED associated with the lower extraction handle be placed next to the handle at the very bottom of the front plate.

Figure 38 shows an example of the LED placement on the front plate.

Figure 38. Example of LEDs Placement



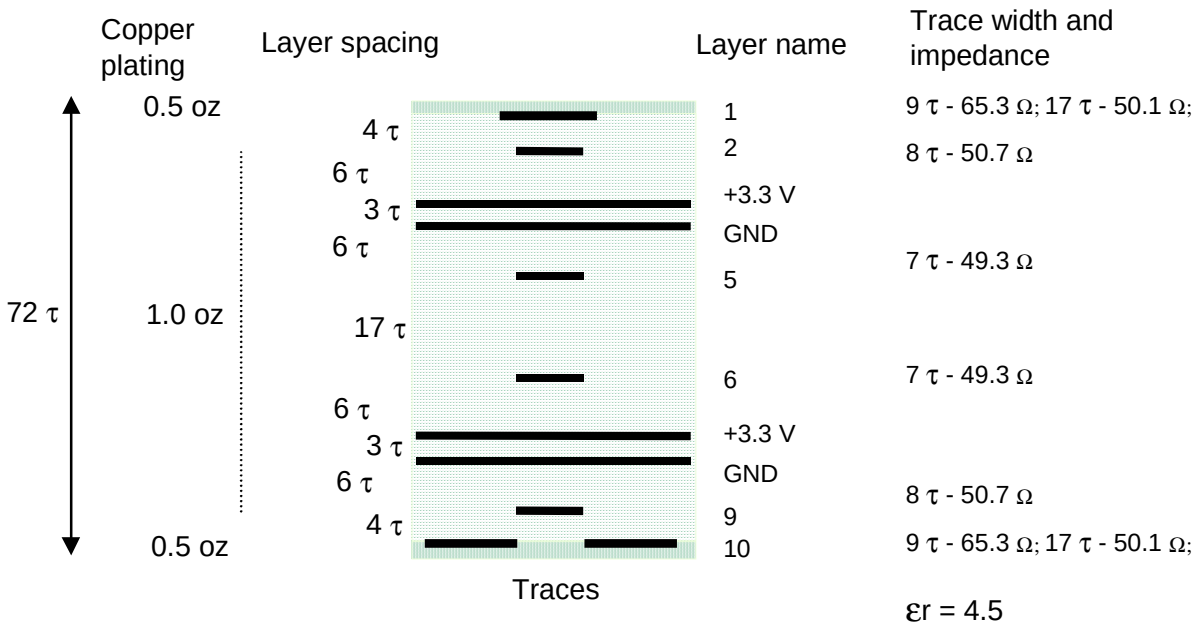
Two green LEDs, used for supply voltages +5 V and +3.3 V, should not be used as an indicator for accurate voltage level. All other LEDs are controlled with the CPLD and are entirely dependent on the software driver.

The blue LED is also software controlled, with the exception of the reset on the host CPU card. The PCI reset turns the LED *ON* using the PCI9054. The blue LED indicates that the card is not operable when it is inserted or removed from the DSLAM shelf.

12.4. Printed Circuit Board Stack

The board is laid out with 10-layer copper stack. Figure 39 shows an example of the cross-section.

Figure 39. PCB Cross-section



The ground and power planes are placed at 0.003-inch spacing. This spacing allows for high capacitance (with low parasitic inductance) between the planes, and to create the best filtering of high frequency power rail noise.

The +5.0 V and +2.5 V rails are isolated islands, cut out from the +3.3 V copper plane (not shown above).

The critical traces for 50 ohm LVDS differential pairs and 65 ohm PCI interface are shown in the most right column. The 50 ohm traces are at 7 to 17 τ wide, depending on the layer. The 65 ohm PCI interface is laid out only on two external layers. The digital lines are done at about 60 ohms with 5 τ wide traces on inner layers.

12.5. Key Coding on the J1 Connector

Connector J1 on the Core Card provides the option for keying, which prevents card insertion into an unknown shelf. The Reference Design Core Card is shipped without the key. The Core Card can operate with VI/O at +5 V or at +3.3 V.

The cPCI *rule-of-the-thumb* is to not plug the cPCI card into an unknown shelf!

12.6. Power Supply Specification

This section briefly describes some issues related to power supply.

12.6.1. Core Card

The Core Card requires a +5 V and 3.3 V supply, fed through cPCI connector J1.

Power required for each chip can be estimated using the VORTEX chipset data sheet. The result, though, may be an exaggerated power dissipation, not exactly correlated to measurement in the real system.

The total current to the Core Card (board Rev. 3) at +3.3 V rail is about 2.9 A, with traffic at about 40 kcell/s at the S/UNI-ATLAS Ingress input. The safety factor of 40 % brings the current to 4.1 A. The higher safety margin is due to some current changes with supply rail variation.

The total current at 5 V rail is about 0.6 A. That current includes the S/UNI-APEX core current at 2.5 V rail. The safety factor of 40 % brings the current to 0.84 A.

Total power dissipation on the Core Card, Issue 3, is estimated at
P = (5.25 V * 0.84 A) + (3.6 V * 4.1 A) = 19.2 W.

The Core Card requires a forced airflow cooling system in enclosed shelves. While the Core Card (board Rev. 3) was tested in an open development shelf, no excessive overheating was observed.

The Core Card operates when it is powered with a standard switching power supply found throughout the PC industry.

12.6.2. S/UNI-DUPLEX and S/UNI-VORTEX

The S/UNI-DUPLEX and S/UNI-VORTEX devices need only a single RC filtering element on the CAVD, CAVD0, and CAVD1. The schematic shows zero ohm resistors on other supply rails. Board can be laid out with those rails shorted directly to +3.3 V rail.

13. SOFTWARE

13.1. System Processor Requirement

The Core Card must be accompanied with a card on the same cPCI shelf. The host processor provides a power-up setup for the DSLAM chipset. The host processor controls operation, alarms and maintenance of the Core Card.

13.2. DSLAM Operating System

The DSLAM Reference Design Core Card is run with a software ported on a host processor card with the VxWorks operating system (OS). This is a real-time OS (RTOS). The device drivers for individual chips are also best portable on a platform with the VxWorks.

13.3. Device Drivers

PMC-Sierra, Inc. provides, on request, drivers for each DSLAM chipset device that is mounted on the Core Card.

PMC-Sierra, Inc. provides, on request, the VORTEX Chipset Driver (board level driver, or metadriver) for the VORTEX chipset that is mounted on the Core Card.

13.4. Example of VORTEX Chipset Setup

The following is an example of a possible VORTEX chipset setup sequence on power-up (or reset), executed by the software. This is only an example sequence. For updates to the software drivers, refer to the PMC-Sierra web site regularly.

13.4.1. APEX Setup

- Reset chip.
- Wait for the DLL to run.
- Do a zero out of all memory apertures.
- Set up the configuration registers.
- Set up the cell buffer free list.
- Set up the shaper.
- Set up the port.
- Set up the class.
- Set up the connection.
- Enable the interrupts.
- Enable the queue engine.

13.4.2. APEX Operations

- Receive or send cells or frames through the SAR interface.
- Perform a watchdog patrol on FCQ VCs.
- Set up or tear down ports, classes, and connections dynamically.

13.4.3. DUPLEX and VORTEX Setup

- Reset the chip.
- Set S/UNI-DUPLEX OCAEN in register 0x0A to 0 (zero). Keep at low through whole initialisation process.
- Set up the configuration registers.
- Set up the Logical Channel Base Address and Address Range in VORTEX chips.
- Set up the Control Channel Base Address in VORTEX chips.
- Enable the HSS links that are connected to the Line Cards or WAN Cards.
- Enable polling on S/UNI-ATLAS.
- Set S/UNI-DUPLEX OCAEN to 1 (one).
- Enable the interrupts, as needed.

IMPORTANT NOTE:
The S/UNI-DUPLEX requires OCAEN bit in register 0x0A to be activated as the very last write, after polling on the S/UNI-ATLAS is enabled. The VORTEX Chipset Driver files vcs_api1.c and dpx.c take care for proper sequencing. Software designers are required to observe sequencing in their drivers.

13.4.4. DUPLEX And VORTEX Operation

- Receive or send cell or messages through its microprocessor port.

13.4.5. ATLAS Setup

- Reset the chip.
- Initialise VC tables, and zero out the SSRAM memory.
- Set up the configuration registers.
- Set up VC connections including the search tree in the Ingress VC Table.
- Set up and enable OAM support.
- Set up PM sessions, if preferred.
- Set up F4 to F5 processing, if preferred.
- Enable the interrupts.
- Enable VCs.

13.4.6. ATLAS Operations

- Receive or send cells or frames through its microprocessor interface. You can use the interface for OAM support.
- Set up or tear down the connections dynamically. The search tree is updated dynamically too.
- Enable or disable the connections dynamically.
- Read out the PM record for performance monitoring, if preferred.

13.4.7. Important Notes For Chipset Level Setup

- Make sure the bus interface configuration for the APEX, ATLAS, VORTEX, DUPLEX devices are compatible, and the devices send or transmit cells of the same protocol. (Prepend and H5/UDF bytes be consistent.)
- Suggest using the same connection ID number for both the APEX and ATLAS VC table index. This simplifies VC management.
- Suggest using the following algorithm to map the loop port address space:
  - LoopId[11:0] = VtxId[11:8] | HssLnkId[7:5] | xdslPhyId[4:0].
  - the logical channel base address and range in VORTEX devices should be configured appropriately, based on the above loop port mapping algorithm.
- Suggest using the following search key in ATLAS:
  - Primary Key = 5 bits PHY ID + 9 bits Field A (embedded address in 9 H5/UDF LSB bits)
  - Secondary Key = 28 bits of VPI/VCI. No field B.

13.5. Firmware

The Core Card has firmware stored in a serial EEPROM that supports the PCI bridge. This device is an 8-pin DIP that is externally programmable and is placed into a socket.

13.6. Programmable Logic Devices

The Core Card has a single, in-circuit, programmable CPLD that is permanently assembled (soldered).

13.7. System Control

The Core Card provides limited functionality for the system control. The CPU processor can execute a global reset on the WAN Card or Line Card through the

Core Card. This can be done with the S/UNI DUPLEX-DUPLEX or VORTEX-DUPLEX LVDS links through the BOC (bit oriented code).

The Inband Communication Channel (ICC) allows building custom communication channel between the two DSLAM entities, and in turn, the whole DSLAM system can be in-system reprogrammed and controlled from a single processing center. It is assumed that the microprocessor entities on both sides of the connection are running a reliable communications protocol. This has not been implemented in VORTEX Chipset Driver.

14. APPENDIX A: TESTS EXAMPLE UTILIZING CORE CARD DRIVER

14.1. Register and RAM Test with VORTEX Chipset Driver

Description: This test uses the VORTEX Chipset Driver functionality and a special test program written in C, creating a primitive text line interface that accesses the Core Card entities.
The primary function of this test is to verify the registers on all VORTEX chipset devices and the external RAM on the S/UNI-ATLAS and S/UNI-APEX. The test also verifies (indirectly) the microprocessor interface.
The register test derives the expected type and ID bits from the register 0x00 on all VORTEX chipset devices.
The RAM test writes, reads, and compares data patterns.

Stimulus: Boot the DSLAM shelf with the Core Card from a boot disk and server software. Run the test software routines that use API and metadriver.
Type the command names to invoke the test routines from Tcl consloe window (or from a dumb terminal). The Core Card must be in a specific state to run the RAM test, that is, the RAMs are not activated and no traffic is allowed during the RAM test.

Expected Results: The test software reports no errors.

Actual Results: Register Test. The register test passed on all boards.

RAM Test. The initial RAM test provided by the software group passed the S/UNI-ATLAS RAM test. It was later found that the Ingress RAM interface reported a parity error with the traffic test. Investigation on the S/UNI-ATLAS RAM interface showed that the test pattern and read/write sequence was inappropriate. If the RAM is written and read immediately after, it may read correct values even if the RAM chip is removed from the board. This is due to the S/UNI-ATLAS data drivers indefinitely holding the last written word. The data bus has no pull down/up resistors and the read data may be exactly as the write one. The solution is to write fifteen rows of complimentary hex pattern words (64-bit) to the whole VC Table RAM and then read it. An example of a pattern is shown below.

aaaaaaaaaaaaaaaa (or binary 10101010 …)
5555555555555555 (or binary 01010101 …)
aaaaaaaaaaaaaaaa
….
aaaaaaaaaaaaaaaa
5555555555555555

It is very important to make sure the last word written is complimentary (different) from the first word read. Other patterns can be (hex) C0C0C0… and 030303… . A walking "1" may not find the problem if the read and write follow each other.

The improved test and sequence pattern was run again, and a cold solder was found on one of the Ingress RAM leads.

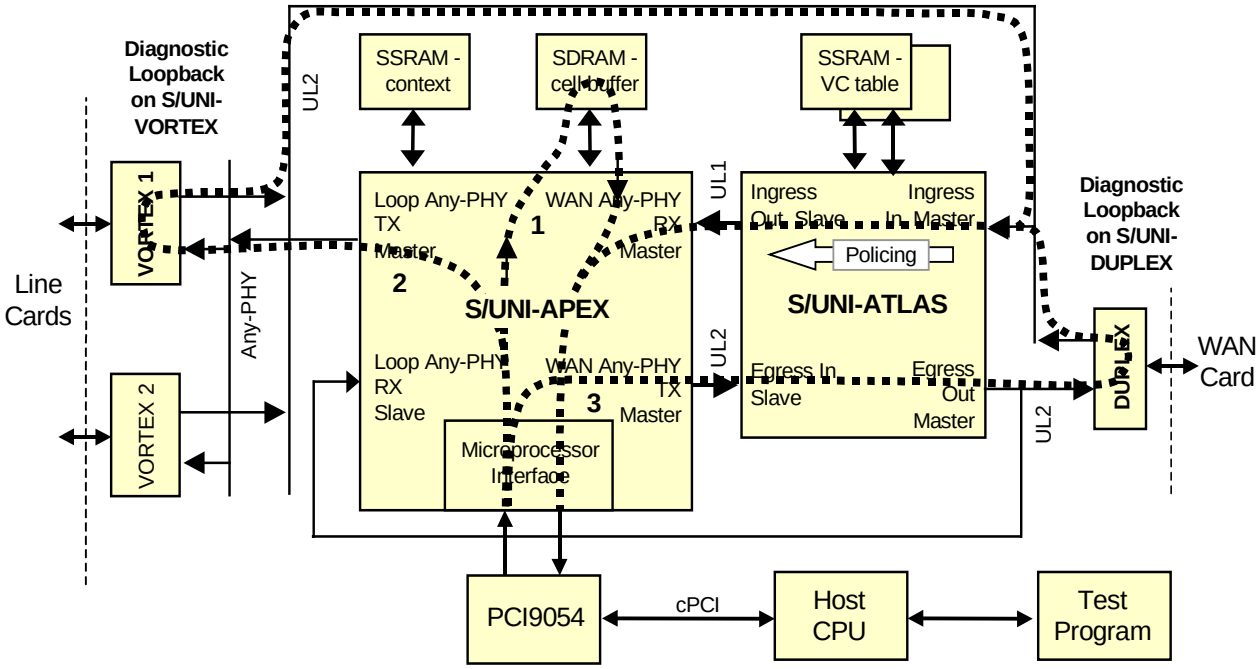
14.2. Cell Data Path with Internal Loopback Test

The tests described in this section verify the cell data paths through the Core Card. This is one of the very first data path tests applied to the Core Card on test shelf. The test is very useful to help troubleshoot and verify the basic functionality of the Core Card.

The test is executed with test routines written in C. The tests are invoked with Tcl environment through a serial port from the external PC or from a dumb terminal that is connected directly to the host processor card running VxWorks and communicating to the Core Card. The Motorola CPV500 SBC host processor card was used throughout software and hardware development and the test.

The cell is generated with the S/UNI-APEX microprocessor interface and received at the same interface. Figure 40 shows the cell path.

Figure 40. Data Path with Internal Loopback



The cell is always stored in the external Cell Buffer RAM (SDRAM), and then directed to the appropriate port. The test routine allows passing cells on three paths:

1. Microprocessor-to-microprocessor at the S/UNI-APEX only, on path 1. This path is useful for troubleshooting the RAM interface on the S/UNI-APEX.

2. Loopback at the S/UNI-VORTEX 1 or 2 on path 2. The cell tests Any-Phy interface from the S/UNI-APEX to the S/UNI-VORTEX. At the S/UNI_VORTEX, the cell is looped with the Diagnostic Loopback on a chosen high-speed link. The cell travels on the Utopia Level 2 / SCI-PHY bus upstream to the Ingress Input on the S/UNI-ATLAS, and finally on the Utopia Level 1 bus to the S/UNI-APEX. The cell is directed to the microprocessor buffer at the S/UNI-APEX.

3. Loopback at the S/UNI-DUPLEX on path 3. The cell tests the Utopia Level 2 bus upstream from the S/UNI-APEX to the S/UNI-ATLAS. Then the cell travels on the Utopia Level 2 bus to the S/UNI-DUPLEX. At the S/UNI-DUPLEX, the cell is looped with the Diagnostic Loopback on one of two high-speed links. The cell travels downstream to the S/UNI-ATLAS (same interface as the cell on path 2) and finally reaches back to the S/UNI-APEX. The cell is directed to the microprocessor buffer at the S/UNI-APEX.

14.3. External Loopback Test

14.3.1. Sub Test 1: Downstream/Upstream on Sixteen Channels.

Description: The test was designed to use the PM1555A ATM over the DS-3 tester. A cell generated with the PM1555A tester travels 32 times through the S/UNI-ATLAS Ingress Input, observed with oscilloscope at the RRDENB line. Each round cell has the VPI/VCI header remapped with the S/UNI-ATLAS, so it can be sent by the S/UNI-APEX to the appropriate port. The cell goes sixteen times through Loop Tx and sixteen times through the WAN Tx ports.
Figure 41 shows the block diagram depicting the test setup.

Figure 41. External Loopback with ATM over DS-3 Tester

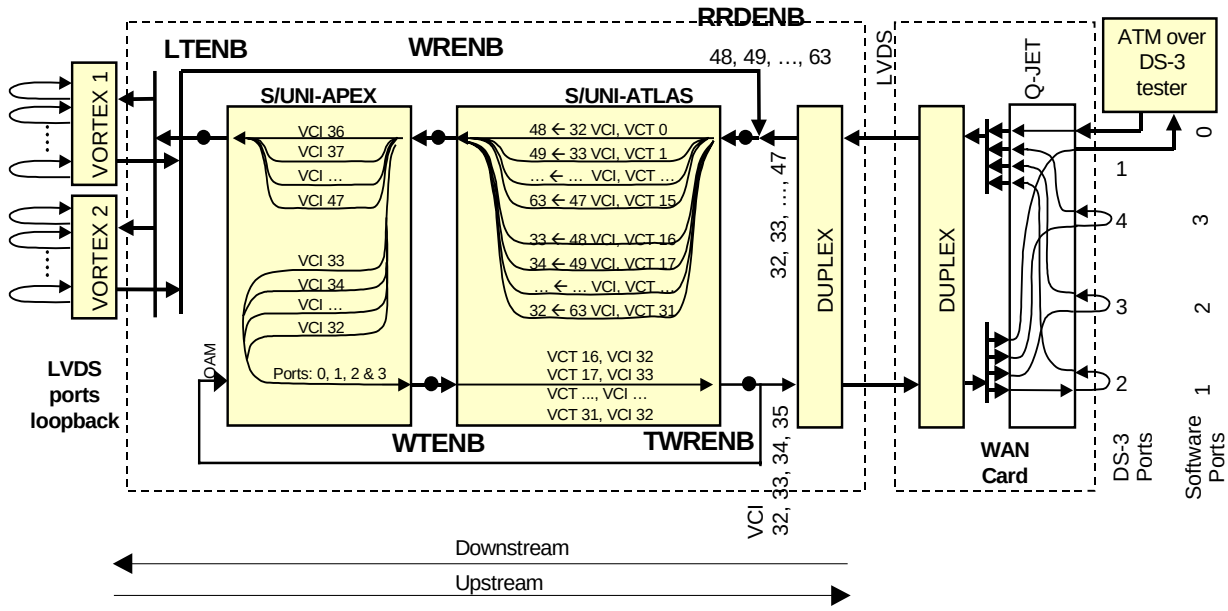


TABLE 8 shows the parameters from an automatic test that sets sixteen connections in each direction (total of 32).

TABLE 8. Connection Setup

Input Port Type		Port #1	VPI	VCI	Input Port Type		Port #2	VPI	VCI	Table #
	VCS_WAN_PORT	0	100	32	VORTEX 1	VCS_LOOP_PORT	0	100	48	0
	VCS_WAN_PORT	1	100	33		VCS_LOOP_PORT	32	100	49	1
	VCS_WAN_PORT	2	100	34		VCS_LOOP_PORT	64	100	50	2
	VCS_WAN_PORT	3	100	35		VCS_LOOP_PORT	96	100	51	3
	VCS_WAN_PORT	1	100	36		VCS_LOOP_PORT	128	100	52	4
	VCS_WAN_PORT	2	100	37		VCS_LOOP_PORT	160	100	53	5
	VCS_WAN_PORT	3	100	38		VCS_LOOP_PORT	192	100	54	6
	VCS_WAN_PORT	1	100	39		VCS_LOOP_PORT	224	100	55	7
	VCS_WAN_PORT	2	100	40	VORTEX 2	VCS_LOOP_PORT	256	100	56	8
	VCS_WAN_PORT	3	100	41		VCS_LOOP_PORT	288	100	57	9
	VCS_WAN_PORT	1	100	42		VCS_LOOP_PORT	320	100	58	10
	VCS_WAN_PORT	2	100	43		VCS_LOOP_PORT	352	100	59	11
	VCS_WAN_PORT	3	100	44		VCS_LOOP_PORT	384	100	60	12
	VCS_WAN_PORT	1	100	45		VCS_LOOP_PORT	416	100	61	13
	VCS_WAN_PORT	2	100	46		VCS_LOOP_PORT	448	100	62	14
	VCS_WAN_PORT	3	100	47		VCS_LOOP_PORT	480	100	63	15
VORTEX 1	VCS_LOOP_PORT	0	100	48		VCS_WAN_PORT	1	100	33	16
	VCS_LOOP_PORT	32	100	49		VCS_WAN_PORT	2	100	34	17
	VCS_LOOP_PORT	64	100	50		VCS_WAN_PORT	3	100	35	18
	VCS_LOOP_PORT	96	100	51		VCS_WAN_PORT	1	100	36	19
	VCS_LOOP_PORT	128	100	52		VCS_WAN_PORT	2	100	37	20
	VCS_LOOP_PORT	160	100	53		VCS_WAN_PORT	3	100	38	21
	VCS_LOOP_PORT	192	100	54		VCS_WAN_PORT	1	100	39	22
	VCS_LOOP_PORT	224	100	55		VCS_WAN_PORT	2	100	40	23
VORTEX 2	VCS_LOOP_PORT	256	100	56		VCS_WAN_PORT	3	100	41	24
	VCS_LOOP_PORT	288	100	57		VCS_WAN_PORT	1	100	42	25
	VCS_LOOP_PORT	320	100	58		VCS_WAN_PORT	2	100	43	26
	VCS_LOOP_PORT	352	100	59		VCS_WAN_PORT	3	100	44	27
	VCS_LOOP_PORT	384	100	60		VCS_WAN_PORT	1	100	45	28
	VCS_LOOP_PORT	416	100	61		VCS_WAN_PORT	2	100	46	29
	VCS_LOOP_PORT	448	100	62		VCS_WAN_PORT	3	100	47	30
	VCS_LOOP_PORT	480	100	63		VCS_WAN_PORT	0	100	32	31

A test routine sets sixteen ports to/from on the loop side and four ports on the WAN side. The cells from the WAN Card enter the S/UNI-ATLAS with the VCI at 32 through 47. The cells from the loop side (loopback at S/UNI-VORTEX LVDS upstream) enter the S/UNI-ATLAS with the VCI at 48 through 63.

All cells have VPI = 100. The parameter *Port number #1* specifies the entry port, and *Port number #2* specifies the exit port. Ports at the S/UNI-VORTEX1 are distributed across four HSS links with port address 0, 32, 64 up to 480 (this is embedded in Any-PHY ID in the downstream direction and in H5/UDF in the upstream direction). Header remapping is set in the S/UNI-ATLAS. This requires setting the global register 0x200 bit GVPIVCI = 1. Also, the appropriate *Header (40)* must be entered in the VC Table at row 0111 for each connection.

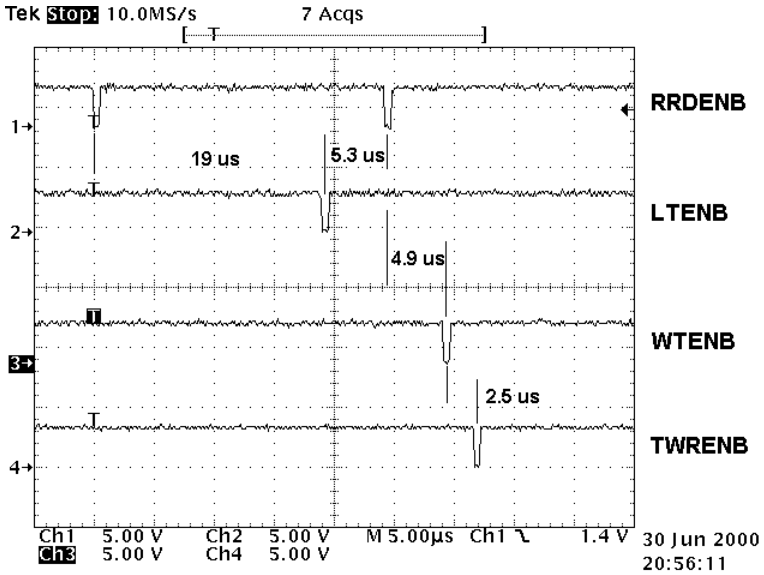
Stimulus: Boot the DSLAM shelf with the Core Card from a boot disk and server software. Run the test software routine `vtxcsExtLpbkTest16d x .`
If cables for external LVDS loopback are not available, then diagnostic loopback on the S/UNI-VORTEX1 and 2 can do the job. Also, Tcl script helps expediting settings.

Expected Results: Data throughput is shaped by the S/UNI-APEX, allowing up to 6 Mb/s per connection and allowing total throughput at the WAN Card (Core Card LVDS of about 6 x 16 = 96 Mb/s).

Actual Results: The Reference Design Core Card Issue 3 passed the external loopback test with about 6 Mb/s (15 kcell/s) of data at the single DS-3 set at the PM1555A tester.

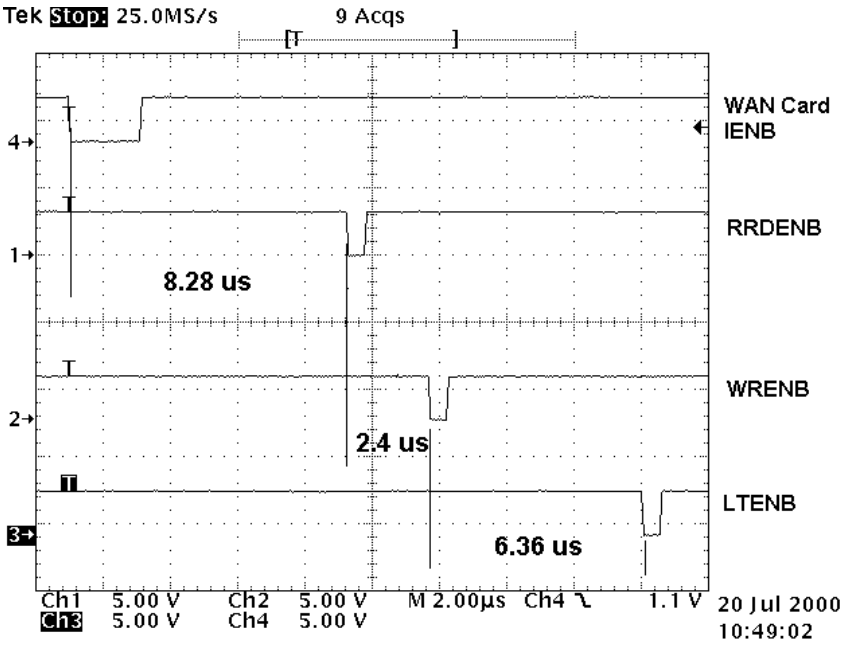
Traffic was set at the PM1555A to below 10 kb/s. FIGURE 1 shows the cell flow that was captured with the oscilloscope.

FIGURE 1. Cell Flow with External Loopback



The first cell at the *RRDENB* comes from the WAN Card. The cell passes the S/UNI-ATLAS ingress and is the output from the S/UNI-APEX downstream at *LTENB* about 19 µs later. The cell arrives at the *RRDENB* about 5.3 µs later after loopback at the S/UNI-VORTEX. After 4.9 µs, the cell passes the S/UNI-ATLAS and S/UNI-APEX, and shows up at *WTENB* on the S/UNI-ATLAS Egress Input. Finally, the cell goes in 2.5 µs through the S/UNI-ATLAS and is sent on *TWRENB* to the S/UNI-DUPLEX and next to the WAN card. The WAN Card is loopback with external DS-3 interface, in such a way that ports 2, 3, and 4 (or software ports 1, 2, and 3) loopback to itself. The cells are sent and received at DS-3 port #1 (or software port 0).

FIGURE 2. Cell Flow with External Loopback including WAN Card



The WAN Card IENB is at 25 MHz and bus width of 8-bits. Therefore, the IENB signal is four times longer than other signals on the Core Card with the clock at 50 MHz and a bus width of 16-bit.

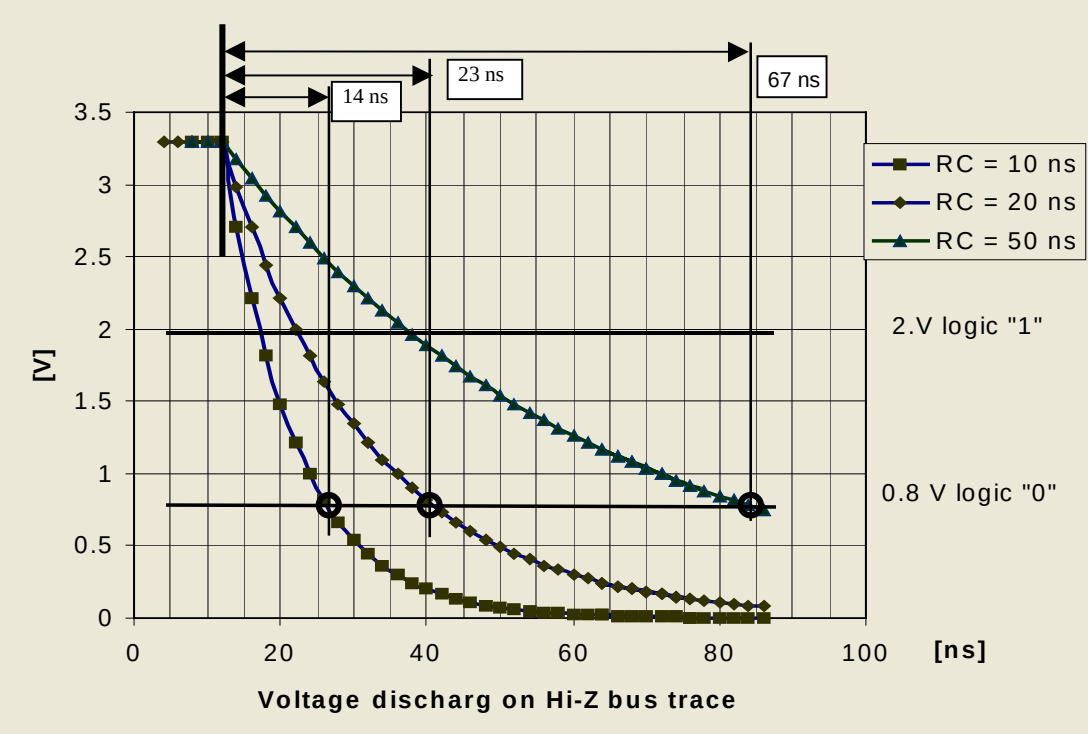
The cell needs about 8.28 µs to get from the WAN Card to the RRDENB. The cell goes in 2.4 µs to the WRENB – S/UNI-APEX Loop Rx. The cell leaves the S/UNI-APEX 6.36 µs later at the LTENB towards S/UNI-VORTEX.

15. APPENDIX B: VOLTAGE DISCHARGE ON TRI-STATED BUS

The voltage discharge on the tri-stated (high-Z) bus line with pull up/down resistors may cause some problems when the time constant is too long. This refers especially to “cell available” lines, for example, RCA, TPA, TCA, ICA, etc. Analyze the situation when there is no pull-down resistor on the “cell available” line. The slave device is polled and responds with logic high on the “cell available” line and then goes into the high-Z. Capacitance distributed across the bus keeps the logic *high* for many clock cycles. If on the next address cycle master polls mismatched slave address with no slave responding, then logic *high* on “cell available” kept by capacitance will fool master and master may initiate non-existing cell transfer. At least one cell cycle is lost, and in the worst condition, unwanted FIFO overflow occurs somewhere. The cell count is increased in the corresponding device. That phenomenon was observed upon development. Inexperienced person may have hard time resolving the problem. With a properly assigned bus poll range and a slave address (channel) range, there should be, in most cases, a device that responds low or high on the “cell available” lines. However, we recommend pull-down resistors on all “cell available” lines.

Figure 42 shows the voltage discharge with a different time constant.

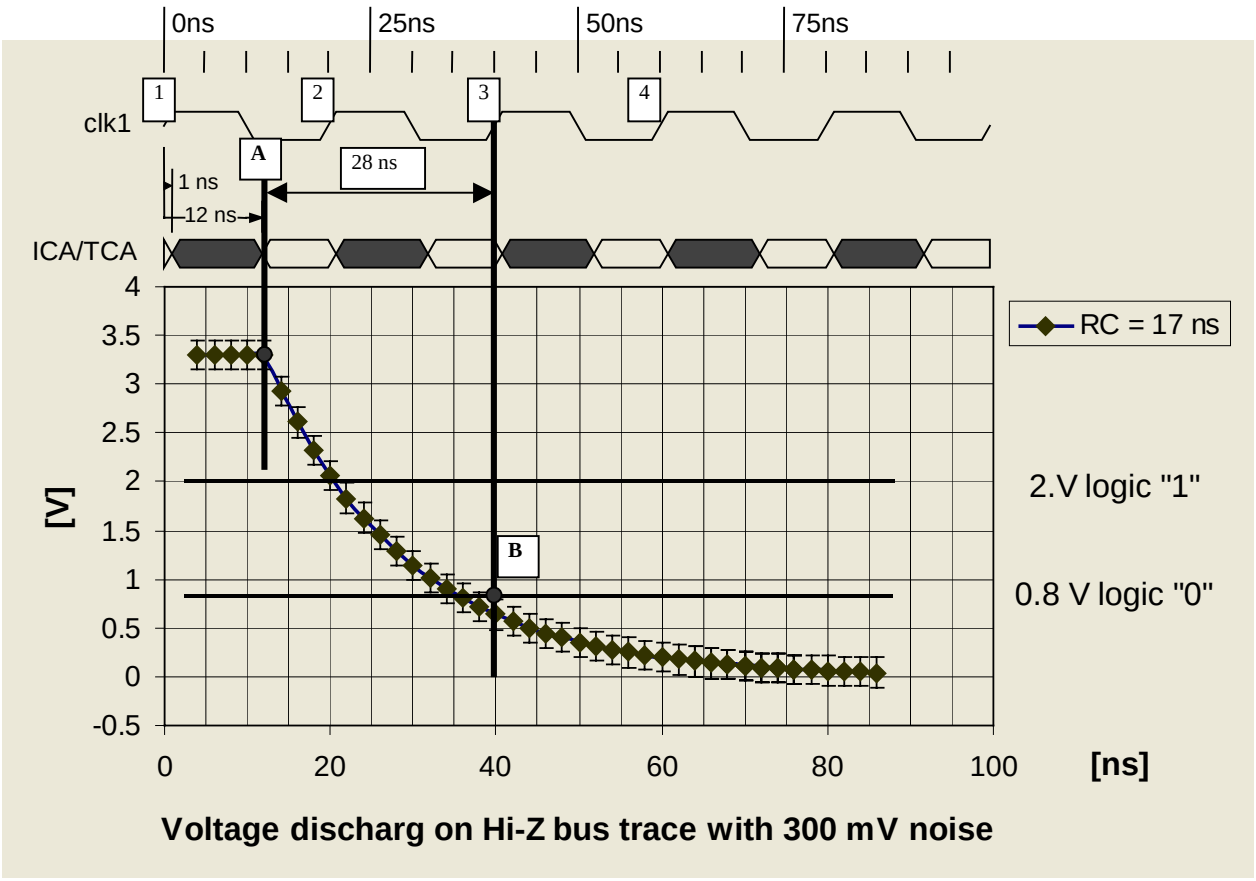
Figure 42. Voltage Discharge on Hi-Z Bus Line



Voltage curves with a time constant at 10 ns, 20 ns, and 50 ns are reaching logic “0” in about 14 ns, 23 ns, and 68 ns respectively.

Figure 43 shows an example of a bus at 50 MHz and a simulated discharge after S/UNI-DUPLEX goes into high-Z.

Figure 43. Voltage Discharge on Hi-Z Bus Line with Noise



Voltage discharg on Hi-Z bus trace with 300 mV noise

A 300 mV (±150 mV) noise is added making exercise more realistic in a digital environment.

For example, assume that the S/UNI-DUPLEX goes into high-Z cycle on the clock edge marked “1”. Also, at this point, the bus master starts the valid address poll cycle and checks the response at clock edge “3”. After 12 ns, according to the S/UNI-DUPLEX data sheet, the output is tri-stated (marked as “A” above). The logic voltage at about 3.3 V starts dropping exponentially. Signal and noise goes below 0.8 V (TTL logic “low” guaranteed by our I/Os) 28 ns later (marked as “B” above). At this point, the clock edge marks “3” samples for “cell available” and finds the signal as logic “low”. If the time constant is longer, as shown in Figure 42, the signal can be sampled as logic “high” fooling bus master.

The time constant is determined at 17 ns for this exercise. With a small bus consisting of three devices, the total capacitance can be estimated as
3 * 5 pF + 5 pF = 20 pF total.

The additional 5 pF is for trace and termination resistors. With this capacitance, the pull-down resistor can be calculated as
R = (17 ns) / (20 pF) = 0.85 kohm.

With the bus consisting of 10 devices, the total capacitance is above 55 pF, and the pull-down resistor is calculated at
R = 0.31 kohm. This resistor value may overload the bus driver and prevent it from delivering logic “high” to the bus line. Designer must verify the *cell available* signals on a build board. When choosing a resistor value, a compromise should be found. The system designer should make sure the polling address range matches the slave address range to prevent additional bus cycles and prevent the sending of undeliverable cells that take 27 to 29 clock cycles.

16. APPENDIX C: EXAMPLE OF SEEP READING ON RESET

Figures 12 and 13 (below) show an example of reading SEEP on PCI reset. Both figures show a signal at pins CK (pin2), CS (pin1), and DO/DI (pin3-4), while PCI9054 reads SEEP.

Figure 44. Example of SEEP Reading Upon PCI Reset

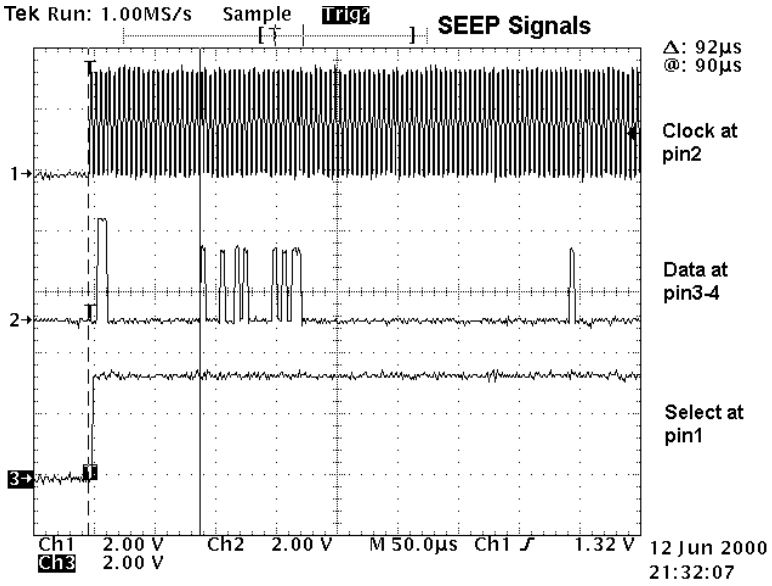
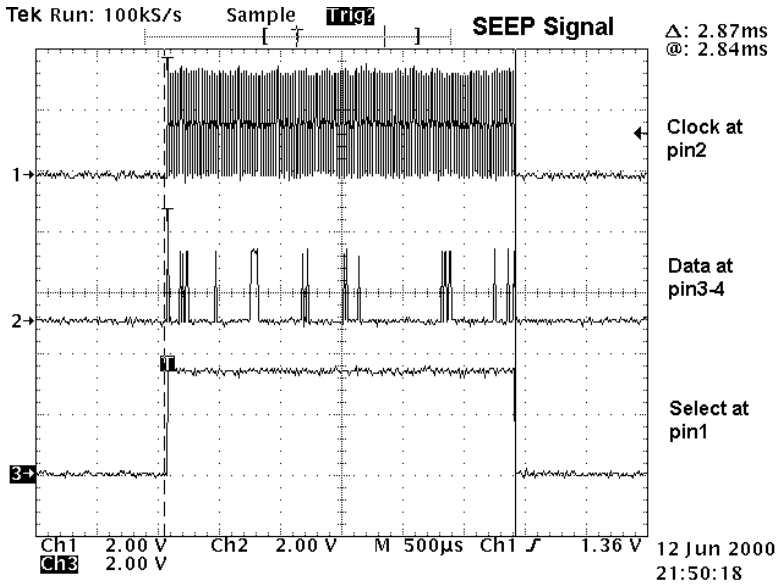


Figure 45. Example of SEEP Reading Upon PCI Reset

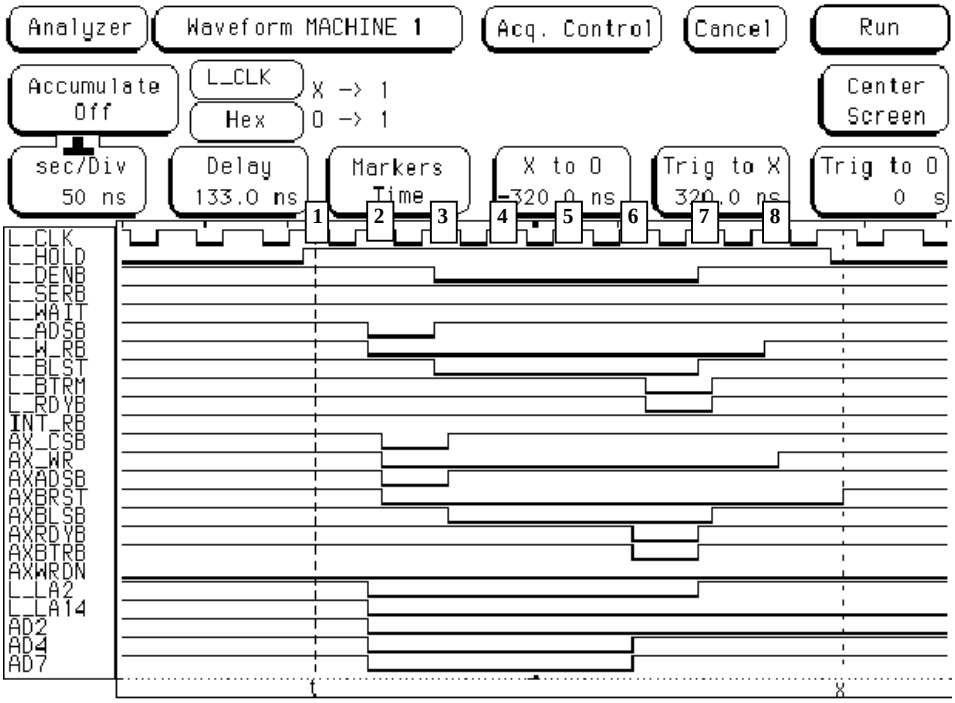


17. APPENDIX D: LOCAL BUS TIMING EXAMPLES

17.1.1. Timing Example for Read from S/UNI-APEX

Figure 46 shows an example of a single read from the S/UNI-APEX, captured with a logic analyzer. Due to logic analyzer limitation, the signal abbreviations may not correspond directly to net names on the schematics.

Figure 46. Example Read from the S/UNI-APEX at 25 MHz



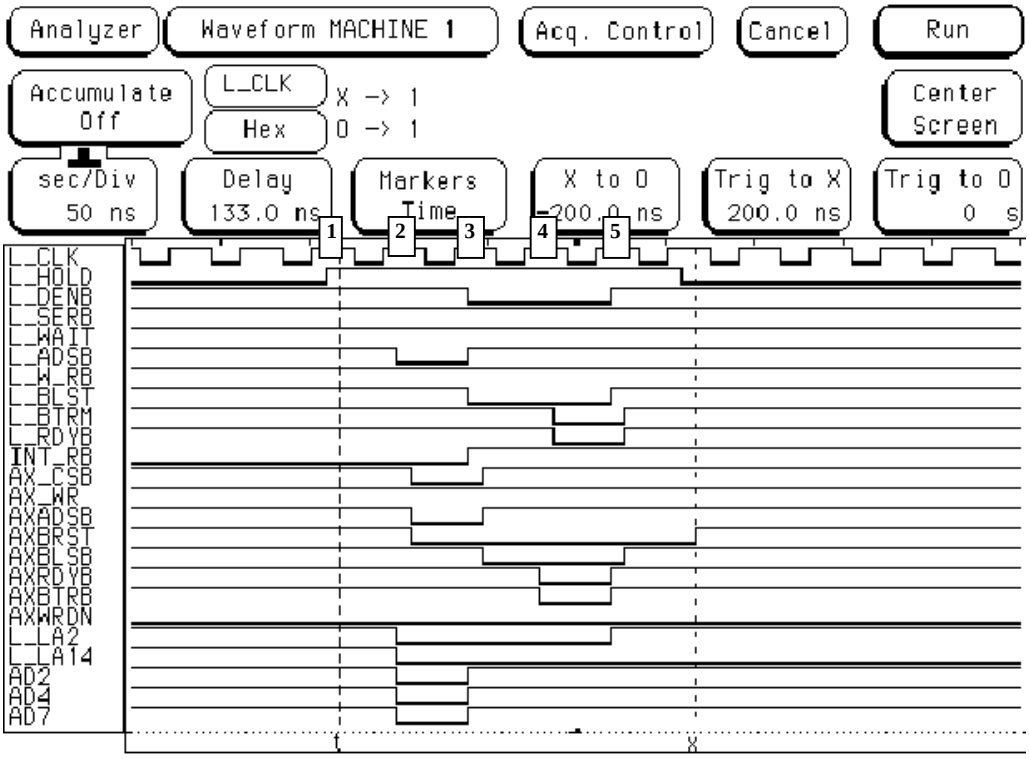
The data transfer is started with a PCI5054 setting of L_HOLD *high*. The S/UNI-APEX asserts the low signal AXRDYB (READYB pin) and AXBTRB (BTERMB pin), which are read into the PCI9054 four clock after line AX_CSB is asserted low. The L_READYB line signals valid data output from the S/UNI-APEX, and that also terminates the data transfer. The PCI9054 de-asserts L_HOLD by toggling it *high* two clocks later. Read from APEX takes eight clock cycles. L_HOLD stays at the *high* setting for eight clock cycles.

Some jitter on data edges is visible due to a 4 ns logic analyzer resolution.

17.1.2. Timing Example for Write to S/UNI-APEX

Figure 47 shows an example of a single write to the S/UNI-APEX, captured with a logic analyzer.

Figure 47. Example Write to APEX Cycle on Local Bus at 25 MHz

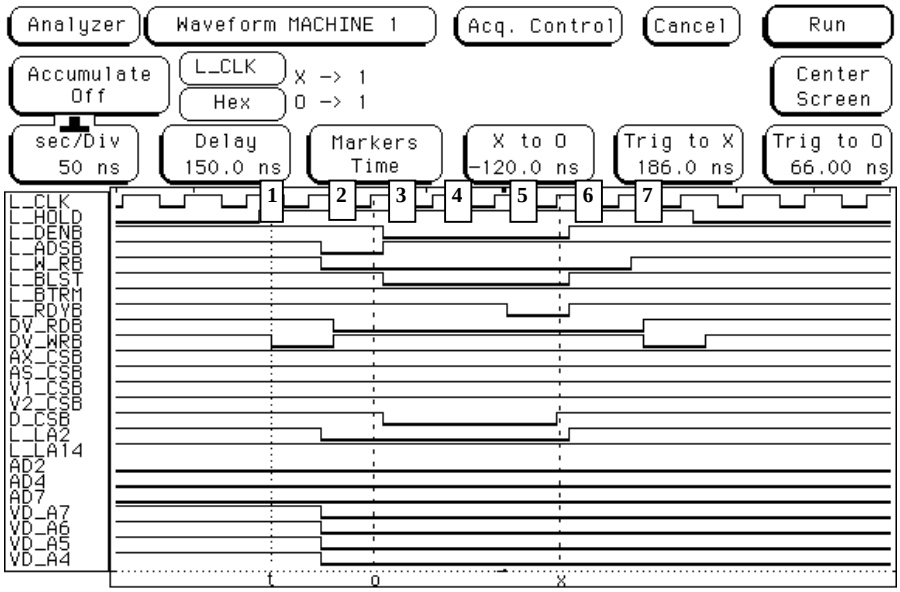


Local address lines L_LA2 and L_LA14 remain steady over three clock cycles, and set the permanent address required for the chip select. Address/Data lines AD2, AD4 and AD7 are all-low with the L_ADSB address strobe at the address cycle (for that particular address) and then toggle to *high* for the data cycle writing all ones to the S/UNI-APEX. A write to the S/UNI-APEX takes five clock cycles, where L_HOLD stays *high* for five clock cycles (at 25 MHz clock, 5 x 40 ns = 200 ns).

17.1.3. Timing Example for Read from S/UNI-DUPLEX

Figure 48 shows an example of the access to the S/UNI-DUPLEX.

Figure 48. Example Read from the S/UNI-DUPLEX



DV_RDB asserted *low* and DV_WRB asserted *high* determines the read from the S/UNI-DUPLEX (DV_RDB and DV_WRB – S/UNI-DUPLEX and S/UNI-VORTEX READ or WRITE *low*). The D_CSB is held low for three clocks, allowing proper access time to the S/UNI-DUPLEX. The L_RDYB goes *low*, signaling to PCI9054 that data is stable and ready to read. The CPLD internal clocking circuit generates the L_RDYB signal, allowing the slower S/UNI-DUPLEX interface to stabilize data. The chip select line D_CSB goes *high* at the same clock edge as the L_RDYB.

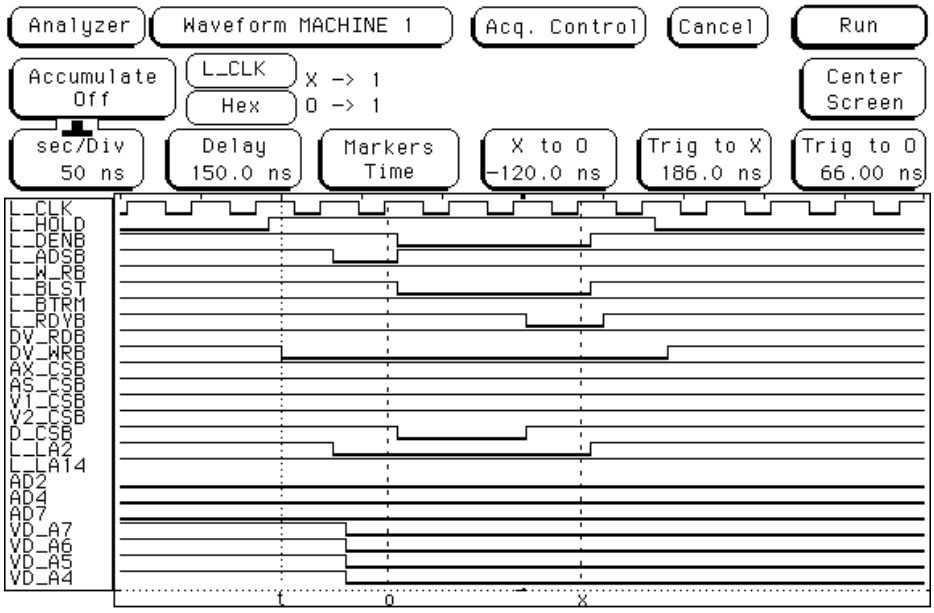
The DV_WRB line going *low*, at the very beginning and at the very end of the access to the S/UNI-DUPLEX, is an artifact of the internal logic. However, toggling is outside of the active access to the chip. (Toggle due to controlling of the DV_WRB with L_HOLD.)

Designer must ensure that timing is not violated on all control lines generated with the CPLD.

17.1.4. Timing Example for Write to S/UNI-DUPLEX

Figure 49 shows an example of a write to the S/UNI-DUPLEX.

Figure 49. Example Write to the S/UNI-DUPLEX



Address strobe L_ADSB latches address into CPLD, which in turns generates the chip select to a selected device. The S/UNI-DUPLEX chip select line D_CSB goes low:

- Immediately after L_ADSB is deselected
- Two clocks after bus hold L_HOLD initiates access to the S/UNI-VORTEX.

The D_CSB going high latches data into the S/UNI-DUPLEX. At the same clock, CPLD asserts L_RDYB, informing the local bus controller about data being accepted at the S/UNI-DUPLEX and ending the write cycle to the S/UNI-DUPLEX. The DX_CSB is held low for two clocks, allowing proper access time to the S/UNI-DUPLEX. CPLD internally generates the delay.

18. APPENDIX E: VHDL FOR CPLD

The preliminary VHDL source code for the CPLD is shown below. Internal LED D12, D13 and D15 programming variations may occur on particular production runs of the Core Card. Programming of those LEDs have no affect on control functions of the CPLD.

Check the PMC-Sierra, Inc. web site for the latest source code.

```
-- ------------------------------------------------------------------
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-- Burnaby, B.C.
-- Canada   V5A 4V7
-- Tel: 604-415-6000
-- Fax: 604-415-6206
-- email: apps@pmc-sierra.com
-- ------------------------------------------------------------------
-- Project      : PMC-990815
-- File Name    : dslam_core_cpld.vhd
-- Path         :
-- Designer     : PMC-Sierra, Inc.
--
-- Revision History
-- Issue        Date            Initials   Description
-- 1            09/09/99        xx         Initial Release
--
-- Function:
-- This is the top level of the VHDL code required for the DSLAM CORE
```

```
 -- reference design.  The code provides control to the micro ports on
 -- all PMC devices (1 S/UNI-DUPLEX, 2 S/UNI-VORTEXes, 1 S/UNI-ATLAS,
 -- 1 S/UNI-APEX) present on the DSLAM CORE Card.
 ----------------------------------------------------------------------
library IEEE;
use IEEE.std_logic_1164.ALL;
use IEEE.std_logic_arith.ALL;
ENTITY cccpld IS
 PORT (
  l_clk1 : IN STD_LOGIC;
  l_la : IN STD_LOGIC_VECTOR(11 DOWNTO 2);
  l_la_dec : IN STD_LOGIC_VECTOR (2 DOWNTO 0);
  l_ad : INOUT STD_LOGIC_VECTOR(15 DOWNTO 0);
  l_blastb : IN STD_LOGIC;
  l_btermb : OUT STD_LOGIC;
  l_w_rb : IN STD_LOGIC;
  l_readyb : OUT STD_LOGIC;
  l_adsb : IN STD_LOGIC;
  l_waitb : IN STD_LOGIC;
  l_intb : OUT STD_LOGIC;
  l_denb : IN STD_LOGIC;
  l_lserrb : IN STD_LOGIC;
  l_bhold : IN STD_LOGIC;
  vx_dx_d : INOUT STD_LOGIC_VECTOR(7 DOWNTO 0);
  vx_dx_a : OUT STD_LOGIC_VECTOR(9 DOWNTO 0);

  rstb : IN STD_LOGIC;
  rstb1 : IN STD_LOGIC;
  dx_vx_rdb : OUT STD_LOGIC;
  dx_vx_wrb : OUT STD_LOGIC;
  dx_csb : OUT STD_LOGIC;
  vx1_csb : OUT STD_LOGIC;
  vx2_csb : OUT STD_LOGIC;

  dx_intb : IN STD_LOGIC;
  vx1_intb : IN STD_LOGIC;
  vx2_intb : IN STD_LOGIC;

  as_busyb : IN STD_LOGIC;
  as_intb : IN STD_LOGIC;
  as_wrb : OUT STD_LOGIC;
  as_rdb : OUT STD_LOGIC;
  as_csb : OUT STD_LOGIC;

  ax_csb : OUT STD_LOGIC;
  ax_wr : OUT STD_LOGIC;
```

```
    ax_adsb : OUT STD_LOGIC;
    ax_burstb : OUT STD_LOGIC;
    ax_blast : OUT STD_LOGIC;
    ax_readyb : IN STD_LOGIC;
    axhi_intb : IN STD_LOGIC;
    axlo_intb : IN STD_LOGIC;
    ax_wrdoneb : IN STD_LOGIC;
    ax_btermb : IN STD_LOGIC;

    dxrx_8k : IN STD_LOGIC;
    vx1rx_8k : IN STD_LOGIC;
    vx2rx_8k : IN STD_LOGIC;
    ck_8kref : IN STD_LOGIC;
    ck_8kout : OUT STD_LOGIC;
    ck_pll_in : OUT STD_LOGIC;
    ck_pll_out : IN STD_LOGIC;
    ck_8kout_all : OUT STD_LOGIC;

    slot6 : IN STD_LOGIC;  -- optional; not shown on block diagram
    type0 : IN STD_LOGIC;  -- optional; same
    type1 : IN STD_LOGIC;  -- optional; same

    ledx1 : OUT STD_LOGIC;
    ledx2 : OUT STD_LOGIC;
    ledx4 : OUT STD_LOGIC;

    leds : OUT STD_LOGIC_VECTOR(13 DOWNTO 0); -- always turned ON with reset
    ga : IN STD_LOGIC_VECTOR(2 DOWNTO 0) -- optional, not used for this Core Card Issue 3
    );

END cccpld;

ARCHITECTURE cccpld_arch OF cccpld IS

  CONSTANT c_REG_ADDR_INTB : STD_LOGIC_VECTOR := "0000000000";
  CONSTANT c_REG_ADDR_LED  : STD_LOGIC_VECTOR := "0000000001";
  CONSTANT c_REG_ADDR_8KHz : STD_LOGIC_VECTOR := "0000000010";
  CONSTANT c_REG_INTB : INTEGER := 0;
  CONSTANT c_REG_LED  : INTEGER := 1;
  CONSTANT c_REG_8KHz : INTEGER := 2;
  CONSTANT c_BIT_DX_INT_ENB : INTEGER := 13;
  CONSTANT c_BIT_VX2_INT_ENB : INTEGER:= 12;
  CONSTANT c_BIT_VX1_INT_ENB : INTEGER :=11;
  CONSTANT c_BIT_AS_INT_ENB : INTEGER :=10;
  CONSTANT c_BIT_AXLO_INT_ENB : INTEGER :=9;
  CONSTANT c_BIT_AXHI_INT_ENB : INTEGER :=8;
```

```
  CONSTANT c_BIT_DX_INT : INTEGER :=5;
  CONSTANT c_BIT_VX2_INT : INTEGER :=4;
  CONSTANT c_BIT_VX1_INT : INTEGER :=3;
  CONSTANT c_BIT_AS_INT : INTEGER :=2;
  CONSTANT c_BIT_AXLO_INT : INTEGER :=1;
  CONSTANT c_BIT_AXHI_INT : INTEGER :=0;
  CONSTANT c_BIT_HEADER_8KHz : INTEGER := 0;
  CONSTANT c_BIT_Pll_0 : INTEGER := 1;
  CONSTANT c_BIT_Pll_1 : INTEGER := 2;
  CONSTANT c_ADDR_AX : STD_LOGIC_VECTOR(2 DOWNTO 0) := "000";
  CONSTANT c_ADDR_CPLD : STD_LOGIC_VECTOR(2 DOWNTO 0) := "001";
  CONSTANT c_ADDR_AS : STD_LOGIC_VECTOR(2 DOWNTO 0) := "010";
  CONSTANT c_ADDR_VX1 : STD_LOGIC_VECTOR(2 DOWNTO 0) := "011";
  CONSTANT c_ADDR_VX2 : STD_LOGIC_VECTOR(2 DOWNTO 0) := "100";
  CONSTANT c_ADDR_DX : STD_LOGIC_VECTOR(2 DOWNTO 0) := "101";
  CONSTANT c_CLOCK_PERIOD : INTEGER := 40;

  TYPE STD_LOGIC_2D IS ARRAY (2 DOWNTO 0) OF STD_LOGIC_VECTOR(15 DOWNTO 0);
  SIGNAL reg_file : STD_LOGIC_2D;

  SIGNAL dvas_readyb : STD_LOGIC;
  SIGNAL dx_vx_as_readyb : STD_LOGIC;
  SIGNAL dx_select : STD_LOGIC;
  SIGNAL vx1_select : STD_LOGIC;
  SIGNAL vx2_select : STD_LOGIC;

  BEGIN
    l_ad(7 DOWNTO 0) <= vx_dx_d WHEN l_w_rb = '0' AND l_denb = '0' AND ((l_la_dec =
c_ADDR_DX) OR (l_la_dec = c_ADDR_VX1) OR (l_la_dec = c_ADDR_VX2))
      ELSE reg_file(c_REG_INTB)(7 DOWNTO 0) WHEN l_w_rb = '0' AND l_denb = '0' AND
((l_la_dec = c_ADDR_CPLD) AND (l_la = c_REG_ADDR_INTB))
      ELSE reg_file(c_REG_LED)(7 DOWNTO 0) WHEN l_w_rb = '0' AND l_denb = '0' AND
((l_la_dec = c_ADDR_CPLD) AND (l_la = c_REG_ADDR_LED))
      ELSE reg_file(c_REG_8KHZ)(7 DOWNTO 0) WHEN l_w_rb = '0' AND l_denb = '0' AND
((l_la_dec = c_ADDR_CPLD) AND (l_la = c_REG_ADDR_8KHZ))
      ELSE "ZZZZZZZZ";

    l_ad(15 DOWNTO 8) <= reg_file(c_REG_INTB)(15 DOWNTO 8) WHEN l_w_rb = '0' AND
l_denb = '0' AND ((l_la_dec = c_ADDR_CPLD) AND (l_la = c_REG_ADDR_INTB))
      ELSE reg_file(c_REG_LED)(15 DOWNTO 8) WHEN l_w_rb = '0' AND l_denb = '0' AND
((l_la_dec = c_ADDR_CPLD) AND (l_la = c_REG_ADDR_LED))
      ELSE reg_file(c_REG_8KHZ)(15 DOWNTO 8) WHEN l_w_rb = '0' AND l_denb = '0' AND
((l_la_dec = c_ADDR_CPLD) AND (l_la = c_REG_ADDR_8KHZ))
      ELSE "ZZZZZZZZ";
```

```
   vx_dx_d <= l_ad(7 DOWNTO 0) WHEN l_w_rb = '1' AND l_denb = '0' AND ((l_la_dec =
c_ADDR_DX) OR (l_la_dec = c_ADDR_VX1) OR (l_la_dec = c_ADDR_VX2) OR (l_la_dec =
c_ADDR_AS))
       ELSE "ZZZZZZZZ";

   ck_pll_in <= dxrx_8k WHEN reg_file(c_REG_8KHZ)(c_BIT_Pll_0) = '0' AND
reg_file(c_REG_8KHz)(c_BIT_Pll_1) = '0'
            else vx1rx_8k WHEN reg_file(c_REG_8KHz)(c_BIT_Pll_0) = '1' AND
reg_file(c_REG_8KHz)(c_BIT_Pll_1) = '0'
            else vx2rx_8k WHEN reg_file(c_REG_8KHz)(c_BIT_Pll_0) = '0' AND
reg_file(c_REG_8KHz)(c_BIT_Pll_1) = '1'
            else '0';

   ck_8kout <= ck_8kref WHEN reg_file(c_REG_8KHz)(c_BIT_HEADER_8KHz) = '0'
            else ck_pll_out;

   ck_8kout_all <= ck_8kref WHEN reg_file(c_REG_8KHz)(c_BIT_HEADER_8KHz) = '0'
            else ck_pll_out;

   -- This toggles interrupt bits <5..0> c_BIT_xx_xx in register 0x4000 c_REG_INTB
   reg_file(c_REG_INTB)(c_BIT_DX_INT) <= (NOT dx_intb);
   reg_file(c_REG_INTB)(c_BIT_VX1_INT) <= (NOT vx1_intb);
   reg_file(c_REG_INTB)(c_BIT_VX2_INT) <= (NOT vx2_intb);
   reg_file(c_REG_INTB)(c_BIT_AS_INT) <= (NOT as_intb);
   reg_file(c_REG_INTB)(c_BIT_AXHI_INT) <= (NOT axhi_intb);
   reg_file(c_REG_INTB)(c_BIT_AXLO_INT) <= (NOT axlo_intb);

  l_intb <= (NOT ((NOT dx_intb) AND (reg_file(c_REG_INTB)(c_BIT_DX_INT_ENB)))) AND
     (NOT ((NOT vx1_intb) AND  (reg_file(c_REG_INTB)(c_BIT_VX1_INT_ENB)))) AND
     (NOT ((NOT vx2_intb) AND  (reg_file(c_REG_INTB)(c_BIT_VX2_INT_ENB)))) AND
     (NOT ((NOT as_intb) AND   (reg_file(c_REG_INTB)(c_BIT_AS_INT_ENB)))) AND
     (NOT ((NOT axhi_intb) AND (reg_file(c_REG_INTB)(c_BIT_AXHI_INT_ENB)))) AND
     (NOT ((NOT axlo_intb) AND (reg_file(c_REG_INTB)(c_BIT_AXLO_INT_ENB))));

  -- LED15 LEDX4, red, also TP_66, inverted l_intb interrupt to PCI9054; always ON with reset
  ledx4 <= ((NOT rstb) OR NOT ((NOT ((NOT dx_intb) AND
(reg_file(c_REG_INTB)(c_BIT_DX_INT_ENB)) )) AND
    (NOT ((NOT vx1_intb) AND (reg_file(c_REG_INTB)(c_BIT_VX1_INT_ENB) ))) AND
    (NOT ((NOT vx2_intb) AND (reg_file(c_REG_INTB)(c_BIT_VX2_INT_ENB)))) AND
    (NOT ((NOT as_intb) AND (reg_file(c_REG_INTB)(c_BIT_AS_INT_ENB)))) AND
    (NOT ((NOT axhi_intb) AND (reg_file(c_REG_INTB)(c_BIT_AXHI_INT_ENB)))) AND
    (NOT ((NOT axlo_intb) AND (reg_file(c_REG_INTB)(c_BIT_AXLO_INT_ENB))))));

   -- LOS or LCD LEDs, red; always ON with reset
   leds <= reg_file(c_REG_LED)(13 DOWNTO 0);
```

```
    -- LED13 LEDX1, red, all interrupts from chipset together; always ON with reset
    ledx2 <= ((NOT rstb) OR (NOT (dx_intb AND vx1_intb AND vx2_intb AND as_intb AND
axhi_intb AND axlo_intb)));

    -- LED12, LEDX2, red; access to DUPLEX or VORTEX; always ON with reset
    ledx1 <= ((NOT rstb) OR dx_vx_as_readyb);

    -- LED14 LEDX3, red; not connected and not defined

    dx_select <= '1' WHEN (l_la_dec = c_ADDR_DX) ELSE '0';
    vx1_select <= '1' WHEN (l_la_dec = c_ADDR_VX1) ELSE '0';
    vx2_select <= '1' WHEN (l_la_dec = c_ADDR_VX2) ELSE '0';

      dx_vx_rdb <= NOT ((NOT l_w_rb) AND l_bhold);

--  dx_vx_rdb <= '0' WHEN l_w_rb = '0' AND l_bhold = '1' AND ((l_la_dec = c_ADDR_DX)
--  OR (l_la_dec = c_ADDR_VX1) OR (l_la_dec = c_ADDR_VX2)) ELSE '1';

      dx_vx_wrb <= NOT ((l_w_rb) AND l_bhold);

    as_rdb <= '0' WHEN l_w_rb = '0' AND l_bhold = '1' AND (l_la_dec = c_ADDR_AS)
      ELSE '1';
    as_wrb <= '0' WHEN l_w_rb = '1' AND l_bhold = '1' AND (l_la_dec = c_ADDR_AS)
      ELSE '1';

    vx_dx_a <= l_la;

    ax_adsb <= '0' WHEN (l_adsb = '0') AND (l_la_dec = c_ADDR_AX)
      ELSE '1';
    ax_csb <= '0' WHEN (l_adsb = '0') AND (l_la_dec = c_ADDR_AX)
      ELSE '1';
    ax_wr <= l_w_rb;
    ax_burstb <= '0' WHEN (l_la_dec = c_ADDR_AX) AND (l_bhold = '1') ELSE '1';

    -- ax_burstb <= '1';
    ax_blast <= l_blastb WHEN (l_la_dec = c_ADDR_AX) AND (l_bhold = '1') ELSE '1';

    l_btermb <= ax_btermb WHEN (l_la_dec = c_ADDR_AX) AND (l_bhold = '1') ELSE '1';
    l_readyb <= ((ax_readyb AND dx_vx_as_readyb) OR l_denb);

   PROCESS (rstb, l_clk1)
   VARIABLE timer : INTEGER RANGE 0 TO 31;
    BEGIN
      IF (rstb = '0') THEN
            dvas_readyb <= '1';
            dx_csb <= '1';
```

```
vx1_csb <= '1';
vx2_csb <= '1';
as_csb <= '1';
dx_vx_as_readyb <= '1';
timer := 0;
-- Bits 5 downto 0 are set by PMC Devices' INTB output lines.
reg_file(c_REG_INTB)(15 DOWNTO 6) <= "0000000000";
reg_file(c_REG_8KHz) <= "0000000000000000";
reg_file(c_REG_LED) <= "0011111111111111";

ELSIF (l_clk1'EVENT AND l_clk1 = '1') THEN
 IF l_adsb = '0' THEN
  timer := 0;
  dx_vx_as_readyb <= '1';
 ELSE
  IF timer < 31 THEN
   timer := timer + 1;
  END IF;
 END IF;

 CASE l_la_dec IS
  WHEN c_ADDR_DX =>
   IF l_adsb = '0' THEN
        dx_csb <= '0';
   END IF;

   IF l_w_rb = '0' THEN
        IF timer = 2 THEN
      dx_vx_as_readyb <= '0';
     ELSIF timer = 3 THEN
         dx_csb <= '1';
        END IF;
   ELSE
        IF timer = 2 THEN
         dx_csb <= '1';
         dx_vx_as_readyb <= '0';
        END IF;
   END IF;

  WHEN c_ADDR_VX1 =>
   IF l_adsb = '0' THEN
        vx1_csb <= '0';
   END IF;

   IF l_w_rb = '0' THEN
        IF timer = 2 THEN
```

```
            dx_vx_as_readyb <= '0';
          ELSIF timer = 3 THEN
            vx1_csb <= '1';
          END IF;
      ELSE
          IF timer = 2 THEN
            vx1_csb <= '1';
            dx_vx_as_readyb <= '0';
          END IF;
      END IF;

    WHEN c_ADDR_VX2 =>
      IF l_adsb = '0' THEN
          vx2_csb <= '0';
      END IF;

      IF l_w_rb = '0' THEN
          IF timer = 2 THEN
            dx_vx_as_readyb <= '0';
          ELSIF timer = 3 THEN
            vx2_csb <= '1';
          END IF;
      ELSE
          IF timer = 2 THEN
            vx2_csb <= '1';
    dx_vx_as_readyb <= '0';
          END IF;
      END IF;

     WHEN c_ADDR_AS =>
       IF l_adsb = '0' THEN
           as_csb <= '0';
       END IF;

          IF as_busyb = '1' THEN
            IF l_w_rb = '0' THEN
              IF timer = 2  THEN
                dx_vx_as_readyb <= '0';
              ELSIF timer = 3  THEN
                as_csb <= '1';
              END IF;
            ELSE
              IF timer = 2 THEN
                as_csb <= '1';
                dx_vx_as_readyb <= '0';
              END IF;
```

```
            END IF;
          ELSE
            IF timer > 0 THEN
              timer := timer - 1;
            END IF;
          END IF;

        WHEN c_ADDR_CPLD =>
          IF l_w_rb = '1' THEN
            IF timer = 1 THEN
              dx_vx_as_readyb <= '0';
                CASE l_la IS
                  WHEN c_REG_ADDR_INTB =>
                    reg_file(c_REG_INTB)(15 DOWNTO 6) <= l_ad(15 DOWNTO 6);
                  WHEN c_REG_ADDR_LED =>
                    reg_file(c_REG_LED) <= l_ad;
                  WHEN c_REG_ADDR_8KHz =>
                    reg_file(c_REG_8KHz) <= l_ad;

                  WHEN OTHERS =>
                  END CASE;
              END IF;
          ELSE
              IF timer = 1 THEN
                dx_vx_as_readyb <= '0';
              END IF;
            END IF;
          WHEN OTHERS =>
          END CASE;
      END IF;
 END PROCESS;
END;
```

19. APPENDIX F: BILL OF MATERIAL

Table 9 shows the bill of material (BOM) for the Core Card.

TABLE 9. Core Card BOM

Item	Description	Vendor Part No.	Reference Designator	Qty
1.	CAPACITOR-1.0 uF, 16 V, Y5V_805 *** due to assembly process, some boards may be assembled with 0.22 uF (read below for more info)	any	C114-C145, C179-C188, C193-C214, C244-C251	72
2.	CAPACITOR-0.1 uF, 16 V, X7R_603	any	C2, C3, C80, C86, C146-C153, C174-C178, C189, C190, C192, C215-C227, C229, C233, C236, C237, C240, C241, C260, C261	41
3.	CAPACITOR-4.7 uF, 10 V, TANT TEH	any	C235, C238	2
4.	CAPACITOR-68 uF, 6.3 V, TANT TEH	any	C239	1
5.	CAPACITOR-0.01 uF, 16 V, X7R_402	any	C5, C6, C8, C10-C16, C18-C29, C31, C32, C34-C53, C57-C79, C81-C83, C89, C92, C93, C96-C101, C103-C113, C154, C155, C158, C159, C162-C173, C191, C228, C231, C254, C255, C258, C259, C262, C263, C266-C272, C276, C279-C305, C307-C313	157
6.	METALIZED FILM CAPACITOR, 0.015 uF, 16 V, 1206	PCF1078CT-ND (Digi-Key)	C85, C88	2
7.	CAPACITOR-22 uF, 6.3V, TANT TE	any	C4, C9, C17, C30, C33, C54-C56, C91, C94, C95, C102, C156, C157, C160, C161, C230, C232, C234, C242, C243, C252, C253, C256, C257, C264, C265, C273-C275, C277, C278	32
8.	ZENER DIODE, 150 mW, 10V, SMD	any	D1, D2	2
9.	LED, SMD, RED	any	D8, D12-D15	5
10.	SCHOTTKY BARRIER RECTIFIER, 3 A, 20 V, SMD	SK32DI (digi-Key)	D3, D11	2
11.	QUAD YELLOW/RED/GREEN/ GREEN LED.	SSF-LXH5147LYIGGD (Lumex)	D4	1
12.	QUAD RED LED.	SSF-LXH5147IIIID (Lumex)	D5-D7	3
13.	SHOTTKY DIODE, LOW CURRENT, 30 mA, 0.30 V, SMD	MA732CT	D8	1
14.	T-1 3/4 LED BLUE VERTICAL PCB MOUNT	LNG995PF9 (PANASONIC)	D9	1
15.	CONNECTOR ZPACK CPCI 2MM HM 110 POS. TYPE A WITH GND SHIELD	352068-1 (AMP)	J1	1
16.	CONNECTOR ZPACK CPCI 2MM HM 110 POS., TYPE B WITH GND SHIELD	352152-1 (AMP)	J5	
17.	HEADER 2, 0.1” SPACING	any	J45, J65, J72, J73, J74	5
18.	HEADER 2X4 100MIL MALE	any	J36	1
19.	IEEE 1394-1995 SHIELD RIGHT ANGLE, 2 mm PIN SPACING	53460-0611 (MOLEX)	J46-J63	18
20.	3-PIN HEADER. 0.1” SPACING	any	J64	1
21.	6-PIN HEADER. 0.1” SPACING	any	J66	1

22.	HEADER 1X3, 2 mm	any	J6-J35, J37-J44, J67, J68	40
23.	HEADER, 1x3, 1.25 mm, MOLEX	53047-0310	TP115	1
24.	Ejector handle microswitch, MOLEX	20817-500		1
25.	OPTIONAL: 38 PIN SIGNAL CONNECTOR, MATCHED iMPEDANCE, 0.025, SMD	2-767004-2 (AMP)	OPTIONAL TEST CONNECTORS: J70, J71	2
26.	GENERAL PURPOSE TRANSISTOR, NPN, SOT-23	MMBT3904LT1 (MOT)	Q1	1
27.	GENERAL PURPOSE TRANSISTOR, PNP, SOT-23	MMBT3906LT1 (MOT)	Q4	1
28.	MOSFET, LOW VOLTAGE	ZXM61N0 2F	Q5, Q6, Q7	3
29.	0.007 OHM, 20 V, HEXFET POWER MOSFET	IRL3502S (IR)	Q2	1
30.	0.047 OHM, 30 V, POWER MOSFET	DI9410	Q3	1
31.	RESISTOR-56, 5 %, 603	any	R16, R23, R28, R32-R35, R39-R41, R55-R61, R66, R192, R199, R201, R204, R206, R210, R216, R262, R282-R287, R300, R311, R315, R316, R323, R325, R343, R348	40
32.	RESISTOR-750, 5 %, 603	any	R106, R108, R110, R112, R114, R116, R118, R120, R176, R178, R180, R182, R184, R186, R188, R190, R239, R240	18
33.	RESISTOR-100 k, 5 %, 603	any	R18, R317, R351	3
34.	RESISTOR-200, 5 %, 603	any	R195, R196	2
35.	RESISTOR-22, 5 %, 603	any	R197, R219, R308-R310, R312, R334	7
36.	RESISTOR-330, 5 %, 603	any	R2, R46, R49, R123, R211, R217, R230, R259, R277-R279, R307, R326, R328, R329	15
37.	RESISTOR-2.2 k, 5 %, 603	any	R205	1
38.	RESISTOR-1.0 k, 5 %, 603	any	R43, R156, R203, R207, R245, R252, R256, R330	8
39.	RESISTOR-7.5 M, 5 %, 805	any	R215	1
40.	RESISTOR-1.00 M, 1 %, 603	any	R22, R36, R37, R45, R47, R62-R65, R67-R84, R87-R89, R128-R154, R157-R159, R193, R194, R212-R214, R296, R297, R299, R303-R306	72
41.	RESISTOR-820, 5 %, 603	any	R220, R241, R254, R288, R289	5
42.	RESISTOR-15 k, 5 %, 603	any	R6, R353	2
43.	RESISTOR-220, 5 %, 603	any	R29, R232	2
44.	RESISTOR-100, 5 %, 603	any	R233, R246-R251, R263-R265, R267-R269, R271-R273	16
45.	RESISTOR-3.0 k, 5 %, 603	any	R243	1
46.	RESISTOR-20, 5 %, 603	any	R281, R295	2
47.	RESISTOR-220, 5 %, 603	any	R29, R232	2
48.	RESISTOR-470, 5 %, 603	any	R224, R301, R302, R313, R314	5
49.	RESISTOR-560, 5 %, 603		R227	1
50.	RESISTOR-0.01, 5 %, 2714	any	R30, R200 (recommended to decrease R200 to 0.005 ohm)	2
51.	RESISTOR-0, 5 %, 603	any	R198, R333, R336, R337, R340-R342, R355, R27, R44, R51, R124, R125, R221, R231, R274	16
52.	RESISTOR-0, 5 %, 0805	any	R54, R127, R234	3

53.	RESISTOR-4.7, 5 %, 0805	any	R42, R126, R244	3
54.	RESISTOR-10 M, 5 %, 1206	any	R319-R321	3
55.	RESISTOR-10, 5 %, 603	any	R335	1
56.	RESISTOR-49.9, 1 %, 603	any	R38, R85, R86, R91, R93, R95, R97, R99, R101, R103, R105, R107, R109, R111, R113, R115, R117, R119, R121, R161, R163, R165, R167, R169, R171, R173, R175, R177, R179, R181, R183, R185, R187, R189, R191, R235, R236	37
57.	RESISTOR-4.7 k, 5%, 603	any	R1, R3-R5, R7-R15, R17, R19, R20, R24-R26, R50, R155, R202, R208, R209, R222, R223, R225, R226, R228, R229, R242, R253, R257, R260, R266, R270, R275, R276, R280, R291-R294, R298, R324, R327, R338, R339, R346, R349, R352, R354, R356, R390, R391	55
58.	RESISTOR-4.75 k, 1 %, 603	any	R48, R122, R290	3
59.	RESISTOR-4.12 k, 1 %, 603	any	R52	1
60.	RESISTOR-430, 5 %, 603	any	R90, R92, R94, R96, R98, R100, R102, R104, R160, R162, R164, R166, R168, R170, R172, R174, R237, R238	18
61.	RES_ARRAY_4_SMD-4.7 k	any	RN1, RN6, RN7, RN12-RN17, RN38, RN86, RN89	12
62.	RES_ARRAY_4_SMD-22	any	RN2, RN3, RN25, RN27-RN30, RN32-RN34, RN36, RN37, RN39-RN41, RN52, RN54, RN55, RN60-RN62, RN64, RN68, RN85, RN91, RN92, RN99, RN100, RN102, RN104-RN10 7, RN111-RN13 5	58
63.	RES_ARRAY_4_SMD-2.2 k	any	RN20, RN67, RN69, RN70	4
64.	RES_ARRAY_4_SMD-56	any	RN4, RN5, RN8-RN11, RN18, RN19, RN21-RN24, RN26, RN31, RN35, RN42-RN51, RN53, RN56-RN59, RN87, RN108-RN110, RN136-RN139	38
65.	RES_ARRAY_4_SMD-330	any	RN63	1
66.	RES_ARRAY_4_SMD-15 k	any	RN65, RN66, RN84, RN88, RN90, RN93-RN98, RN101, RN103	13
67.	RES_ARRAY_4_SMD-10	any	RN71-RN83, RN140	14
68.	S/UNI-ATLAS LAYER SOLUTION	PM7324 DI (PMC-Sierra, Inc.)	U1	1
69.	S/UNI-APEX ATM TRAFFIC MANAGER	PM7326 BI (PMC-Sierra, Inc.)	U7	1
70.	S/UNI-VORTEX	PM7351-BI (PMC-Sierra, Inc.)	U19, U20	2
71.	S/UNI-DUPLEX	PM7350-BI (PMC-Sierra, Inc.)	U27	1
72.	3.3 V, 100 MHz, 8MB NBT SRAM (512 k x 18), 119-PBGA	GS882Z18B-100 (GSI)	U10, U12	2
73.	VERY HIGH SPEED, QUAD BUFFER WITH THREE STATE OUTPUTS	SN74ALVC125D (TI)	U17, U25, U26	3
74.	PROGRAMMABLE CLOCK RECOVERY PLL, 20-PIN SMD	MK2049-01S (ICS Microclock)	U13	1
75.	FAIRCHILD 4 kbit SERIAL EEPROM, 8_PIN DIP, SOCKET, 8-PIN DIP	NM93CS66EN (Fairchild)	U14	1
76.	DUAL HOT SWAP CONTROLLER	LTC1645CS8 (LT)	U16	1
77.	+5 V and 3.3 V SUPERVISING	LTC1326CMS8 (LT)	U11	1

	CIRCUIT			
78.	LOW VOLTAGE OP-AMP, RAIL-TO-RAIL IN/OUT, SOIC8 PACKAGE	TLV2461CD (TI)	U18	1
79.	DUAL 1-TO-5 CLOCK BUFFER	QS53805 (Quality Smi.)	U2, U3	2
80.	REGULATOR, 2.5 V, 800 mA, POSITIVE, LOW DROPOUT	LT1118CST-2.5 (LT)	U21	1
81.	MINI-LOGIC, AND GATE, IN SSOP5 PACKAGE, 0.95 MM PIN-SPACING, 3.3 V TO 5 V	TC7S08FCT (Toshiba)	U22, U23	2
82.	PCI I/O ACCELERATOR	PCI9054-AA50PI (PLX)	U15	1
83.	IN-SYSTEM PROGRAMMABLE CPLD, 288 MICROCELLS	XC95288XL-10TQ144 C (Xilinx)	U31	1
84.	3.3V, 100 MHz, 1MB SSRAM (512 k x 36)	GS88036T-100 (GSI)	U4-U6	3
85.	3.3 V, 100 MHz, 8 Mbit SDRAM (1Mbit x 4 BANKS x 16 WIDE)	MT48LC4M16A2-75 (Micron)	U8, U9	2
86.	EPSON 12.288 MHz CRYSTAL	MA-505-12.288M-C2 (Epson)	Y1	1
87.	OSCILLATOR, 50 MHz, 3.3 V, 50PPM	CB3LV-3C-50.0000- T	Y2	1
88.	OSCILLATOR, 25 MHz, 3.3 V, 50PPM	CB3LV-3C-25.0000- T	Y3, Y5	2
89.	OSCILLATOR, 80 MHz, 3.3 V, 50PPM	CB3LV-3C-80.0000- T	Y4	1
90.		N/u	C1, C7, C84, C87, C90	
91.		N/u	R21, R31, R53, R218, R255, R258, R261, R318, R322, R331, R332, R344, R345, R347, R350	
92.		N/u	L1, Q4	
93.		Not a part – pads for optional wire strapping	DP1, DP2, ZQ1, ZQ2	
94.		Not a part – optional test pads, mounting holes, or wiring pads	A0, ADSC1, ADSC2, AS_ICLK, BA0, BA1, CAS, CE1, CKL3, CLK, CLK4, CMA0, CMD0, CS, DQ, DQ0, D_CLK, ESA0, ESA16, ESD0, ESP0, GND1-GND4, GW1, GW2, ISA0, ISA16, ISD0, ISP0, OE1, OE2, RAS, RW, TP1-TP3, TP7-TP17, TP21-TP32, TP35-TP37, TP42-TP49, TP66-TP69, TP72-TP76, TP78, TP79, TP81-TP117 , TP_2.5V, TP_3.3V, TP_RSTB, TP_VCC, WE, DP1, DP2, FT1, FT2, JP1-JP4, JP8, JP9, JP11-JP13, JP16-JP18, VDD1, VDD2, ZQ1, ZQ2 M1, P1	
95.				

***/ Due to assembly process, some boards may have serial LVDS capacitors assembled with 0.22 uF. It is recommended to observe baseline wander in real systems, and possibly increase capacitor value to 1.0 uF. That may be especially important if LVDS is run at slower speed, i.e. 100 Mbps (our Core Card runs at 200 Mbps).

20. APPENDIX G: SCHEMATIC DIAGRAMS

The Core Card schematic pages are organized by blocks, as shown in the “Core Card Root Drawing”, page 1. Each block may have one or two pages. If two pages are in a single block, then each page has the additional number 1 or 2 shown on each page title, for example, S/UNI-APEX 1 and S/UNI-APEX 2.

The interconnections between blocks are marked with the suffix “\I”, for example, RSTB\I, L_AD<31..0>\I, etc. Interconnections on the same page or between two pages in the same block do not have the suffix, for example, L_BTERMB, L_DENB, etc: All interconnections with the suffix “\I” on individual pages are shown in “Core Card Root Drawing” on page 1. However, page 1 netlists do not show the suffix “\I” (the way Concept CAD tool works).
Single page or single block connections are not shown on page 1.

Page 1: Root drawing with interconnections between blocks.

Page 2 – FRONT: IEEE 1394 LVDS connectors, front panel LEDs, blue LED and ejector switch header

Page 3 – S/UNI-VORTEX2 BLOCK: S/UNI-VORTEX 2, page 1, digital sub-blocks and power.

Page 4 – S/UNI-VORTEX2 BLOCK: S/UNI-VORTEX 2, page 2, LVDS ports.

Page 5 – S/UNI-DUPLEX: S/UNI-DUPLEX, LVDS ports, digital sub-blocks and power.

Page 6 – S/UNI-VORTEX1 BLOCK: S/UNI-VORTEX 1, page 1, digital sub-blocks and power.

Page 7 – S/UNI-VORTEX1 BLOCK: S/UNI-VORTEX 1, page 2, LVDS ports.

Page 8 – S/UNI-APEX BLOCK: S/UNI-APEX 1, page 1, digital sub-blocks and power.

Page 9 – S/UNI-APEX BLOCK: S/UNI-APEX 1, page 2, RAM interfaces.
The RAM size for the S/UNI-APEX is shown for exercise purposes only. The circuit supports the BGA package. The smaller size NBT (ZBT) SSRAMs may be available in TQFP packages only. The RAM size for the S/UNI-APEX should be calculated as explained in [7] and [12], depending on the system requirements.

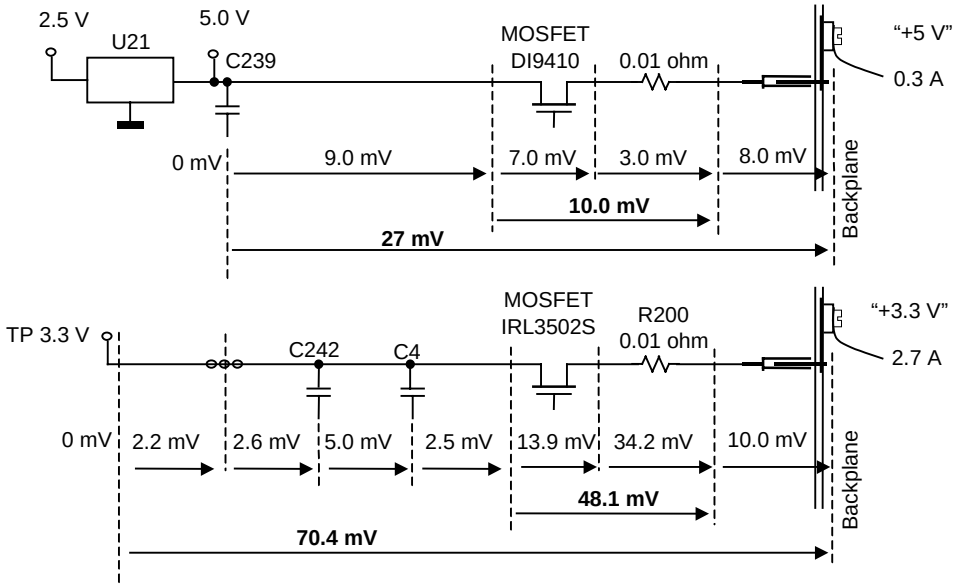
Page 10 – S/UNI-ATLAS BLOCK: S/UNI-ATLAS 1, page 1, digital sub-blocks and power.

Page 11 – S/UNI-ATLAS BLOCK: S/UNI-ATLAS 2, page 2, RAM interfaces.

Page 12 – J1, PCI, PCI9054 & CPLD: PCI_CPLD 1, page 1, cPCI interface over J1 and PCI9054 bridge.

Page 13 – J1, PCI, PCI9054 & CPLD: PCI_CPLD 2, page 2, CPLD, 8 kHz PLL, test connectors.

Page 14 – J5 CONNECTOR: J5 LVDS connector, Hot-Swap circuit, RESET. Resistor R200 should be decreased to 0.005 ohm to have lower voltage drop.



The hot swap controlling elements introduce 48.1 mV voltage drop for 3.3 V rail. . That is too close to current sensing threshold on LTC1645.

Page 15 – Signal cross-reference**:** Optional page helping finding netlists names.

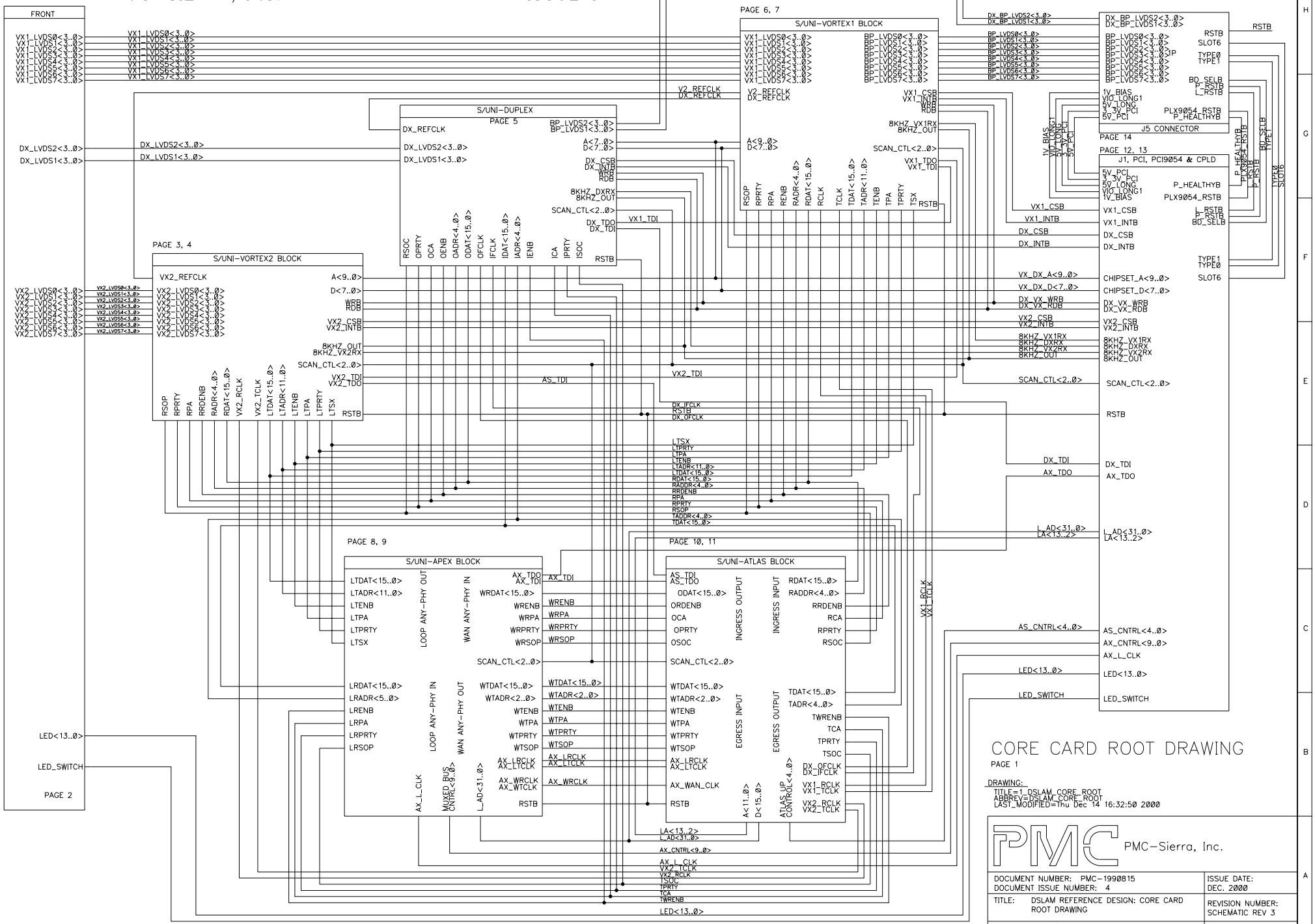
Page 16 – Component cross-reference**:** Optional page to help find components names.

Page 17 – Component cross-reference**:** Optional page to help find components names.

Page 18 – Component cross-reference**:** Optional page to help find components names.

DSLAM REFERENCE DESIGN: CORE CARD
PMC–SIERRA, INC. ISSUE 3

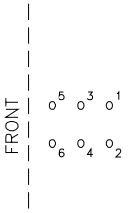
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

ALL LVDS LINES 50 OHM

FRONT



2MM J46 — MOLEX 53460-0611
TXD1+ / TXD1− / RXD1+ / RXD1− → VX1_LVDS1<3..0>\I → 7F10<>

2MM J47 — MOLEX 53460-0611
TXD3+ / TXD3− / RXD3+ / RXD3− → VX1_LVDS3<3..0>\I → 7E10<>

2MM J48 — MOLEX 53460-0611
TXD5+ / TXD5− / RXD5+ / RXD5− → VX1_LVDS5<3..0>\I → 7C10<>

2MM J49 — MOLEX 53460-0611
TXD7+ / TXD7− / RXD7+ / RXD7− → VX1_LVDS7<3..0>\I → 7A10<>

2MM J54 — MOLEX 53460-0611
TXD0+ / TXD0− / RXD0+ / RXD0− → VX1_LVDS0<3..0>\I → 7G10<>

2MM J55 — MOLEX 53460-0611
TXD2+ / TXD2− / RXD2+ / RXD2− → VX1_LVDS2<3..0>\I → 7F10<>

2MM J56 — MOLEX 53460-0611
TXD4+ / TXD4− / RXD4+ / RXD4− → VX1_LVDS4<3..0>\I → 7D10<>

2MM J57 — MOLEX 53460-0611
TXD6+ / TXD6− / RXD6+ / RXD6− → VX1_LVDS6<3..0>\I → 7B10<>

S/UNI−VORTEX1 LVDS

S/UNI−VORTEX2 LVDS

2MM J50 — MOLEX 53460-0611
TXD1+ / TXD1− / RXD1+ / RXD1− → VX2_LVDS1<3..0>\I → 4G10<>

2MM J51 — MOLEX 53460-0611
TXD3+ / TXD3− / RXD3+ / RXD3− → VX2_LVDS3<3..0>\I → 4E10<>

2MM J52 — MOLEX 53460-0611
TXD5+ / TXD5− / RXD5+ / RXD5− → VX2_LVDS5<3..0>\I → 4C10<>

2MM J53 — MOLEX 53460-0611
TXD7+ / TXD7− / RXD7+ / RXD7− → VX2_LVDS7<3..0>\I → 4B10<>

2MM J58 — MOLEX 53460-0611
TXD0+ / TXD0− / RXD0+ / RXD0− → VX2_LVDS0<3..0>\I → 4G10<>

2MM J59 — MOLEX 53460-0611
TXD2+ / TXD2− / RXD2+ / RXD2− → VX2_LVDS2<3..0>\I → 4F10<>

2MM J60 — MOLEX 53460-0611
TXD4+ / TXD4− / RXD4+ / RXD4− → VX2_LVDS4<3..0>\I → 4D10<>

2MM J61 — MOLEX 53460-0611
TXD6+ / TXD6− / RXD6+ / RXD6− → VX2_LVDS6<3..0>\I → 4B10<>

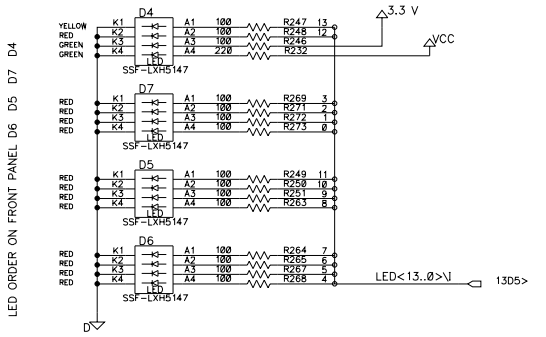
LVDS CONNECTORS MOUNTED ON FRONT PANEL

2MM J63 — MOLEX 53460-0611
TXD0+ / TXD0− / RXD0+ / RXD0− → DX_LVDS1<3..0>\I → 5G10>

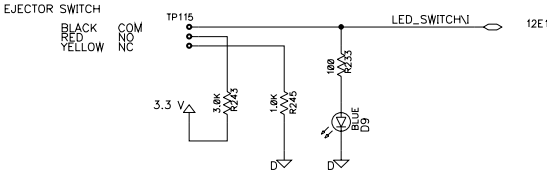
2MM J62 — MOLEX 53460-0611
TXD0+ / TXD0− / RXD0+ / RXD0− → DX_LVDS2<3..0>\I → 5E10>

S/UNI−DUPLEX LVDS

LEDS



EJECTOR SWITCH AND BLUE LED



FRONT PANEL

DRAWING

TITLE=2_FRONT
ABBREV=FRONT
LAST_MODIFIED=Thu Dec 14 16:58:35 2000

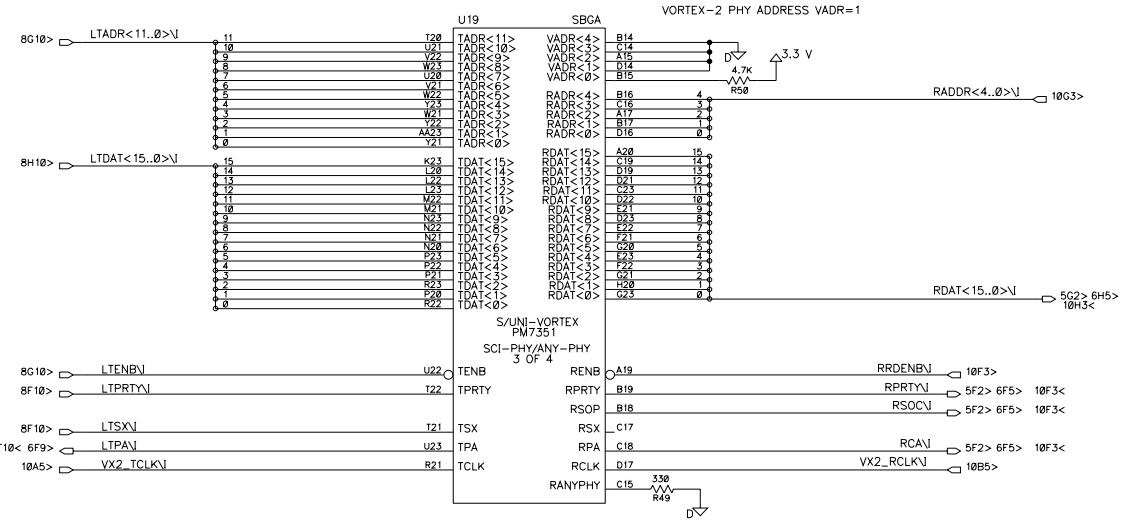
PMC-Sierra, Inc.

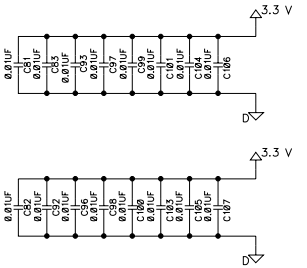
DOCUMENT NUMBER: PMC-1990815 DOCUMENT ISSUE NUMBER: 4	ISSUE DATE: DEC. 2000
TITLE: DSLAM REFERENCE DESIGN: CORE CARD FRONT PLATE INTERFACE	REVISION NUMBER: SCHEMATIC REV 3
ENGINEER: PMC/WT	PAGE: 2 OF 14

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

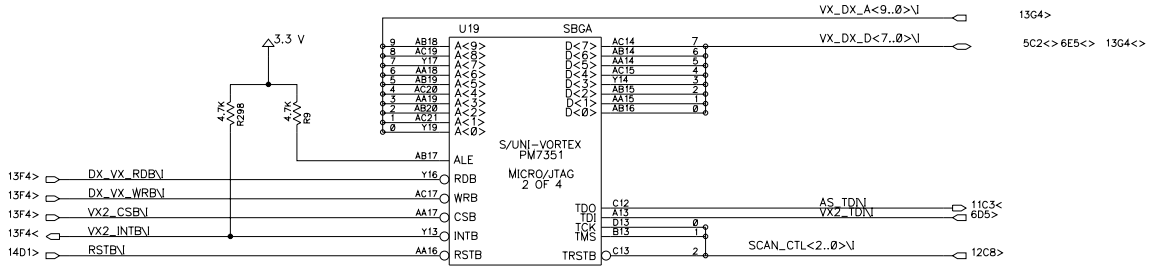
TO S/UNI-APEX LOOOP ANY/PHY TX MASTER

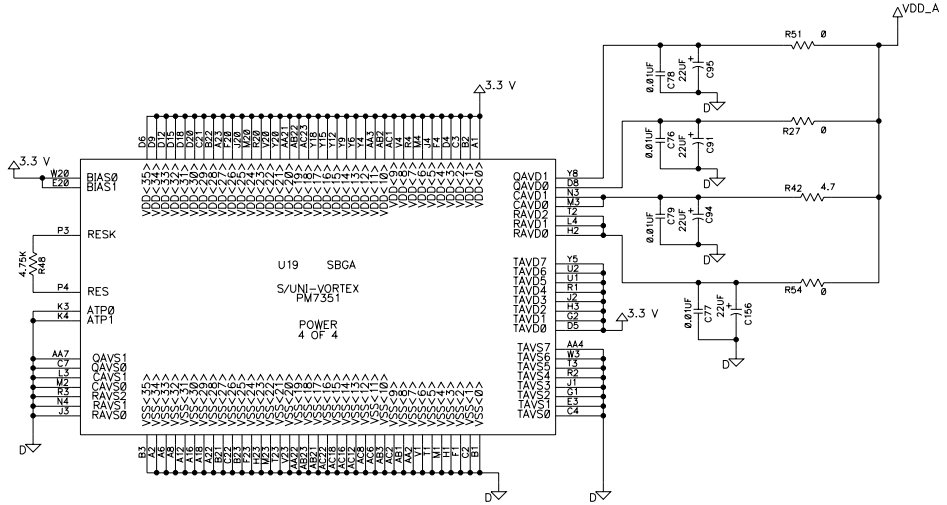
TO S/UNI-ATLAS INGRESS IN MASTER





ALTERNATE CAPS ON SUNI-DUPLEX VDD PINS





FILTERING RESISTORS FOR
QAVD, RAVD AND TAVD
CAN BE SHORTED TO 3.3 V RAIL.
LOW NOISE 3.3 V RAIL RECOMMENDED.

NOTE: PLACE FILTER NETWORKS AS PHYSICALLY CLOSE TO THE DEVICE AS POSSIBLE.

DRAWING

TITLE=3_VORTEX_2_BLOCK
ABBREV=VORTEX2
LAST_MODIFIED=Thu Dec 14 16:58:25 2000

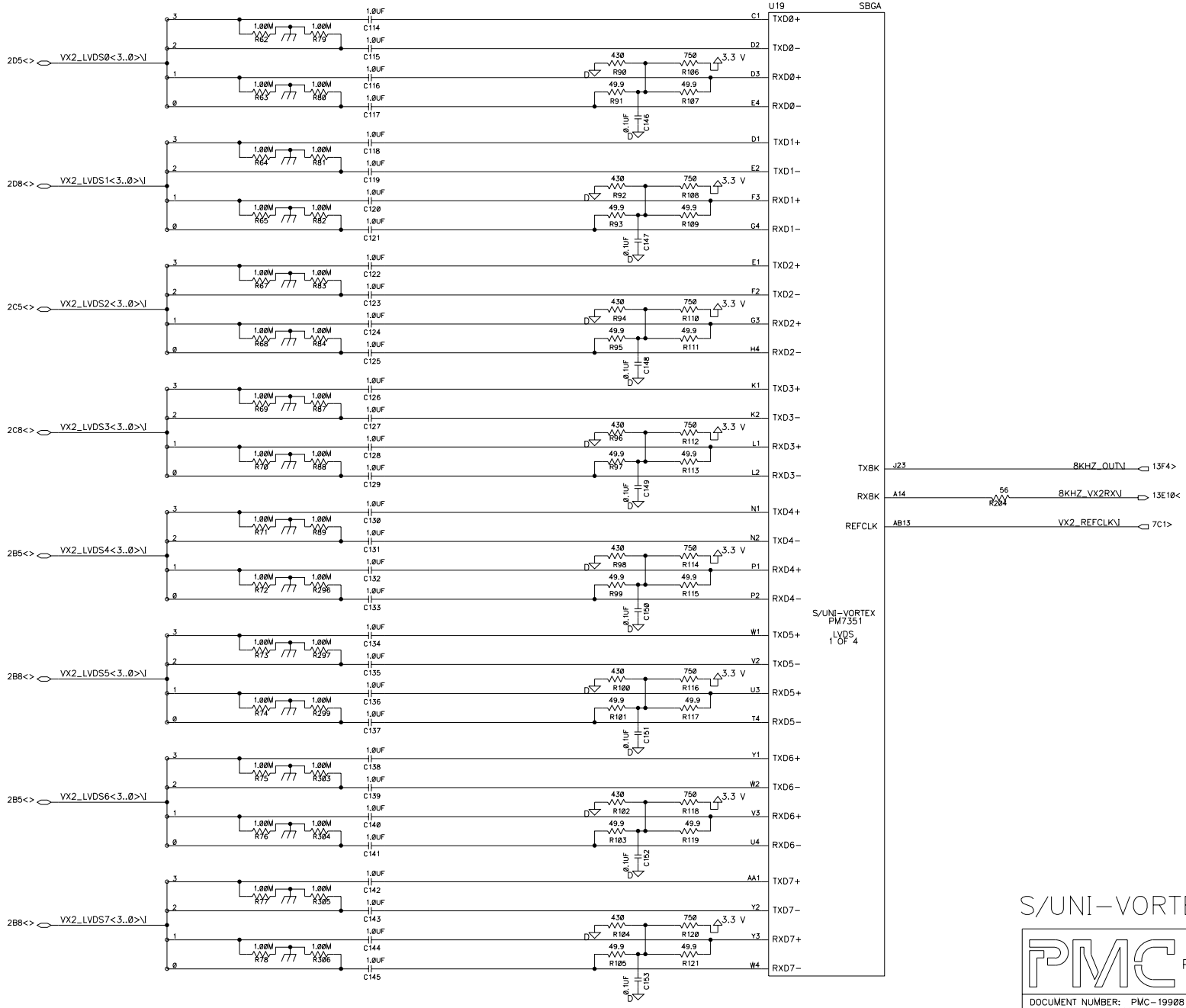
S/UNI-VORTEX2.1

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1990815 DOCUMENT ISSUE NUMBER: 4	ISSUE DATE: DEC. 2000
TITLE: DSLAM REFERENCE DESIGN: CORE CARD S/UNI-VORTEX2 BLOCK	REVISION NUMBER: SCHEMATIC REV 3
ENGINEER: PMC/WT	PAGE: 3 OF 14

ALL LVDS TRACES 50 OHM

LVDS CONNECTORS MOUNTED ON FRONT PANEL



DRAWING

TITLE=3_VORTEX_2_BLOCK
ABBREV=VORTEX2
LAST_MODIFIED=Thu Dec 14 16:58:30 2000

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPR

S/UNI-VORTEX2.2

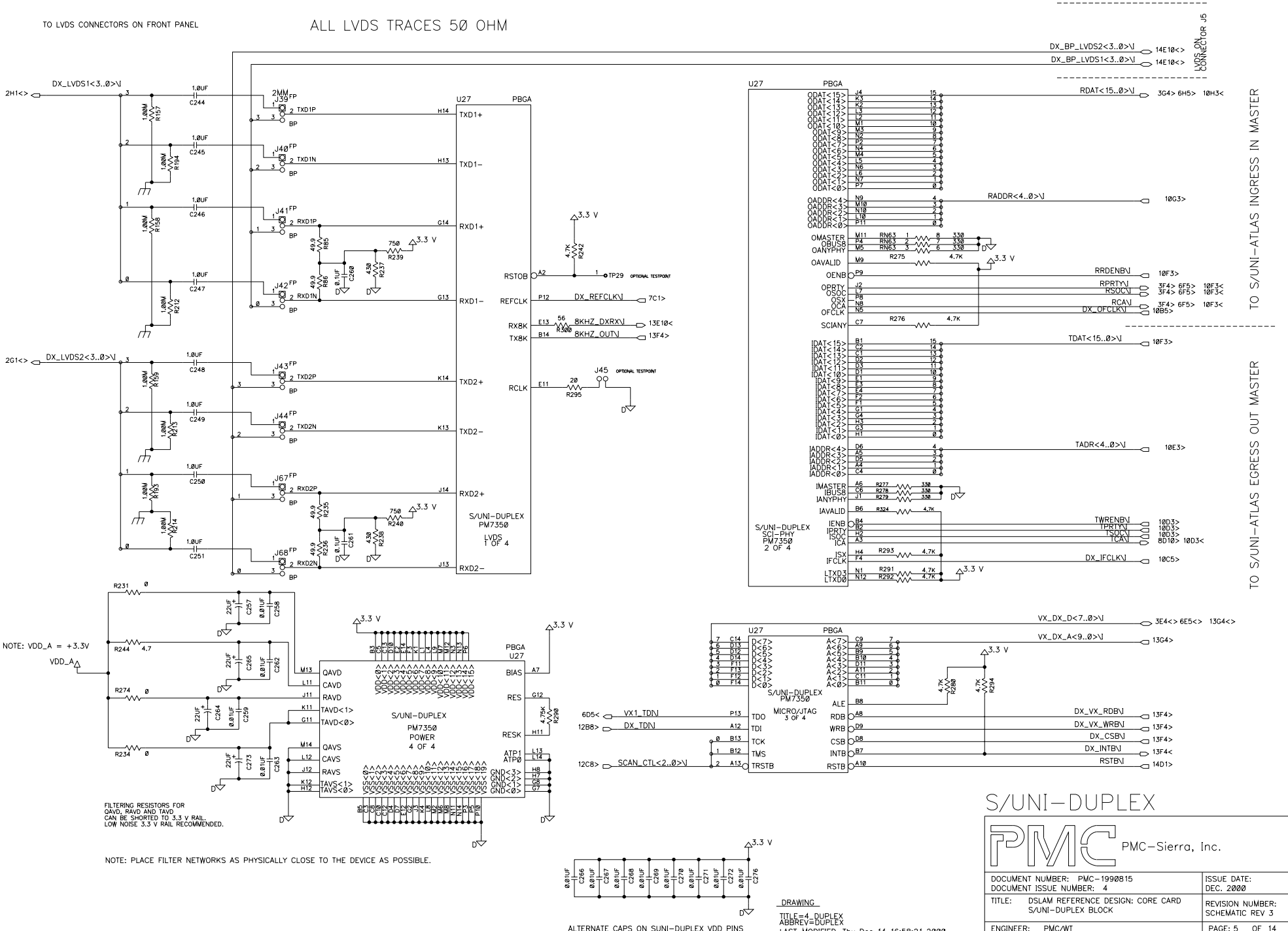
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1990815 DOCUMENT ISSUE NUMBER: 4	ISSUE DATE: DEC. 2000
TITLE: DSLAM REFERENCE DESIGN: CORE CARD S/UNI-VORTEX2 LVDS INTERFACE	REVISION NUMBER: SCHEMATIC REV 3
ENGINEER: PMC/WT	PAGE: 4 OF 14

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

TO LVDS CONNECTORS ON FRONT PANEL

ALL LVDS TRACES 50 OHM



S/UNI-DUPLEX

PMC-Sierra, Inc.

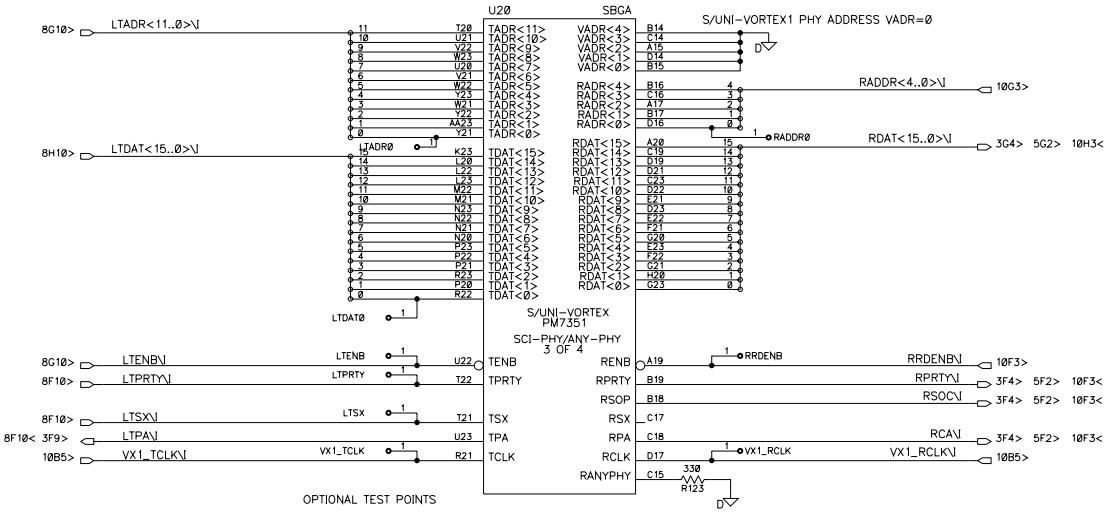
DOCUMENT NUMBER: PMC-1990815 DOCUMENT ISSUE NUMBER: 4	ISSUE DATE: DEC. 2000
TITLE: DSLAM REFERENCE DESIGN: CORE CARD S/UNI-DUPLEX BLOCK	REVISION NUMBER: SCHEMATIC REV 3
ENGINEER: PMC/WT	PAGE: 5 OF 14

DRAWING

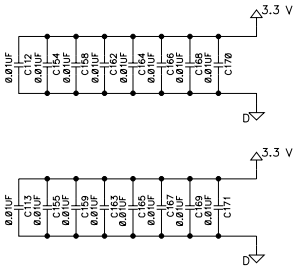
TITLE=4_DUPLEX
ABBREV=DUPLEX
LAST_MODIFIED=Thu Dec 14 16:58:21 2000

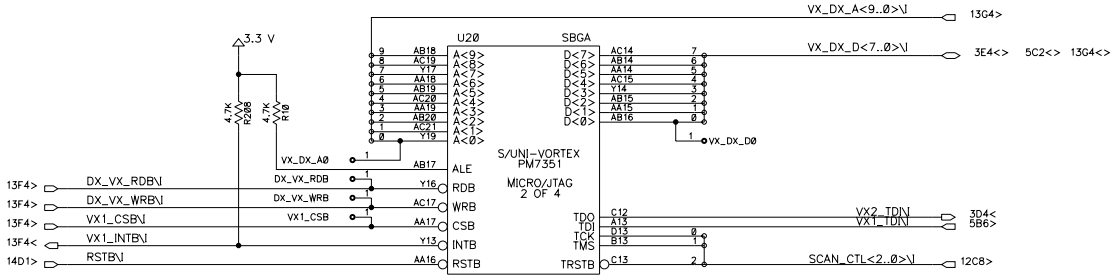
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

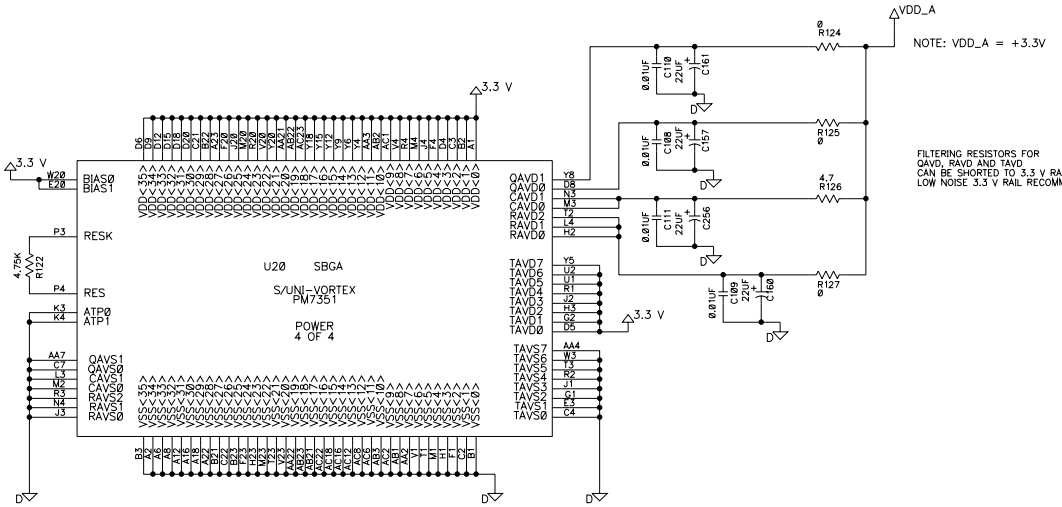
TO S/UNI-APEX LOOOP ANY/PHY TX MASTER



TO S/UNI-ATLAS INGRESS IN MASTER







NOTE: PLACE FILTER NETWORKS AS PHYSICALLY CLOSE TO THE DEVICE AS POSSIBLE.

DRAWING

TITLE=5_VORTEX_1_BLOCK
ABBREV=VORTEX1
LAST_MODIFIED=Thu Dec 14 16:58:07 2000

S/UNI-VORTEX1.1

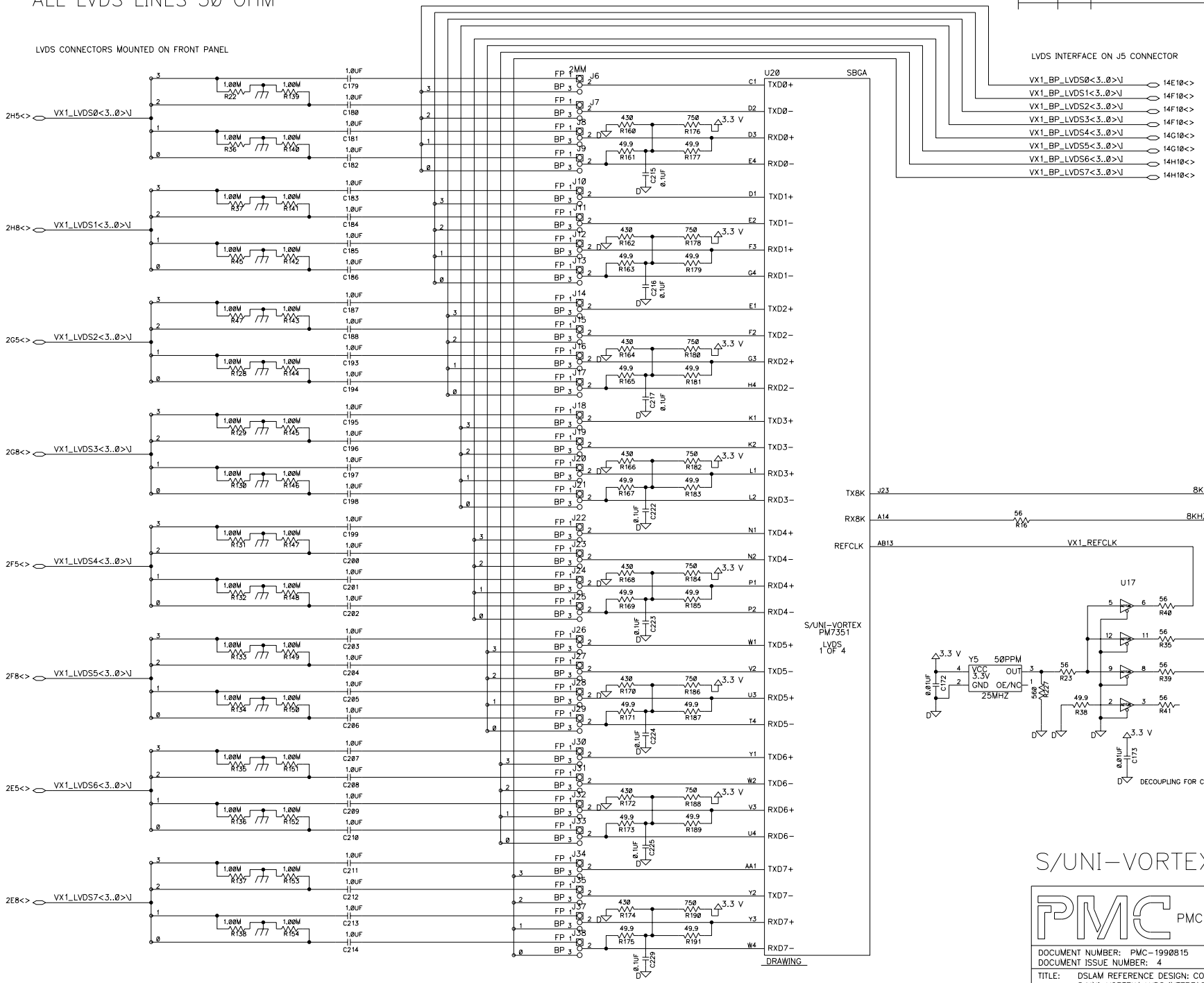
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1990815 DOCUMENT ISSUE NUMBER: 4	ISSUE DATE: DEC. 2000
TITLE: DSLAM REFERENCE DESIGN: CORE CARD S/UNI-VORTEX1 BLOCK	REVISION NUMBER: SCHEMATIC REV 3
ENGINEER: PMC/WT	PAGE: 6 OF 14

ALL LVDS LINES 50 OHM

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

LVDS CONNECTORS MOUNTED ON FRONT PANEL

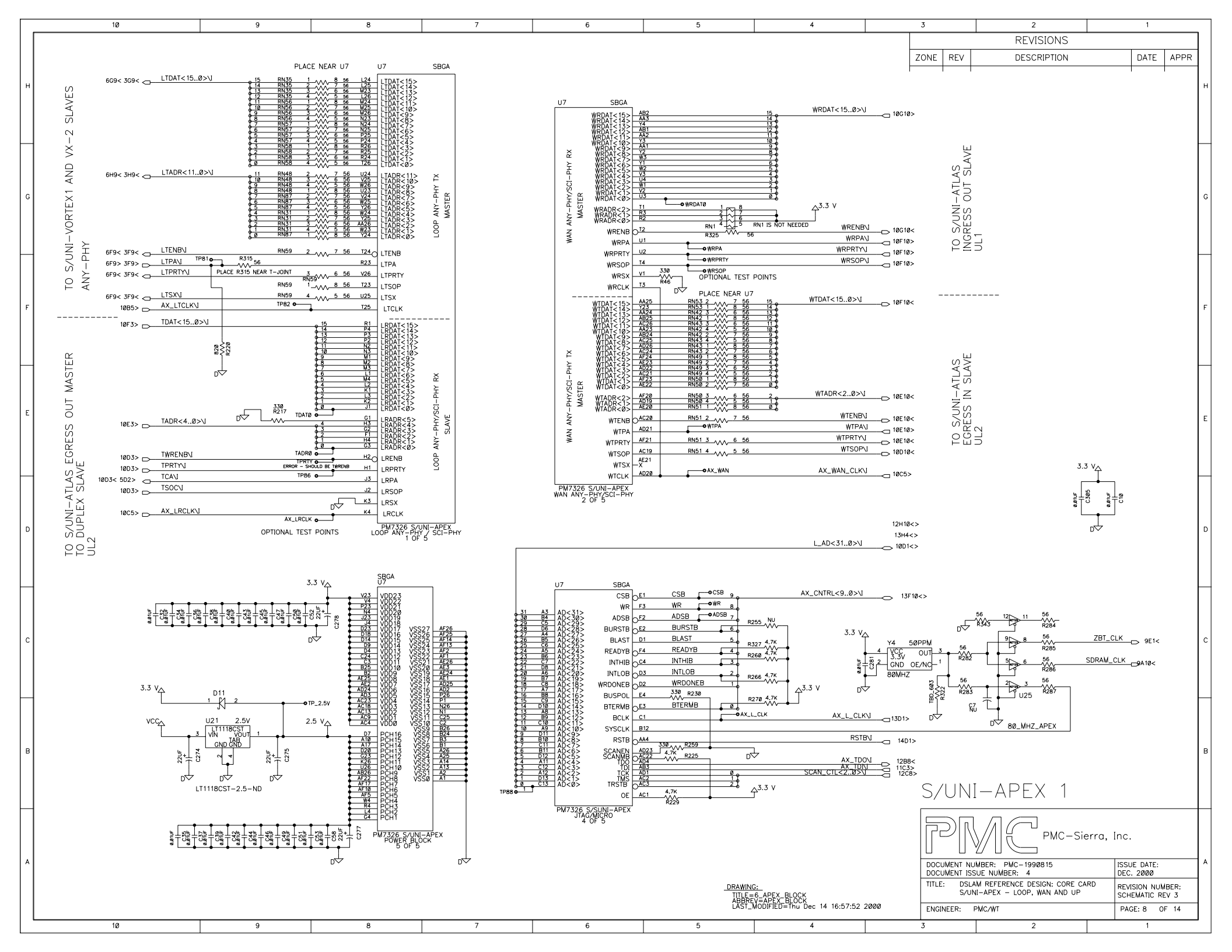


TITLE=5_VORTEX_1_BLOCK
ABBREV=VORTEX1
LAST_MODIFIED=Thu Dec 14 16:58:14 2000

S/UNI-VORTEX-1.2

PMC-Sierra, Inc.

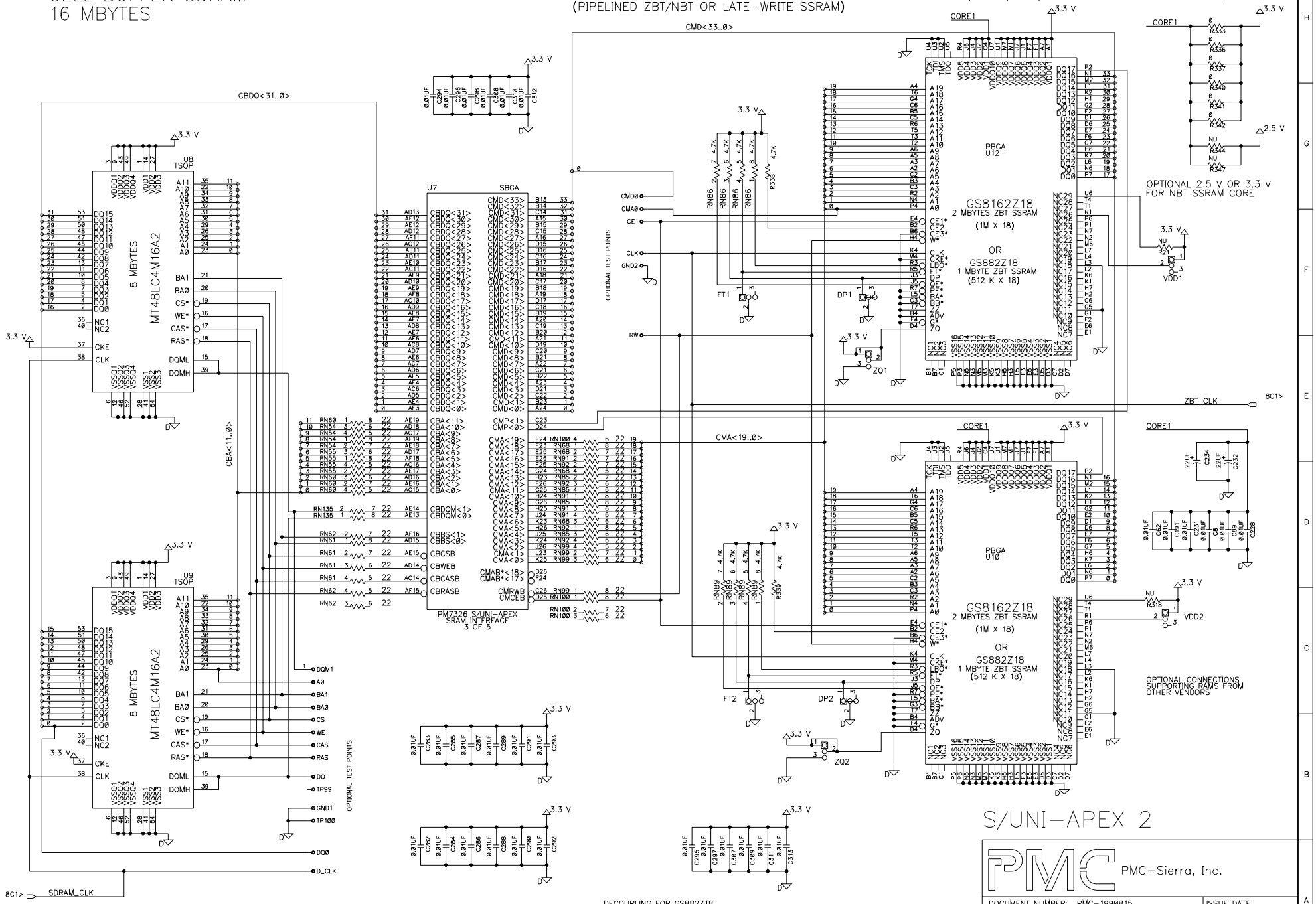
DOCUMENT NUMBER: PMC-1990815 DOCUMENT ISSUE NUMBER: 4	ISSUE DATE: DEC. 2000
TITLE: DSLAM REFERENCE DESIGN: CORE CARD S/UNI-VORTEX1 LVDS INTERFACE	REVISION NUMBER: SCHEMATIC REV 3
ENGINEER: PMC/WT	PAGE: 7 OF 14


REVISIONS
ZONE | REV | DESCRIPTION | DATE | APPR
TO S/UNI-VORTEX1 AND VX-2 SLAVES ANY-PHY
PLACE NEAR U7
U7
SBGA
LOOP ANY-PHY TX MASTER
LOOP ANY-PHY/SCI-PHY RX SLAVE
PM7326 S/UNI-APEX LOOP ANY-PHY / SCI-PHY 1 OF 5
OPTIONAL TEST POINTS
PLACE R315 NEAR T-JOINT
TO S/UNI-ATLAS EGRESS OUT MASTER TO DUPLEX SLAVE UL2
TO S/UNI-ATLAS INGRESS OUT SLAVE UL1
TO S/UNI-ATLAS EGRESS IN SLAVE UL2
WAN ANY-PHY/SCI-PHY TX MASTER
WAN ANY-PHY/SCI-PHY RX MASTER
PM7326 S/UNI-APEX WAN ANY-PHY/SCI-PHY 2 OF 5
RN1 IS NOT NEEDED
PM7326 S/UNI-APEX JTAG/MICRO 4 OF 5
PM7326 S/UNI-APEX POWER BLOCK 5 OF 5
LT1118CST-2.5-ND
80MHZ
80_MHZ_APEX
S/UNI-APEX 1
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-1990815
DOCUMENT ISSUE NUMBER: 4
ISSUE DATE: DEC. 2000
TITLE: DSLAM REFERENCE DESIGN: CORE CARD S/UNI-APEX - LOOP, WAN AND UP
REVISION NUMBER: SCHEMATIC REV 3
ENGINEER: PMC/WT
PAGE: 8 OF 14
DRAWING:
TITLE=6_APEX_BLOCK
ABBREV=APEX_BLOCK
LAST_MODIFIED=Thu Dec 14 16:57:52 2000

CELL BUFFER SDRAM
16 MBYTES

CONTEXT MEMORY ZBT/NBT SSRAM
(PIPELINED ZBT/NBT OR LATE-WRITE SSRAM)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



DRAWING:
TITLE=6_APEX_BLOCK
ABBREV=APEX_BLOCK
LAST_MODIFIED=Thu Dec 14 16:58:01 2000

S/UNI-APEX 2

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1990815 DOCUMENT ISSUE NUMBER: 4	ISSUE DATE: DEC. 2000
TITLE: DSLAM REFERENCE DESIGN: CORE CARD S/UNI-APEX SSRAM INTERFACE	REVISION NUMBER: SCHEMATIC REV 3
ENGINEER: PMC/WT	PAGE: 9 OF 14

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

TO S/UNI-APEX WAN, RX MASTER
UTOPIA L1

TO S/UNI-APEX WAN, TX MASTER
UTOPIA L2

TO S/UNI-VX1, S/UNI-VX2 AND
S/UNI-DUPLEX SLAVES
SCY-PHY/UL2

TO S/UNI-APEX LOOP RX SLAVE
TO S/UNI-DUPLEX SLAVE
UL2

PM7324 S/UNI-ATLAS
SLAVE UTOPIA
2 OF 5

PM7324 S/UNI-ATLAS
MASTER UTOPIA
1 OF 5

PM7324 S/UNI-ATLAS
MICRO INTERFACE
3 OF 5

PLACE NEAR U1

PLACE NEAR T-JOINT

PLACE NEAR U2 OR U3

SHORT TRACES

QS53805 CLOCK BUFFER DUAL 1-TO-5

50MHZ

S/UNI-ATLAS 1

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1990815 DOCUMENT ISSUE NUMBER: 4	ISSUE DATE: DEC. 2000
TITLE: DSLAM REFERENCE DESIGN: CORE CARD S/UNI-ATLAS, INGRESS, EGRESS AND UP	REVISION NUMBER: SCHEMATIC REV 3
ENGINEER: PMC/WT	PAGE: 10 OF 14

DRAWING:
TITLE=7_ATLAS_BLOCK
ABBREV=ATLAS_BLOCK
LAST_MODIFIED=Thu Dec 14 16:57:29 2000

S/UNI-ATLAS RAM INTERFACE

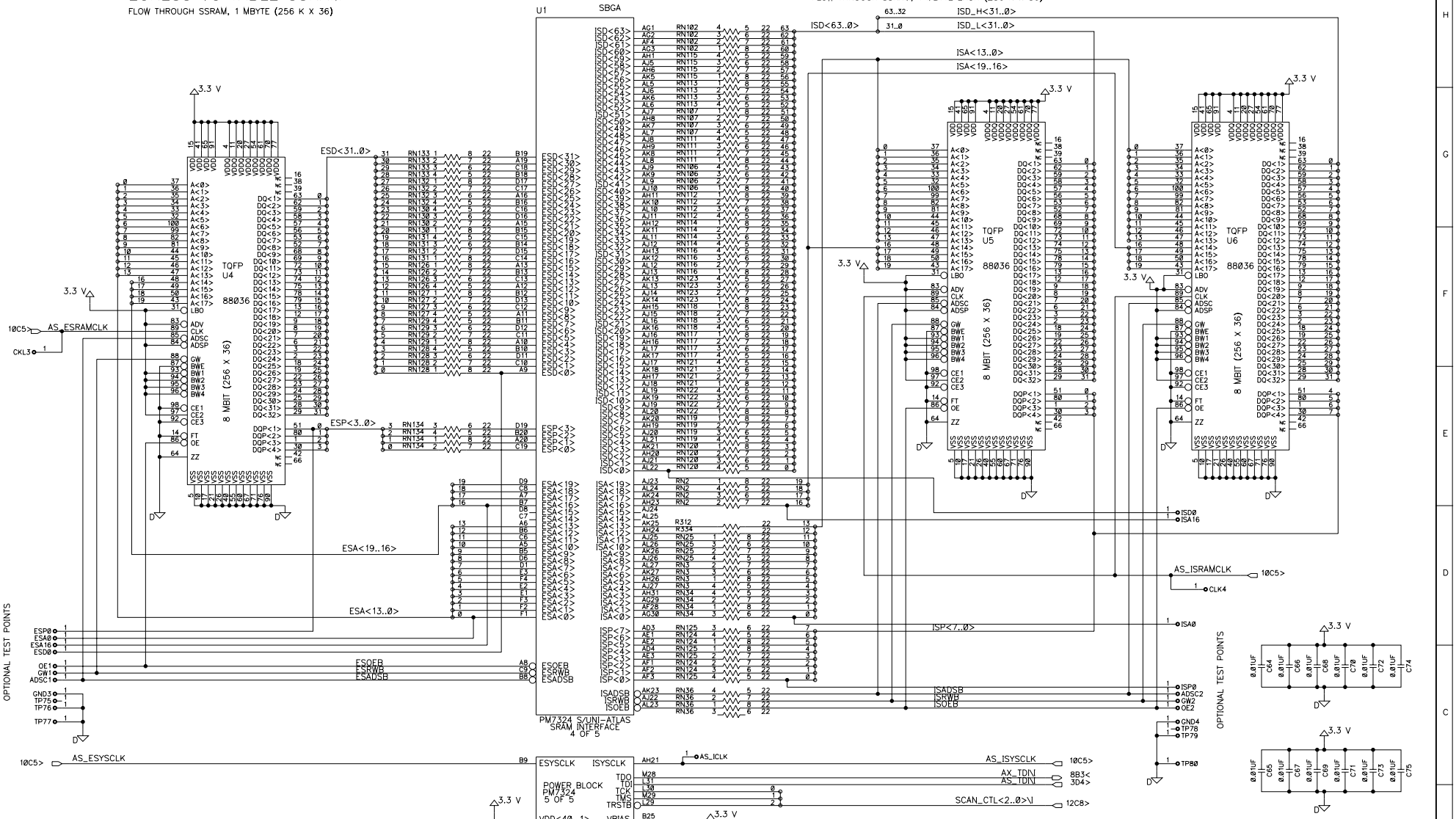
EGRESS VC TABLE SSRAM

FLOW THROUGH SSRAM, 1 MBYTE (256 K X 36)

INGRESS VC TABLE SSRAM

FLOW THROUGH SSRAM, 1 MBYTE EACH (256 K X 36)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

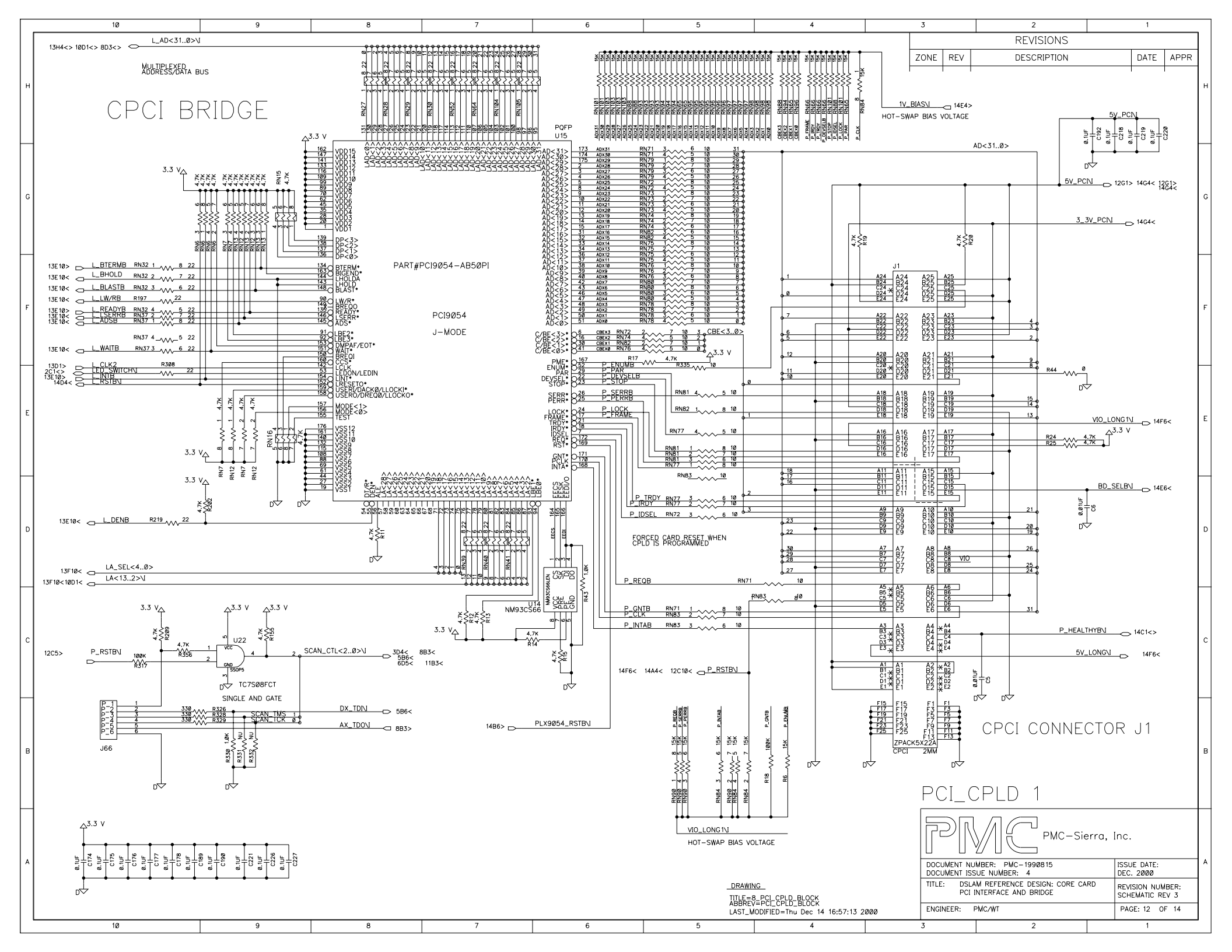


S/UNI-ATLAS 2

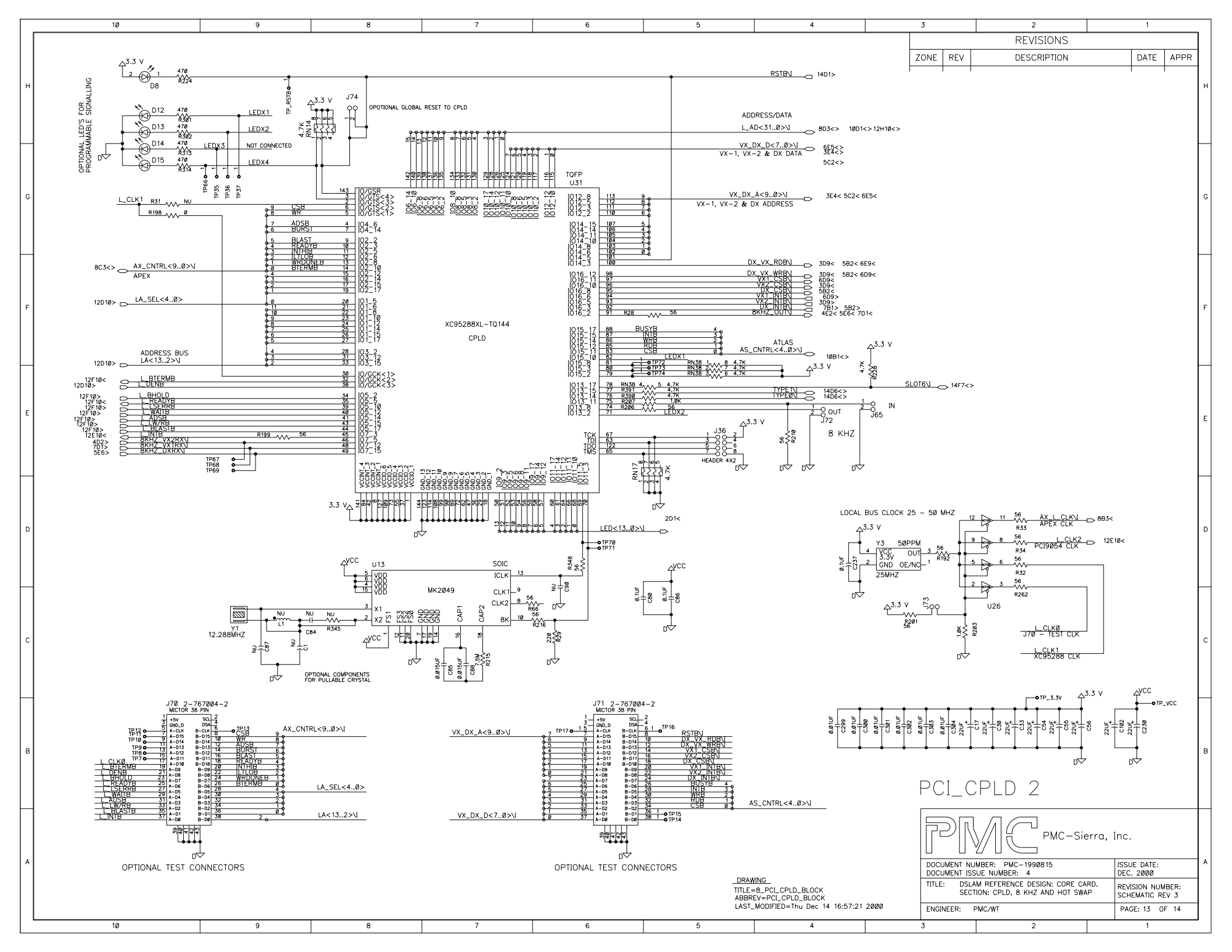
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1990815 DOCUMENT ISSUE NUMBER: 4	ISSUE DATE: DEC. 2000
TITLE: DSLAM REFERENCE DESIGN: CORE CARD S/UNI-ATLAS SSRAM INTERFACE	REVISION NUMBER: SCHEMATIC REV 3
ENGINEER: PMC/WT	PAGE: 11 OF 14

DRAWING:
TITLE=7_ATLAS_BLOCK
ABBREV=ATLAS_BLOCK
LAST_MODIFIED=Thu Dec 14 16:57:42 2000



REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR


REVISIONS
ZONE | REV | DESCRIPTION | DATE | APPR
OPTIONAL LED'S FOR PROGRAMMABLE SIGNALLING
D8
D12
D13
D14
D15
LEDX1
LEDX2
LEDX3
LEDX4
NOT CONNECTED
J74
OPOTIONAL GLOBAL RESET TO CPLD
RSTBN
14D1>
ADDRESS/DATA
L_AD<31..0>\I
8D3<> 10D1<> 12H10<>
VX_DX_D<7..0>\I
VX-1, VX-2 & DX DATA
6E5<>
3E4<>
5C2<>
TQFP
U31
VX_DX_A<9..0>\I
VX-1, VX-2 & DX ADDRESS
3E4< 5C2< 6E5<
L_CLK1
DX_VX_RDBN\I
DX_VX_WRBN\I
VX1_CSBN\I
VX2_CSBN\I
DX_CSBN\I
VX1_INTBN\I
VX2_INTBN\I
DX_INTBN\I
8KHZ_OUT\I
3D9< 5B2< 6E9<
3D9< 5B2< 6D9<
6D9<
3D9<
5B2<
6D9>
3D9>
7B1> 5B2>
4E2< 5E6< 7D1<
8C3<>
AX_CNTRL<9..0>\I
APEX
12D10>
LA_SEL<4..0>
ADDRESS BUS
LA<13..2>\I
XC95288XL-TQ144
CPLD
BUSYB
INTB
WRB
RDB
CSB
ATLAS
AS_CNTRL<4..0>\I
10B1<>
LEDX1
LEDX2
TYPE1\I
TYPE0\I
14D6<>
SLOT6\I
14F7<>
IN
OUT
J72
8 KHZ
J65
J36
HEADER 4X2
TCK
TDI
TDO
TMS
LED<13..0>\I
2D1<
TP67
TP68
TP69
TP70
TP71
U13
SOIC
MK2049
12.288MHZ
OPTIONAL COMPONENTS FOR PULLABLE CRYSTAL
LOCAL BUS CLOCK 25 - 50 MHZ
Y3
50PPM
25MHZ
AX_L_CLK\I
APEX CLK
8B3<
L_CLK2
PCI9054 CLK
12E10<
U26
L_CLK0
J70 - TEST CLK
L_CLK1
XC95288 CLK
J70 2-767004-2
MICTOR 38 PIN
J71 2-767004-2
MICTOR 38 PIN
OPTIONAL TEST CONNECTORS
OPTIONAL TEST CONNECTORS
TP_3.3V
TP_VCC
PCI_CPLD 2
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-1990815
DOCUMENT ISSUE NUMBER: 4
ISSUE DATE: DEC. 2000
TITLE: DSLAM REFERENCE DESIGN: CORE CARD. SECTION: CPLD, 8 KHZ AND HOT SWAP
REVISION NUMBER: SCHEMATIC REV 3
ENGINEER: PMC/WT
PAGE: 13 OF 14
DRAWING
TITLE=8_PCI_CPLD_BLOCK
ABBREV=PCI_CPLD_BLOCK
LAST_MODIFIED=Thu Dec 14 16:57:21 2000

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

VORTEX-1

DUPLEX

J5

ZPACK5X22B
CPCI 2MM

OPTIONAL TEST GND

OPTIONAL TRACES

OPTIONAL CONNECTORS

10 V ZENER DIODES TO PROTECT GATES

TO PREVENT CURRENT SENSING TRIGGER
R200 SHOULD BE 0.005 OHM

NEVER SHORT +5 V AND VI/O

Q4 FOR OPTIONAL POWER
CYCLING ON RESET

HOT SWAP CONTROLLER FOR +5 V AND +3.3 V

SOIC8_TLV2461
OP-AMP

RESET CONTROLLER

NON HOT SWAP SHELVES
HAVE THIS PIN AS GROUND

OPTIONAL CIRCUIT
GENERATING HEALTHY# FOR
HOT SWAP COMPATIBILITY

TC7S08FCT
SINGLE AND GATE

R351 CAN BE LOWER VALUE

J5 CONNECTOR

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1990815 DOCUMENT ISSUE NUMBER: 4	ISSUE DATE: DEC. 2000
TITLE: DSLAM REFERENCE DESIGN: CORE CARD J5 WITH LVDS TO BACKPLANE	REVISION NUMBER: SCHEMATIC REV 3
ENGINEER: PMC/WT	PAGE: 14 OF 14

DRAWING

TITLE=9_J5_CONNECTOR
ABBREV=J5
LAST_MODIFIED=Thu Dec 14 16:57:01 2000

21. APPENDIX H: LAYOUT

The layout section contains:

- drawing summary report
- x-y coordinates pages
- mechanical drawing page
- top component placement page
- top silk screen page
- copper layers, ten pages
- bottom silk screen page
- bottom component placement page

21.1. Drawing Summary Report

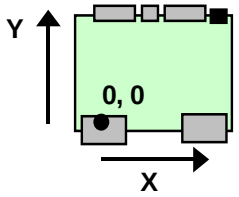
```
|-------------------------------------------------------------------------|
|                          DRAWING SUMMARY REPORT                         |
|                                                                Page   1  |
|-------------------------------------------------------------------------|
|  W:\pcb8\pcb\dslam_core.brd                                             |
|                                                 Wed May 03 11:08:26 2000  |
|-------------------------------------------------------------------------|
     Drawing Extents XL -4900.000  YL -6600.000  XU 17100.000  YU 10400.000
                Dimensions in mils with 3 decimal places
    - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
     Package Symbols:   1115 Total    424 Mirrored   6083  Pins
    - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
     Mechanical Symbols:  12 Total                     8  Pins
    - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
     Format Symbols:       1
    - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
     DRC:                  0 Errors
    - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
     Padstacks:           62 Definitions
    - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
     Functions:  Assigned 1558  Unassigned 0  Total 1558
    - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

```
    Layout Statistics:
    ------------------
        Components:  Placed 1115  Unplaced 0  Total 1115
        Nets:  W/Rats 1546  No/Rats 1  Total 1547
        Pins:  W/Rats 5508  No/Rats 148  Unused 423  Unplaced 0  Total 6079
        Equivalent ICs (1 pin = 1/14 EIC)  434
        RatTs             0
Connection Statistics:        W/Rats      No/Rats      Total
    ---------------------        ------      -------      -----
        Connections               3962         147         4109
        Already Connected         3962         147         4109
        Missing Connections          0           0            0
        Dangling Connections (See logfile)                    0
        Connection Completion      100.00%     100.00%      100.00%
        Manh Distance (inches)    3290.61
        Etch Length (inches)      3281.20       23.88      3305.10
        Number of vias          4263           0         4263
        Vias per Connection          1.07        0.00         1.03
        Smd pins with attached clines                      4909
    - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
     Etch:                  #connect   #shapes  #rect-  #non-connect
                           lines/arcs  (voids)  angles   lines/arcs   #text
       TOP                    3869      8(0)        0         1          3
       SIG1                    402     1(88)        0         1          3
       GND_PLANE               289   3(3644)        0         1          3
       3V3_PLANE                32   1(3941)        0         1          3
       SIG2                    473      0(0)        0         1          3
       SIG3                    395      0(0)        0         1          3
       3V3_A_PLANE              32   4(3907)        0         1          3
       GND1_PLANE              288   3(3644)        0         1          3
       SIG4                    308     1(80)        0         1          3
       BOTTOM                 1640      0(0)        0         1          3
|-------------------------------------------------------------------------|
|                          DRAWING SUMMARY REPORT                Page   2  |
|-------------------------------------------------------------------------|
|  W:\pcb8\pcb\dslam_core.brd                      Wed May 03 11:08:26 2000  |
|-------------------------------------------------------------------------|
   etch totals           7728 21(15304)        0        10         30
|------------------------    End  Summary  Report   -------------------------|
```

21.2. X-Y Coordinates for Issue 3 Board

Following pages show X-Y coordinates for components placed on Issue 3 board.

X-Y Coordinates for components on Core Card Issue 3



UUNITS = MILS (e.g. 4160 = 4.160 inch)

Component	X	Y	Footprint
A0	-880	3960	TST_PT_PAD50CIR32D
ADSC1	4160	1200	TST_PT_PAD50CIR32D
ADSC2	6920	1800	TST_PT_PAD50CIR32D
AS_ICLK	3365	2705	TST_PT_PAD50CIR32D
AX_WAN	280	2825	TST_PT_PAD50CIR32D
BA0	-800	3960	TST_PT_PAD50CIR32D
BA1	-800	3880	TST_PT_PAD50CIR32D
C1	3415	630	603
C10	4945	380	402
C100	3300	4300	402
C101	2950	4450	402
C102	2410	680	SMDTANCAP_B
C103	3800	3575	402
C104	3225	4475	402
C105	3125	4100	402
C106	3975	4475	402
C107	3825	3950	402
C108	6995	3920	402
C109	6320	4480	402
C11	4375	975	402
C110	5595	4020	402
C111	6570	4495	402
C112	6845	4295	402
C113	5995	3920	402
C114	2275	5612.5	SMDCAP805
C115	2350	5612.5	SMDCAP805
C116	2437.5	5612.5	SMDCAP805
C117	2512.5	5612.5	SMDCAP805
C118	1900	5612.5	SMDCAP805
C119	1975	5612.5	SMDCAP805
C12	3500	1365	402
C120	2062.5	5612.5	SMDCAP805
C121	2137.5	5612.5	SMDCAP805
C122	1525	5612.5	SMDCAP805
C123	1600	5612.5	SMDCAP805
C124	1687.5	5612.5	SMDCAP805
C125	1762.5	5612.5	SMDCAP805
C126	1150	5612.5	SMDCAP805
C127	1225	5612.5	SMDCAP805
C128	1312.5	5612.5	SMDCAP805
C129	1387.5	5612.5	SMDCAP805
C13	4325	2425	402
C130	675	5612.5	SMDCAP805
C131	750	5612.5	SMDCAP805
C132	837.5	5612.5	SMDCAP805
C133	912.5	5612.5	SMDCAP805
C134	300	5612.5	SMDCAP805
C135	375	5612.5	SMDCAP805
C136	462.5	5612.5	SMDCAP805
C137	537.5	5612.5	SMDCAP805
C138	-75	5612.5	SMDCAP805
C139	0	5612.5	SMDCAP805
C14	3150	1725	402
C140	87.5	5612.5	SMDCAP805
C141	162.5	5612.5	SMDCAP805
C142	-450	5612.5	SMDCAP805
C143	-375	5612.5	SMDCAP805
C144	-287.5	5612.5	SMDCAP805
C145	-212.5	5612.5	SMDCAP805
C146	4052.5	4790	603
C147	3902.5	4790	603
C148	3752.5	4790	603
C149	3502.5	4790	603
C15	4650	2225	402
C150	3350	4795	603
C151	3102.5	4790	603
C152	2952.5	4790	603
C153	2802.5	4790	603
C154	6720	3645	402
C155	6670	3395	402
C156	3227.5	4727.5	SMDTANCAP_B
C157	7045	3940	SMDTANCAP_B
C158	5982.5	4095	402
C159	6345	3420	402
C16	3755	1365	402
C160	6282.5	4532.5	SMDTANCAP_B
C161	5580	3990	SMDTANCAP_B
C162	5995	3620	402
C163	6020	3395	402
C164	6870	3220	402
C165	6195	4115	402
C166	5770	3245	402
C167	6690	3770	402
C168	6095	4295	402
C169	6685	4070	402
C17	2510	4720	SMDTANCAP_B
C170	5820	4270	402
C171	6495	4120	402
C172	4345	3650	402
C173	4775	3410	402
C174	-12.5	785	603
C175	-627.5	1165	603
C176	112.5	1795	603
C177	132.5	810	603
C178	-72.5	1815	603
C179	6525	5612.5	SMDCAP805
C18	5645	1775	402
C180	6600	5612.5	SMDCAP805
C181	6687.5	5612.5	SMDCAP805
C182	6762.5	5612.5	SMDCAP805
C183	6150	5612.5	SMDCAP805
C184	6225	5612.5	SMDCAP805
C185	6312.5	5612.5	SMDCAP805
C186	6387.5	5612.5	SMDCAP805
C187	5775	5612.5	SMDCAP805
C188	5850	5612.5	SMDCAP805
C189	402.5	1200	603
C19	4100	1725	402
C190	-172.5	785	603

C191	1825	4300	402	C25	4800	1130	402
C192	-925	410	603	C250	3012.5	5612.5	SMDCAP805
C193	5937.5	5612.5	SMDCAP805	C251	3087.5	5612.5	SMDCAP805
C194	6012.5	5612.5	SMDCAP805	C252	7275	1825	SMDTANCAP_B
C195	5400	5612.5	SMDCAP805	C253	5510	3700	SMDTANCAP_B
C196	5475	5612.5	SMDCAP805	C254	3595	2860	402
C197	5562.5	5612.5	SMDCAP805	C255	3855	2860	402
C198	5637.5	5612.5	SMDCAP805	C256	6532.5	4532.5	SMDTANCAP_B
C199	4925	5612.5	SMDCAP805	C257	5221.5	4530	SMDTANCAP_B
C2	2940	2355	603	C258	5165	4550	402
C20	5200	1130	402	C259	5170	4190	402
C200	5000	5612.5	SMDCAP805	C26	5400	2225	402
C201	5087.5	5612.5	SMDCAP805	C260	4725	4650	603
C202	5162.5	5612.5	SMDCAP805	C261	4931.5	4650	603
C203	4550	5612.5	SMDCAP805	C262	5165	4430	402
C204	4625	5612.5	SMDCAP805	C263	5165	4320	402
C205	4712.5	5612.5	SMDCAP805	C264	5220	4150	SMDTANCAP_B
C206	4787.5	5612.5	SMDCAP805	C265	5221.5	4405	SMDTANCAP_B
C207	4175	5612.5	SMDCAP805	C266	4990	4450	402
C208	4250	5612.5	SMDCAP805	C267	4695	4320	402
C209	4337.5	5612.5	SMDCAP805	C268	4556.5	4100	402
C21	3750	2085	402	C269	4757	4027	402
C210	4412.5	5612.5	SMDCAP805	C27	5825	2425	402
C211	3800	5612.5	SMDCAP805	C270	4919	3960	402
C212	3875	5612.5	SMDCAP805	C271	5087.5	4164	402
C213	3962.5	5612.5	SMDCAP805	C272	4911.5	4280	402
C214	4037.5	5612.5	SMDCAP805	C273	5221.5	4280	SMDTANCAP_B
C215	7070	4205	603	C274	800	2900	SMDTANCAP_B
C216	7070	4550	603	C275	1350	2900	SMDTANCAP_B
C217	6810	4645	603	C276	5036.5	4040	402
C218	-825	410	603	C277	1100	3125	SMDTANCAP_B
C219	1125	300	603	C278	1325	3125	SMDTANCAP_B
C22	5725	1075	402	C279	3595	2460	402
C220	1125	200	603	C28	5645	2125	402
C221	-212.5	1815	603	C280	3855	2460	402
C222	6660	4645	603	C281	-175	5045	402
C223	6370	4585	603	C282	-270	3235	402
C224	6150	4645	603	C283	-435	4045	402
C225	6010	4645	603	C284	-450	3235	402
C226	402.5	1360	603	C285	-590	4090	402
C227	-627.5	1575	603	C286	-180	3785	402
C228	1825	3525	402	C287	-900	4595	402
C229	5860	4645	603	C288	-630	3230	402
C23	3495	2085	402	C289	-165	4045	402
C230	2750	800	SMDTANCAP_B	C29	5725	2325	402
C231	2125	4300	402	C290	-920	3780	402
C232	1970	3140	SMDTANCAP_B	C291	-165	4590	402
C233	1200	0	603	C292	-450	3785	402
C234	1965	3920	SMDTANCAP_B	C293	-435	4590	402
C235	1100	25	SMDTANCAP_B	C294	1750	3675	402
C236	3605	260	603	C295	2555	4150	402
C237	1510	2830	603	C296	2200	3600	402
C238	1215	455	SMDTANCAP_B	C297	2205	4370	402
C239	382.5	2645	NEC_D	C298	2300	3400	402
C24	4475	1075	402	C299	1830	2040	402
C240	1125	425	603	C3	4230	2175	603
C241	3705	255	603	C30	6045	675	SMDTANCAP_B
C242	2090	5	SMDTANCAP_B	C300	1485	2045	402
C243	7205	3260	SMDTANCAP_B	C301	1430	1090	402
C244	3225	5612.5	SMDCAP805	C302	2300	1437.5	402
C245	3300	5612.5	SMDCAP805	C303	1820	1060	402
C246	3387.5	5612.5	SMDCAP805	C304	1295	1770	402
C247	3462.5	5612.5	SMDCAP805	C305	595	5190	402
C248	2850	5612.5	SMDCAP805	C307	2295	4190	402
C249	2925	5612.5	SMDCAP805	C308	2555	3375	402

C309	1750	4100	402	C86	3075	1000	603
C31	5550	1130	402	C87	3505	875	603
C310	1745	3320	402	C88	2850	885	SMDCAP1206
C311	2545	4455	402	C89	2425	3525	402
C312	2550	3685	402	C9	600	500	SMDTANCAP_B
C313	1750	4450	402	C90	2935	1160	SMDCAP805
C32	375	3925	402	C91	4195	4125	SMDTANCAP_B
C33	-200	2600	SMDTANCAP_B	C92	4000	3400	402
C34	775	3480	402	C93	3600	4320	402
C35	975	3220	402	C94	3627.5	4727.5	SMDTANCAP_B
C36	1025	4325	402	C95	2700	4150	SMDTANCAP_B
C37	120	3475	402	C96	3475	3600	402
C38	1375	4500	402	C97	3150	3575	402
C39	1220	4230	402	C98	3125	3800	402
C4	1915	5	SMDTANCAP_B	C99	3100	4275	402
C40	375	3675	402	CAS	-640	3880	TST_PT_PAD50CIR32D
C41	5000	2225	402	CE1	2440	3920	TST_PT_PAD50CIR32D
C42	525	4325	402	CKL3	4165	1660	TST_PT_PAD50CIR32D
C43	575	4325	402	CLK	2200	3920	TST_PT_PAD50CIR32D
C44	925	4325	402	CLK4	7000	1800	TST_PT_PAD50CIR32D
C45	225	4500	402	CMA0	2360	3920	TST_PT_PAD50CIR32D
C46	1460	4100	402	CMD0	2120	3920	TST_PT_PAD50CIR32D
C47	1220	4125	402	CS	-720	3880	TST_PT_PAD50CIR32D
C48	4550	1575	402	D1	2205	750	SOD323
C49	625	3220	402	D11	-25	3050	SMC_2
C5	-860	450	402	D12	2225	2350	LED_11
C50	1350	3325	402	D13	2095	2350	LED_11
C51	1125	3480	402	D14	1965	2350	LED_11
C52	225	3350	402	D15	1835	2350	LED_11
C53	1455	3695	402	D2	1490	-25	SOD323
C54	4130	2765	SMDTANCAP_B	D3	2530	310	SMC_2
C55	-350	4900	SMDTANCAP_B	D4	7575	6017.5	SSF-LXH5147
C56	2725	2675	SMDTANCAP_B	D5	7175	6017.5	SSF-LXH5147
C57	4550	1975	402	D6	6975	6017.5	SSF-LXH5147
C58	120	4075	402	D7	7375	6017.5	SSF-LXH5147
C59	4425	2325	402	D8	2355	2350	LED_11
C6	2825	190	402	D9	-625	5840	LED_5MM
C60	4550	1225	402	DP1	2270	4485	JUMPER_3PIN_INLINE
C61	5645	1575	402	DP2	2020	3275	JUMPER_3PIN_INLINE
C62	2425	4300	402	DQ	-560	3960	TST_PT_PAD50CIR32D
C63	5825	975	402	DQ0	25	4450	TST_PT_PAD50CIR32D
C64	6570	2610	402	DX_VX_RDB	5425	3675	TST_PT_PAD50CIR32D
C65	6225	1375	402	DX_VX_WRB	5600	3430	TST_PT_PAD50CIR32D
C66	6825	2610	402	ESA0	4070	1120	TST_PT_PAD50CIR32D
C67	6830	1015	402	ESA16	4070	1200	TST_PT_PAD50CIR32D
C68	6570	1890	402	ESD0	4070	1280	TST_PT_PAD50CIR32D
C69	6415	1735	402	ESP0	4070	1370	TST_PT_PAD50CIR32D
C7	260	5190	SMDCAP805	FT1	2145	4485	JUMPER_3PIN_INLINE
C70	7180	2250	402	FT2	2735	3575	JUMPER_3PIN_INLINE
C71	7175	1375	402	GND1	-560	3880	TST_PT_PAD50CIR32D
C72	6830	1890	402	GND2	2520	3920	TST_PT_PAD50CIR32D
C73	6570	1015	402	GND3	3075	1925	TST_PT_PAD50CIR32D
C74	6225	2250	402	GND4	6680	1800	TST_PT_PAD50CIR32D
C75	6980	1735	402	GW1	4160	1370	TST_PT_PAD50CIR32D
C76	4150	4100	402	GW2	6760	1800	TST_PT_PAD50CIR32D
C77	3265	4690	402	ISA0	6520	1800	TST_PT_PAD50CIR32D
C78	2750	4175	402	ISA16	6440	1800	TST_PT_PAD50CIR32D
C79	3665	4690	402	ISD0	6600	1800	TST_PT_PAD50CIR32D
C8	2150	3550	402	J1	0	88.583	ZPACK5X22FH_ASCPCI
C80	3450	950	603	J10	7370.496	4284.5	HEADER3_2MM
C81	2900	3400	402	J11	7370.496	4205.5	HEADER3_2MM
C82	3850	3825	402	J12	7370.496	4482	HEADER3_2MM
C83	3850	4275	402	J13	7370.496	4403	HEADER3_2MM
C84	3565	730	SMDCAP805	J14	7420.5	4920.496	HEADER3_2MM
C85	2950	885	SMDCAP1206	J15	7499.5	4920.496	HEADER3_2MM

J16	7223	4920.496	HEADER3_2MM	JP12	7115	1800	JUMPER_3PIN_INLINE
J17	7302	4920.496	HEADER3_2MM	JP13	5590	725	JUMPER_3PIN_INLINE
J18	7025.5	4920.496	HEADER3_2MM	JP16	580	1190	JUMPER_3PIN_INLINE
J19	7104.5	4920.496	HEADER3_2MM	JP17	4395	4630	JUMPER_3PIN_INLINE
J20	6828	4920.496	HEADER3_2MM	JP18	5	2625	JUMPER_3PIN_INLINE
J21	6907	4920.496	HEADER3_2MM	JP2	1780	3920	JUMPER_3PIN_INLINE
J22	6630.5	4920.496	HEADER3_2MM	JP3	2220	2085	JUMPER_3PIN_INLINE
J23	6709.5	4920.496	HEADER3_2MM	JP4	1785	3140	JUMPER_3PIN_INLINE
J24	6433	4920.496	HEADER3_2MM	JP8	6450	915	JUMPER_3PIN_INLINE
J25	6512	4920.496	HEADER3_2MM	JP9	1325	1145	JUMPER_3PIN_INLINE
J26	6235.5	4920.496	HEADER3_2MM	L1	3485	600	SMDCAP1206
J27	6314.5	4920.496	HEADER3_2MM	LA2	4195	1845	TST_PT_PAD50CIR32D
J28	6038	4920.496	HEADER3_2MM	LTADR0	5900	2950	TST_PT_PAD50CIR32D
J29	6117	4920.496	HEADER3_2MM	LTENB	6060	2950	TST_PT_PAD50CIR32D
J30	5840.5	4920.496	HEADER3_2MM	M1	7868.11	6020.860	MOUNT_HOLE_150
J31	5919.5	4920.496	HEADER3_2MM	OE1	4160	1280	TST_PT_PAD50CIR32D
J32	5643	4920.496	HEADER3_2MM	OE2	6840	1800	TST_PT_PAD50CIR32D
J33	5722	4920.496	HEADER3_2MM	P1	-917.322	3006.889	CPCI_ESD_STRIP
J34	5445.5	4920.496	HEADER3_2MM	Q1	3100	125	SOT23
J35	5524.5	4920.496	HEADER3_2MM	Q2	1715	292.5	D2PAK
J36	995	895	HEADER_4X2	Q3	2235	520	SO8NB-3
J37	5248	4920.496	HEADER3_2MM	Q4	3100	325	SOT23
J38	5327	4920.496	HEADER3_2MM	Q5	-50	1315	SOT23
J39	4487	4950.496	HEADER3_2MM	Q6	-195	1350	SOT23
J40	4566	4950.496	HEADER3_2MM	Q7	135	1300	SOT23
J41	4289.5	4950.496	HEADER3_2MM	R1	3100	225	603
J42	4368.5	4950.496	HEADER3_2MM	R10	5580	3495	603
J43	4882	4950.496	HEADER3_2MM	R100	3140	4690	603
J44	4961	4950.496	HEADER3_2MM	R101	3140	4690	603
J45	4250	4450	HEADER_2	R102	2990	4690	603
J46	6265	5944	MOLEX53460_0611	R103	2990	4690	603
J47	5515	5944	MOLEX53460_0611	R104	2765	4690	603
J48	4665	5944	MOLEX53460_0611	R105	2840	4690	603
J49	3915	5944	MOLEX53460_0611	R106	4090	4690	603
J5	7100.394	88.583	ZPACK5X22FH_BSCPCI	R107	4015	4690	603
J50	2015	5944	MOLEX53460_0611	R108	3865	4690	603
J51	1265	5944	MOLEX53460_0611	R109	3865	4690	603
J52	415	5944	MOLEX53460_0611	R11	545	1115	603
J53	-335	5944	MOLEX53460_0611	R110	3715	4690	603
J54	6640	5944	MOLEX53460_0611	R111	3715	4690	603
J55	5890	5944	MOLEX53460_0611	R112	3540	4690	603
J56	5040	5944	MOLEX53460_0611	R113	3465	4690	603
J57	4290	5944	MOLEX53460_0611	R114	3315	4690	603
J58	2390	5944	MOLEX53460_0611	R115	3315	4690	603
J59	1640	5944	MOLEX53460_0611	R116	3065	4690	603
J6	7370.496	3889.5	HEADER3_2MM	R117	3065	4690	603
J60	790	5944	MOLEX53460_0611	R118	2915	4690	603
J61	40	5944	MOLEX53460_0611	R119	2915	4690	603
J62	2965	5944	MOLEX53460_0611	R12	397.5	2025	603
J63	3340	5944	MOLEX53460_0611	R120	2840	4690	603
J64	-825	587.5	JUMPER3	R121	2765	4690	603
J65	2775	1350	HEADER_2	R122	6257.5	4057.5	603
J66	5300	475	SIP6	R123	6645	3632.5	603
J67	4684.5	4950.496	HEADER3_2MM	R124	5595	3970	603
J68	4763.5	4950.496	HEADER3_2MM	R125	6995	3970	603
J7	7370.496	3810.5	HEADER3_2MM	R126	6530	4500	603
J70	925	1850	MICTOR_38_PIN	R127	6270	4520	SMDRES805
J71	2650	1950	MICTOR_38_PIN	R128	5937.5	5637.5	603
J72	2775	1125	HEADER_2	R129	5400	5637.5	603
J73	2080	3030	HEADER_2	R13	342.5	2025	603
J74	2210	2525	HEADER_2	R130	5562.5	5637.5	603
J8	7370.496	4087	HEADER3_2MM	R131	4925	5637.5	603
J9	7370.496	4008	HEADER3_2MM	R132	5087.5	5637.5	603
JP1	-785	3125	JUMPER_3PIN_INLINE	R133	4550	5637.5	603
JP11	6715	2700	JUMPER_3PIN_INLINE	R134	4712.5	5637.5	603

R135	4175	5637.5	603	R194	3300	5637.5	603
R136	4337.5	5637.5	603	R195	6475	425	603
R137	3800	5637.5	603	R196	6400	425	603
R138	3962.5	5637.5	603	R197	452.5	2025	603
R139	6600	5637.5	603	R198	1237.5	1392.5	603
R14	-575	2625	603	R199	1237.5	1267.5	603
R140	6762.5	5637.5	603	R2	5350	2150	603
R141	6225	5637.5	603	R20	1100	175	603
R142	6387.5	5637.5	603	R200	1385	430	POWERRES_2714
R143	5850	5637.5	603	R201	2250	3025	603
R144	6012.5	5637.5	603	R202	680	1105	603
R145	5475	5637.5	603	R203	2375	2700	603
R146	5637.5	5637.5	603	R204	4125	3825	603
R147	5000	5637.5	603	R205	6550	425	603
R148	5162.5	5637.5	603	R206	2575	1050	603
R149	4625	5637.5	603	R207	2575	1125	603
R15	-675	2625	603	R208	6020	3720	603
R150	4787.5	5637.5	603	R209	4925	475	603
R151	4250	5637.5	603	R21	2725	4395	603
R152	4412.5	5637.5	603	R210	2575	1350	603
R153	3875	5637.5	603	R211	5275	2150	603
R154	4037.5	5637.5	603	R212	3462.5	5637.5	603
R155	4825	350	603	R213	2925	5637.5	603
R156	3605	135	603	R214	3087.5	5637.5	603
R157	3225	5637.5	603	R215	2905	835	SMDRES805
R158	3387.5	5637.5	603	R216	3300	1275	603
R159	2850	5637.5	603	R217	1100	4725	603
R16	7050	3675	603	R218	2760	300	603
R160	7069	4063.5	603	R219	745	1105	603
R161	7019	4063.5	603	R22	6525	5637.5	603
R162	7069	4401	603	R220	830	3600	603
R163	7019	4401	603	R221	2752.5	72.5	603
R164	6770	4575	603	R222	2925	225	603
R165	6845	4515	603	R223	2925	150	603
R166	6620	4590	603	R224	2355	2525	603
R167	6695	4520	603	R225	500	3550	603
R168	6405	4660	603	R226	3215	405	603
R169	6450	4525	603	R227	4710	3750	603
R17	-612.5	1050	603	R228	5875	260	603
R170	6195	4565	603	R229	325	4675	603
R171	6195	4495	603	R23	4740	3660	603
R172	6045	4555	603	R230	1075	4675	603
R173	6045	4495	603	R231	5180	4510	603
R174	5895	4555	603	R232	3940	615	603
R175	5895	4495	603	R233	-750	5625	603
R176	7069	4138.5	603	R234	5200	4265	SMDRES805
R177	7019	4138.5	603	R235	4795	4650	603
R178	7069	4476	603	R236	4860	4650	603
R179	7019	4476	603	R237	4656.5	4650	603
R18	-925	900	603	R238	4860	4650	603
R180	6845	4575	603	R239	4581.5	4650	603
R181	6770	4515	603	R24	915	410	603
R182	6695	4590	603	R240	4795	4650	603
R183	6620	4520	603	R241	4910	2635	603
R184	6450	4585	603	R242	4340	4010	603
R185	6370	4525	603	R243	-650	5625	603
R186	6115	4565	603	R244	5180	4380	603
R187	6115	4495	603	R245	-550	5625	603
R188	5970	4555	603	R246	7750	5750	603
R189	5970	4495	603	R247	1400	925	603
R19	1100	250	603	R248	1462.5	925	603
R190	5820	4555	603	R249	1525	925	603
R191	5820	4495	603	R25	765	410	603
R192	1925	2875	603	R250	1587.5	925	603
R193	3012.5	5637.5	603	R251	1650	925	603

R252	3780	255	603	R310	5000	1275	603
R253	3340	495	603	R311	4850	1275	603
R254	4855	2635	603	R312	6085	2225	603
R255	1225	4675	603	R313	1965	2185	603
R256	2925	-50	603	R314	1835	2185	603
R257	3100	25	603	R315	725	3600	603
R258	2925	365	603	R316	5600	2825	603
R259	500	3500	603	R317	4725	475	603
R26	4175	2100	603	R318	2410	3740	603
R260	1375	4675	603	R319	-925	2300	SMDRES1206
R261	2925	75	603	R32	1925	2675	603
R262	1925	2800	603	R320	-900	5125	SMDRES1206
R263	1712.5	925	603	R321	-800	5125	SMDRES1206
R264	1900	925	603	R322	180	5095	603
R265	1837.5	925	603	R323	5225	2600	603
R266	1300	4675	603	R324	4375	4150	603
R267	1775	925	603	R325	650	4105	603
R268	1962.5	925	603	R326	5150	590	603
R269	2025	925	603	R327	1110	4325	603
R27	4150	4150	603	R328	5250	590	603
R270	1150	4675	603	R329	5390	590	603
R271	2087.5	925	603	R33	2375	2775	603
R272	2150	925	603	R330	5100	590	603
R273	2212.5	925	603	R331	5300	590	603
R274	5180	4140	603	R332	5440	590	603
R275	5056.5	4650	603	R333	1900	4565	603
R276	4375	4275	603	R334	6085	2290	603
R277	4375	4212.5	603	R335	985	410	603
R278	4375	4075	603	R336	2425	4565	603
R279	4925	3825	603	R337	2625	4070	603
R28	2410	1470	603	R338	1600	4450	603
R280	4375	4335	603	R339	1840	3250	603
R281	3605	5	603	R34	2375	2625	603
R282	275	4950	603	R340	1895	3120	603
R283	275	5100	603	R341	2455	3235	603
R284	750	5000	603	R342	2625	3900	603
R285	750	4850	603	R343	755	5065	603
R286	275	4875	603	R344	1710	4530	603
R287	275	5025	603	R345	3565	800	603
R288	4850	1425	603	R346	-105	1145	603
R289	3735	3675	603	R347	1775	3075	603
R29	3175	1275	603	R348	2915	1045	603
R290	4785	4320	603	R349	-295	1190	603
R291	5000	3825	603	R35	4740	3560	603
R292	5006.5	4650	603	R350	-230	1190	603
R293	4875	3825	603	R351	865	1125	603
R294	4375	4275	603	R352	-45	1145	603
R295	4375	4400	603	R353	100	1145	603
R296	912.5	5637.5	603	R354	245	1330	603
R297	375	5637.5	603	R355	35	1145	603
R298	3150	3900	603	R356	4895	600	603
R299	537.5	5637.5	603	R36	6687.5	5637.5	603
R3	5325	2600	603	R37	6150	5637.5	603
R30	2175	205	POWERRES_2714	R38	5190	3435	603
R300	4375	4475	603	R39	4770	3750	603
R301	2225	2185	603	R390	2575	1200	603
R302	2095	2185	603	R391	2575	1275	603
R303	0	5637.5	603	R4	5125	2150	603
R304	162.5	5637.5	603	R40	5190	3660	603
R305	-375	5637.5	603	R41	5190	3510	603
R306	-212.5	5637.5	603	R42	3615	4690	603
R307	5200	2150	603	R43	-475	2625	603
R308	550	1025	603	R44	840	410	603
R309	4925	1275	603	R45	6312.5	5637.5	603
R31	1237.5	1330	603	R46	485	4730	603

R47	5775	5637.5	603
R48	3390	4260	603
R49	3737.5	3750	603
R5	5250	1275	603
R50	4125	3875	603
R51	2750	4125	603
R52	3100	-50	603
R53	2925	300	603
R54	3202.5	4702.5	SMDRES805
R55	3040	2570	603
R56	3260	2605	603
R57	3260	2545	603
R58	3260	2485	603
R59	3475	2650	603
R6	250	1025	603
R60	3975	2650	603
R61	3475	2275	603
R62	2275	5637.5	603
R63	2437.5	5637.5	603
R64	1900	5637.5	603
R65	2062.5	5637.5	603
R66	3450	1100	603
R67	1525	5637.5	603
R68	1687.5	5637.5	603
R69	1150	5637.5	603
R7	4775	2150	603
R70	1312.5	5637.5	603
R71	675	5637.5	603
R72	837.5	5637.5	603
R73	300	5637.5	603
R74	462.5	5637.5	603
R75	-75	5637.5	603
R76	87.5	5637.5	603
R77	-450	5637.5	603
R78	-287.5	5637.5	603
R79	2350	5637.5	603
R8	4775	2595	603
R80	2512.5	5637.5	603
R81	1975	5637.5	603
R82	2137.5	5637.5	603
R83	1600	5637.5	603
R84	1762.5	5637.5	603
R85	4581.5	4650	603
R86	4656.5	4650	603
R87	1225	5637.5	603
R88	1387.5	5637.5	603
R89	750	5637.5	603
R9	2800	3675	603
R90	4015	4690	603
R91	4090	4690	603
R92	3940	4690	603
R93	3940	4690	603
R94	3790	4690	603
R95	3790	4690	603
R96	3465	4690	603
R97	3540	4690	603
R98	3390	4690	603
R99	3390	4690	603
RADDR0	7125	3600	TST_PT_PAD50CIR32D
RAS	-720	3960	TST_PT_PAD50CIR32D
RN1	699.244	4275.472	RN4
RN10	5294.244	2824.527	RN4
RN100	1599.527	3849.244	RN4
RN101	-824.527	899.244	RN4
RN102	6475.756	1474.527	RN4
RN103	-824.527	749.244	RN4
RN104	86.744	2024.527	RN4
RN105	236.744	2024.527	RN4
RN106	6774.244	1250.472	RN4
RN107	6775.756	1474.527	RN4
RN108	2860.756	2954.527	RN4
RN109	2560.756	3174.527	RN4
RN11	5124.244	2824.527	RN4
RN110	5475.756	2824.527	RN4
RN111	6924.244	1250.472	RN4
RN112	6474.244	1250.472	RN4
RN113	6925.756	1474.527	RN4
RN114	6624.244	1250.472	RN4
RN115	6625.756	1474.527	RN4
RN116	6475.756	2349.527	RN4
RN117	6775.756	2349.527	RN4
RN118	6925.756	2349.527	RN4
RN119	6474.244	2125.472	RN4
RN12	-824.527	1199.244	RN4
RN120	6624.244	2125.472	RN4
RN121	6924.244	2125.472	RN4
RN122	6774.244	2125.472	RN4
RN123	6625.756	2349.527	RN4
RN124	6084.527	939.244	RN4
RN125	6084.527	1124.244	RN4
RN126	3850.756	1599.527	RN4
RN127	3700.756	1599.527	RN4
RN128	3550.756	1599.527	RN4
RN129	3400.756	1599.527	RN4
RN13	-824.527	1799.244	RN4
RN130	3849.244	1825.472	RN4
RN131	3699.244	1825.472	RN4
RN132	3549.244	1825.472	RN4
RN133	3399.244	1825.472	RN4
RN134	4069.527	1964.244	RN4
RN135	499.527	4079.244	RN4
RN136	1425.472	2425.756	RN4
RN137	1425.472	2275.756	RN4
RN138	1650.472	2275.756	RN4
RN139	1650.472	2425.756	RN4
RN14	1524.527	1724.244	RN4
RN15	-824.527	1649.244	RN4
RN16	-824.527	1499.244	RN4
RN17	2024.244	1300.472	RN4
RN18	3475.472	2374.244	RN4
RN19	3974.527	2350.756	RN4
RN2	6084.527	1669.244	RN4
RN20	6999.244	424.527	RN4
RN21	5749.244	2575.472	RN4
RN22	5599.244	2575.472	RN4
RN23	5449.244	2575.472	RN4
RN24	5299.244	2575.472	RN4
RN25	6084.527	1819.244	RN4
RN26	5149.244	2575.472	RN4
RN27	-513.256	2024.527	RN4
RN28	-363.256	2024.527	RN4
RN29	-363.256	1625.472	RN4
RN3	6084.527	1969.244	RN4
RN30	-213.256	1625.472	RN4
RN31	4605.472	3280.756	RN4
RN32	-825.472	1950.756	RN4
RN33	5475.756	2825.472	RN4
RN34	6084.527	2119.244	RN4
RN35	4605.472	3104.244	RN4
RN36	6084.527	1519.244	RN4

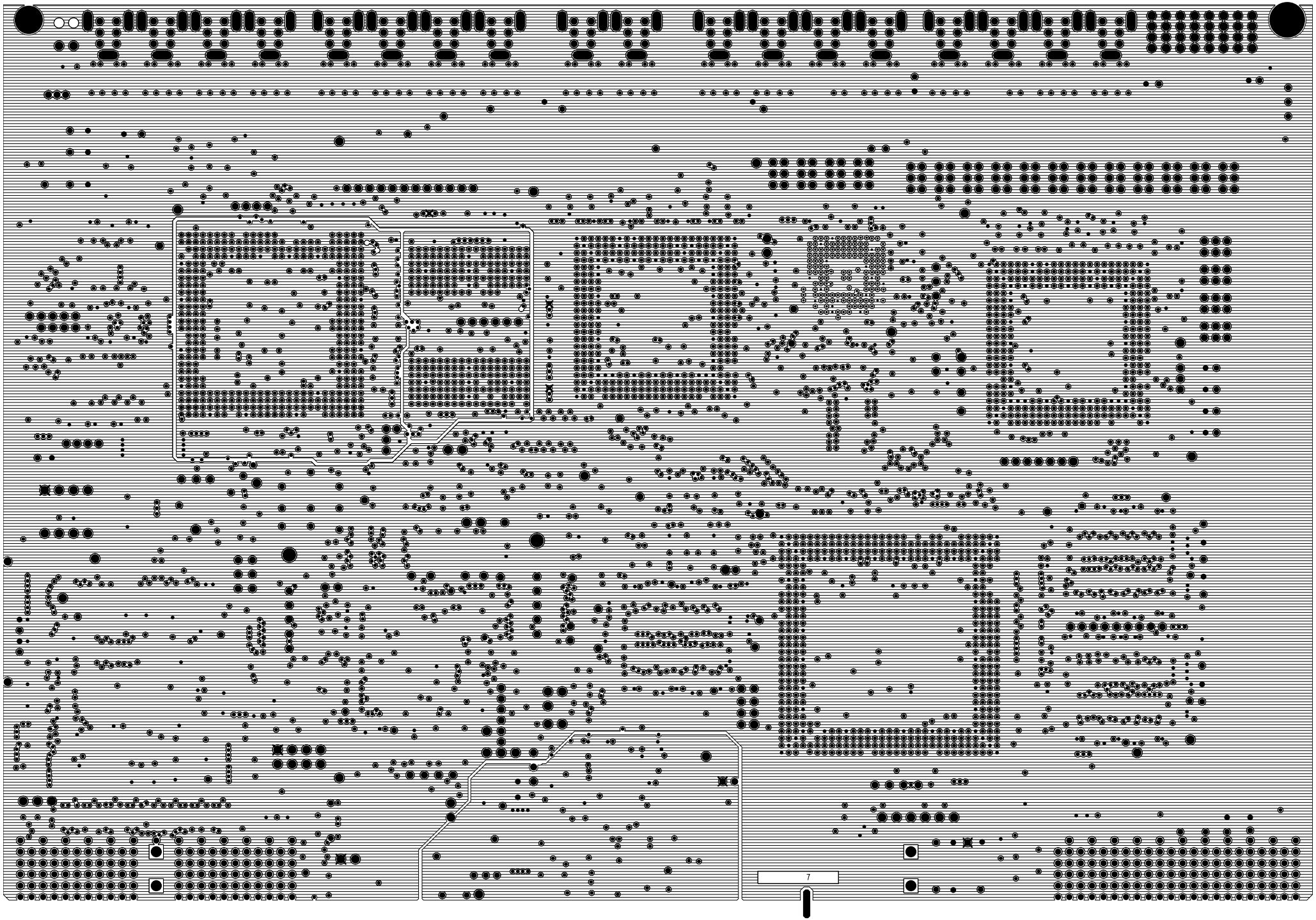
RN37	-825.472	2100.756	RN4
RN38	2025.472	1475.756	RN4
RN39	575.472	1474.244	RN4
RN4	3475.472	2749.244	RN4
RN40	575.472	1624.244	RN4
RN41	575.472	1774.244	RN4
RN42	599.244	3075.472	RN4
RN43	449.244	3075.472	RN4
RN44	2560.756	2954.527	RN4
RN45	2709.244	2954.527	RN4
RN46	2860.756	3174.527	RN4
RN47	2709.244	3174.527	RN4
RN48	4870.472	3280.756	RN4
RN49	299.244	3075.472	RN4
RN5	3974.527	2750.756	RN4
RN50	499.527	3649.244	RN4
RN51	499.527	3824.244	RN4
RN52	-213.256	2024.527	RN4
RN53	749.244	3075.472	RN4
RN54	19.527	3899.244	RN4
RN55	-405.472	3899.244	RN4
RN56	4605.472	3279.244	RN4
RN57	4870.472	3104.244	RN4
RN58	4870.472	3279.244	RN4
RN59	4870.472	3105.756	RN4
RN6	-824.527	1349.244	RN4
RN60	-180.472	3899.244	RN4
RN61	-325.472	4249.244	RN4
RN62	-325.472	3574.244	RN4
RN63	5199.527	3999.244	RN4
RN64	-63.256	2024.527	RN4
RN65	150.756	490.472	RN4
RN66	-149.244	490.472	RN4
RN67	6050.472	-0.756	RN4
RN68	1599.527	4149.244	RN4
RN69	6050.472	149.244	RN4
RN7	221.744	1625.472	RN4
RN70	6050.472	299.244	RN4
RN71	-824.527	900.756	RN4
RN72	-600.756	490.472	RN4
RN73	-450.756	490.472	RN4
RN74	-300.756	490.472	RN4
RN75	299.244	490.472	RN4
RN76	449.244	490.472	RN4
RN77	-150.756	490.472	RN4
RN78	574.527	924.244	RN4
RN79	-824.527	750.756	RN4
RN8	5295.756	2824.527	RN4
RN80	574.527	774.244	RN4
RN81	-0.756	490.472	RN4
RN82	149.244	490.472	RN4
RN83	-824.527	1050.756	RN4
RN84	-825.472	1050.756	RN4
RN85	1599.527	3699.244	RN4
RN86	2300.756	4599.527	RN4
RN87	4605.472	3105.756	RN4
RN88	-599.244	490.472	RN4
RN89	2324.244	3225.472	RN4
RN9	5125.756	2824.527	RN4
RN90	-0.756	489.527	RN4
RN91	1599.527	4299.244	RN4
RN92	1599.527	3549.244	RN4
RN93	-449.244	490.472	RN4
RN94	-299.244	490.472	RN4
RN95	300.756	490.472	RN4
RN96	450.756	490.472	RN4
RN97	574.527	775.756	RN4
RN98	574.527	925.756	RN4
RN99	1599.527	3999.244	RN4
RRDENB	7125	3450	TST_PT_PAD50CIR32D
RW	2280	3920	TST_PT_PAD50CIR32D
TDAT0	1405	4850	TST_PT_PAD50CIR32D
TP_2.5V	175	2825	TST_PT_PAD50CIR32D
TP_3.3V	5645	300	TST_PT_PAD50CIR32D
TP_RSTB	2425	2525	TST_PT_PAD50CIR32D
TP_VCC	3940	725	TST_PT_PAD50CIR32D
TP1	5200	700	TST_PT_PAD50CIR32D
TP10	670	2065	TST_PT_PAD50CIR32D
TP100	-625	3075	TST_PT_PAD50CIR32D
TP11	670	2165	TST_PT_PAD50CIR32D
TP115	-750	5500	TST_PT_PAD50CIR32D
TP117	-630	5500	TST_PT_PAD50CIR32D
TP12	670	2265	TST_PT_PAD50CIR32D
TP13	1175	2075	TST_PT_PAD50CIR32D
TP14	2880	1705	TST_PT_PAD50CIR32D
TP15	2880	1805	TST_PT_PAD50CIR32D
TP16	2895	2140	TST_PT_PAD50CIR32D
TP17	2395	2145	TST_PT_PAD50CIR32D
TP18	2500	925	TST_PT_PAD60CIR36D
TP19	2625	4825	TST_PT_PAD60CIR36D
TP2	2065	770	TST_PT_PAD50CIR32D
TP20	4158.5	1119	TST_PT_PAD60CIR36D
TP22	1600	3175	TST_PT_PAD50CIR32D
TP23	5425	4300	TST_PT_PAD50CIR32D
TP24	5100	700	TST_PT_PAD50CIR32D
TP25	1600	3025	TST_PT_PAD50CIR32D
TP26	2125	4850	TST_PT_PAD50CIR32D
TP27	2625	725	TST_PT_PAD50CIR32D
TP28	5425	4200	TST_PT_PAD50CIR32D
TP3	1765	770	TST_PT_PAD50CIR32D
TP30	5300	700	TST_PT_PAD50CIR32D
TP31	1965	770	TST_PT_PAD50CIR32D
TP32	5000	700	TST_PT_PAD50CIR32D
TP33	-650	2000	TST_PT_PAD60CIR36D
TP38	7125	3775	TST_PT_PAD60CIR36D
TP39	7205	2985	TST_PT_PAD60CIR36D
TP4	4200	2585	TST_PT_PAD60CIR36D
TP40	150	4700	TST_PT_PAD60CIR36D
TP41	4175	5025	TST_PT_PAD60CIR36D
TP42	1865	770	TST_PT_PAD50CIR32D
TP43	1965	4850	TST_PT_PAD50CIR32D
TP45	5425	4100	TST_PT_PAD50CIR32D
TP46	2625	825	TST_PT_PAD50CIR32D
TP47	2045	4850	TST_PT_PAD50CIR32D
TP48	2205	4850	TST_PT_PAD50CIR32D
TP49	2625	925	TST_PT_PAD50CIR32D
TP5	5115	3850	TST_PT_PAD60CIR36D
TP50	1275	750	TST_PT_PAD60CIR36D
TP51	2245	-60	TST_PT_PAD60CIR36D
TP52	-425	2275	TST_PT_PAD60CIR36D
TP53	5600	3675	TST_PT_PAD60CIR36D
TP54	1275	5175	TST_PT_PAD60CIR36D
TP55	275	2475	TST_PT_PAD60CIR36D
TP56	700	2800	TST_PT_PAD60CIR36D
TP57	2725	1250	TST_PT_PAD60CIR36D
TP58	3960	2195	TST_PT_PAD60CIR36D
TP59	2980	2850	TST_PT_PAD60CIR36D
TP6	7195	1015	TST_PT_PAD60CIR36D
TP60	5625	4675	TST_PT_PAD60CIR36D
TP61	2300	1075	TST_PT_PAD60CIR36D

TP62	2050	475	TST_PT_PAD60CIR36D
TP63	2050	575	TST_PT_PAD60CIR36D
TP64	1385	185	TST_PT_PAD60CIR36D
TP65	1285	185	TST_PT_PAD60CIR36D
TP68	2400	1075	TST_PT_PAD50CIR32D
TP7	570	2065	TST_PT_PAD50CIR32D
TP70	2300	925	TST_PT_PAD60CIR36D
TP71	2400	925	TST_PT_PAD60CIR36D
TP72	2400	1375	TST_PT_PAD50CIR32D
TP74	2400	1225	TST_PT_PAD50CIR32D
TP75	3075	1650	TST_PT_PAD50CIR32D
TP76	4025	725	TST_PT_PAD50CIR32D
TP77	3825	900	TST_PT_PAD60CIR36D
TP78	7025	2700	TST_PT_PAD50CIR32D
TP79	6200	2600	TST_PT_PAD50CIR32D
TP8	570	2165	TST_PT_PAD50CIR32D
TP80	6825	925	TST_PT_PAD60CIR36D
TP81	3225	3250	TST_PT_PAD50CIR32D
TP82	1450	2680	TST_PT_PAD50CI32D
TP86	4420	3770	TST_PT_PAD50CIR32D
TP88	1265	2075	TST_PT_PAD50CIR32D
TP9	570	2265	TST_PT_PAD50CIR32D
TP99	-400	3075	TST_PT_PAD50CIR32D
U1	5075	1700	SBGA432
U10	2150	3525	PBGA119
U11	3150	550	SO8NB-3
U12	2150	4300	PBGA119
U13	3250	975	SO20WB
U14	-625	2600	DIP8_SOCKET
U15	-112.5	1300	QFP176
U16	3375	250	SO8NB-3
U17	4965	3560	SO14NB-2
U18	3375	12.5	SOIC8
U19	3450	3925	SBGA_304
U2	3725	2700	QSOP20
U20	6320	3745	SBGA_304
U21	1075	2825	SOT223-3
U22	4823.5	475	SSOP5_95
U23	896.5	1235	SSOP5_95
U25	525	5000	SO14NB-2
U26	2150	2775	SO14NB-2
U27	4781.5	4225	PBGA160
U3	3725	2300	QSOP20
U31	1800	1565	TQFP144-2
U4	3625	1725	TQFP_100-3
U5	6700	2250	TQFP_100-3
U6	6700	1375	TQFP_100-3
U7	775	3925	SBGA352
U8	-480	3510	TSOP54
U9	-465	4320	TSOP54
VDD1	2735	4005	JUMPER_3PIN_INLINE
VDD2	2735	3420	JUMPER_3PIN_INLINE
VX_DX_D0	5425	3575	TST_PT_PAD50CIR32D
VX1_CSB	5600	3575	TST_PT_PAD50CIR32D
VX1_TCLK	6300	2950	TST_PT_PAD50CIR32D
WE	-640	3960	TST_PT_PAD50CIR32D
WR	1565	4850	TST_PT_PAD50CIR32D
WRDAT0	700	4725	TST_PT_PAD50CIR32D
WRPRTY	550	4725	TST_PT_PAD50CIR32D
WTPA	375	2825	TST_PT_PAD50CIR32D
Y1	3665	746	CRYS_MA-505
Y2	3125	2300	OSC-2
Y3	1700	2775	OSC-2
Y4	0	4975	OSC-2
Y5	4515	3585	OSC-2
ZQ1	1900	4675	JUMPER_3PIN_INLINE
ZQ2	1640	3390	JUMPER_3PIN_INLINE

22. APPENDIX I: GLOSSARY

ADSL	Asymmetric Digital Subscriber Line
ATM	Asynchronous Transfer Mode
CPLD	CMOS Programmable Logic Device
DSLAM	Digital Subscriber Line Access Multiplexer
LCD	Loss of Cell Delineation
LED	Light Emitting Diode
LOS	Loss of Signal
LSW	Least Significant Word
LVDS	Low Voltage Differential Signal
Metadriver	= VORTEX Chipset Driver (card level driver)
MSW	Most Significant Word
NBT SSRAM	No-bus-turnaround Synchronous Static RAM
PCB	Printed Circuit Board
POTS	Plain Old Telephony System
SDRAM	Synchronous Dynamic Random Access Memory
SEEP	Serial EEPROM
SONET	Synchronous Optical NETwork
SSRAM	Synchronous Static RAM
S/UNI	SATURN User Network Interface
Telco	Telephone Company
UTOPIA	Universal Test & Operations PHY Interface
VCC	Virtual Channel Connection
VPC	Virtual Path Connection

3V3_A_PLANE



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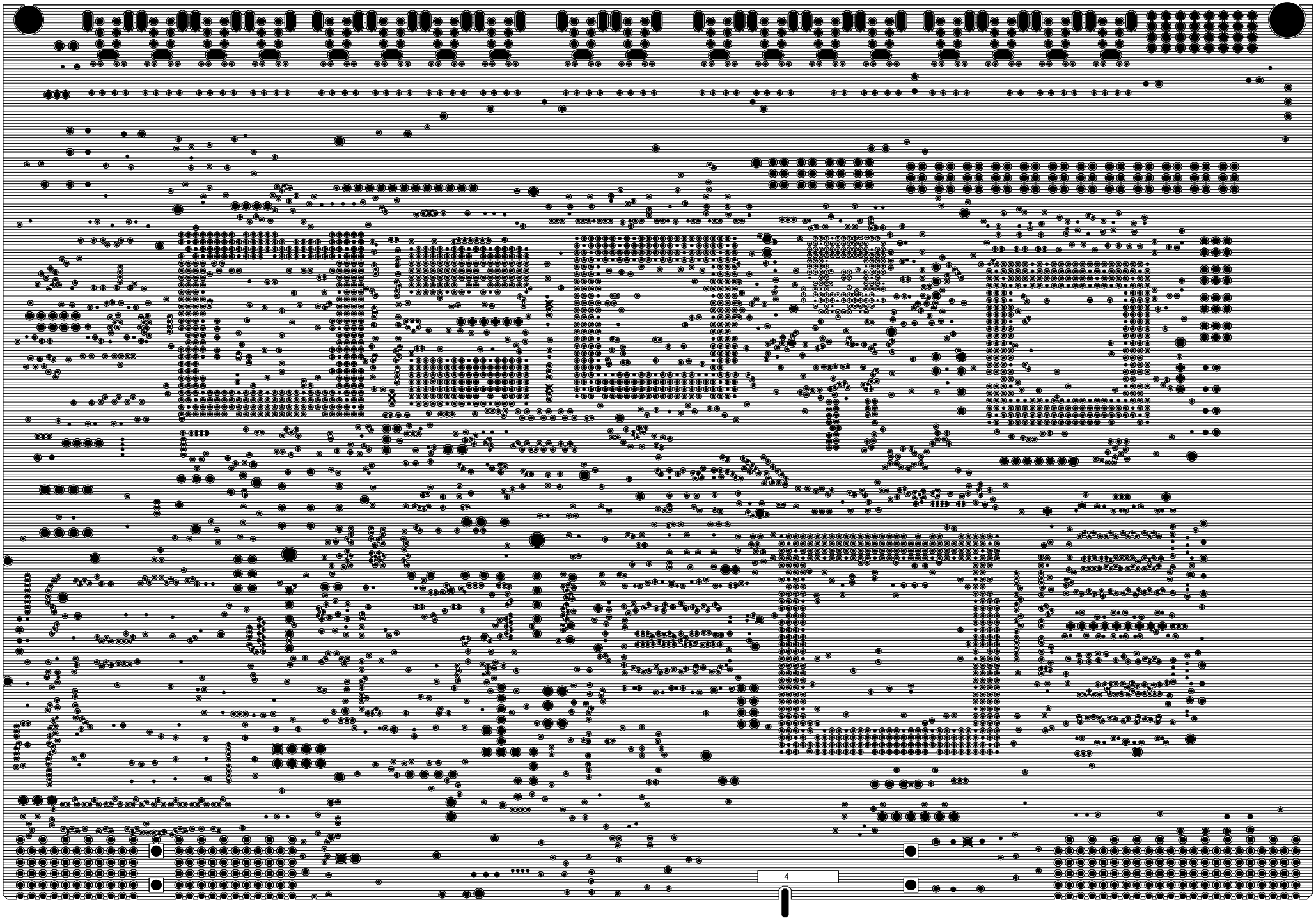
3V3 PLANE



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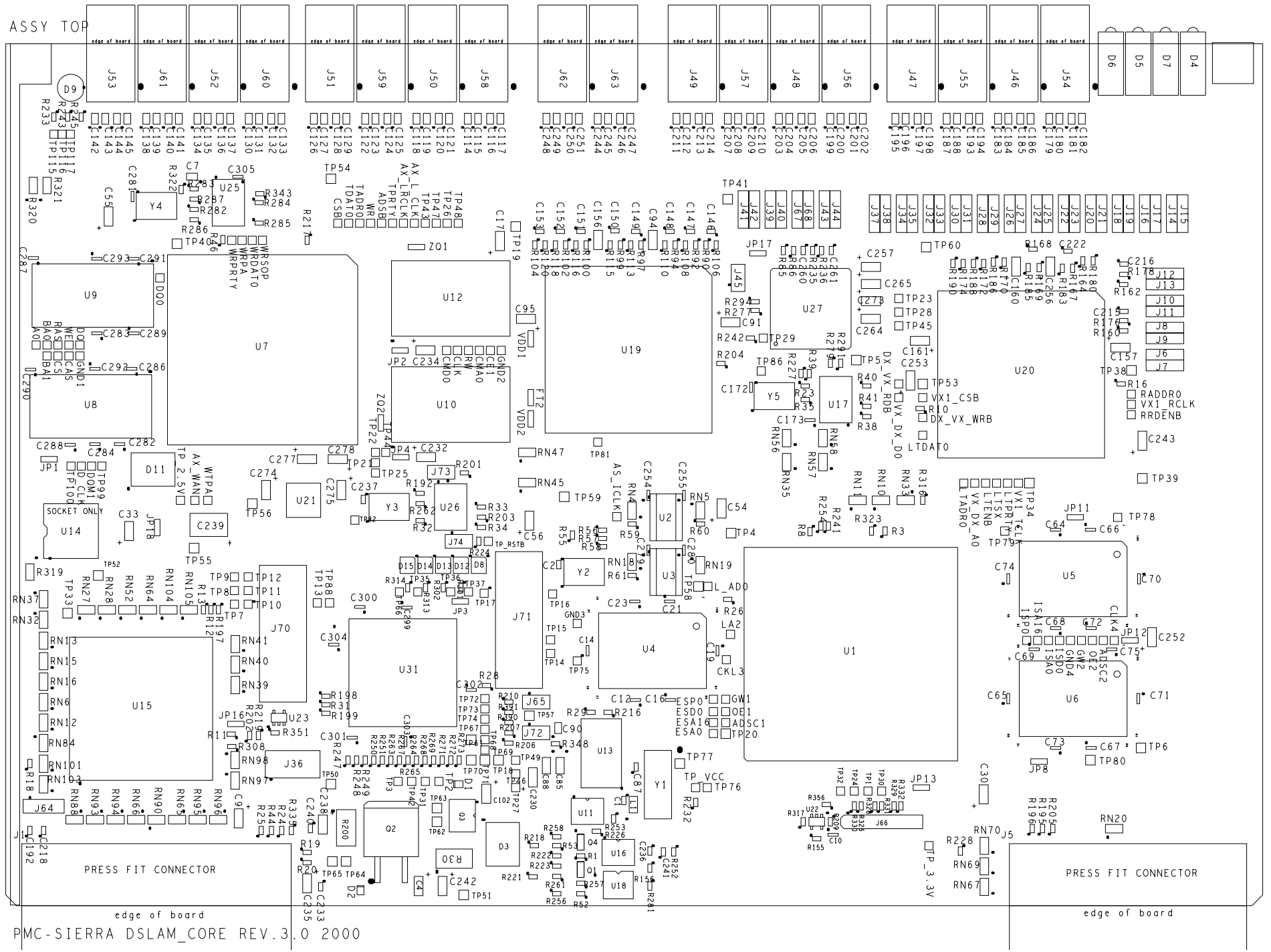
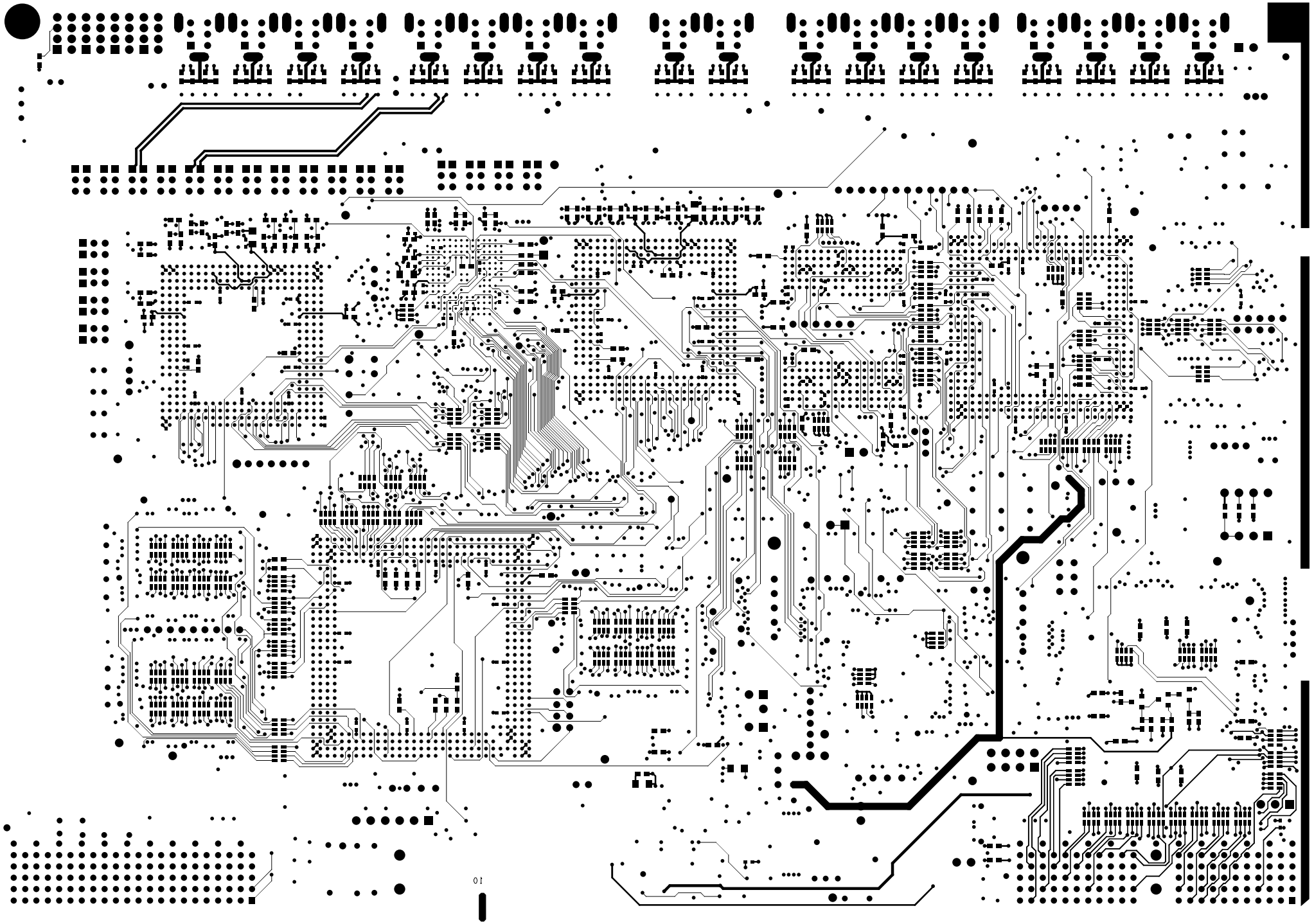
ASSY BOTTOM
PMC-SIERRA DSLAM_CORE REV.3.0 2000
R246

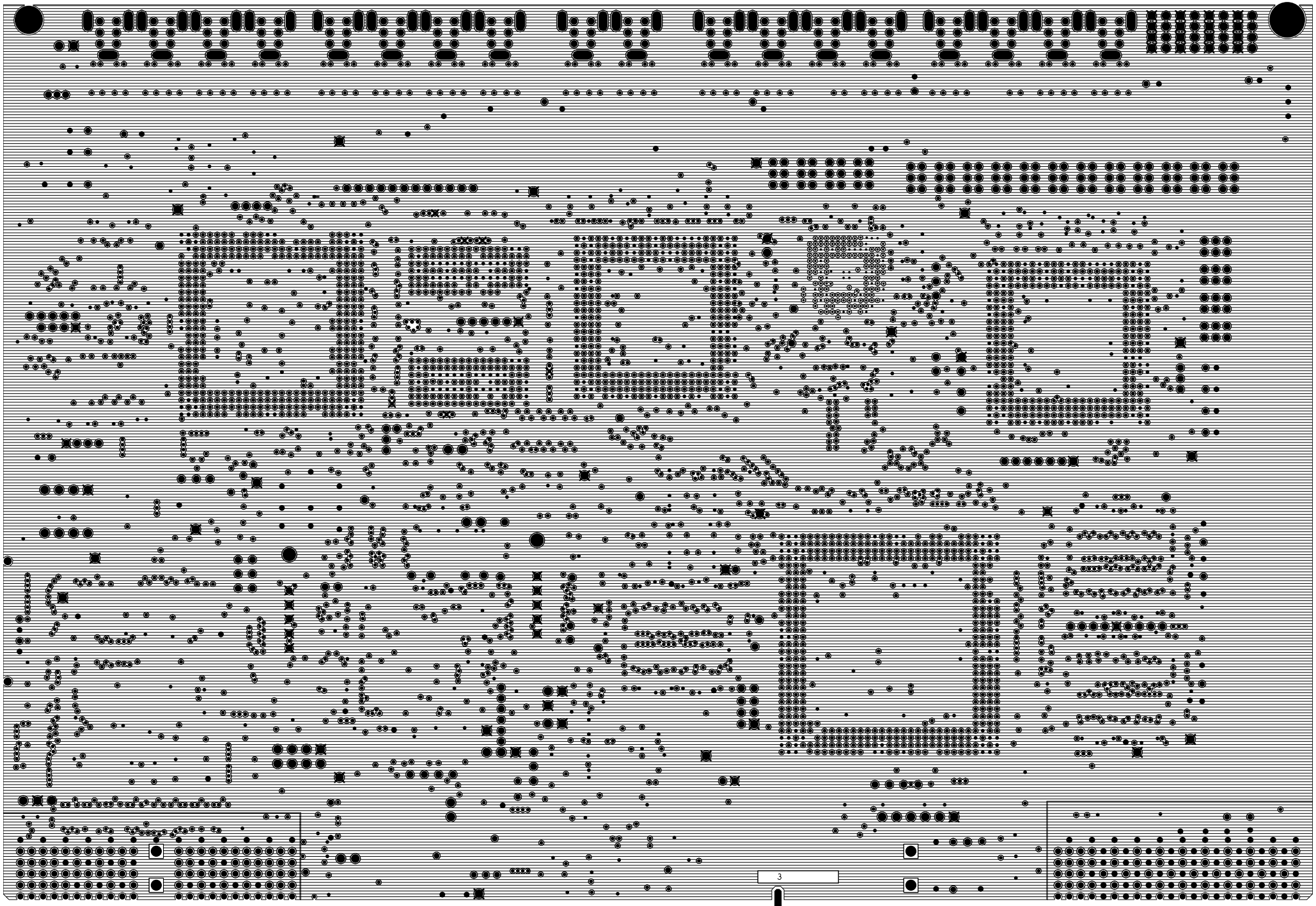

ASSY TOP
edge of board
J53
J61
J52
J60
J51
J59
J50
J58
J62
J63
J49
J57
J48
J56
J47
J55
J46
J54
D6
D5
D7
D4
D9
U9
U7
U8
U12
U10
U19
U27
U20
U17
U14
SOCKET ONLY
U21
U26
U2
U3
U4
U1
U5
U6
U15
U31
J70
J71
J72
J73
J74
J65
J66
J36
J64
U11
U13
U16
U18
Y1
Y2
Y3
Y4
Y5
Q1
Q2
Q3
D1
D2
D3
PRESS FIT CONNECTOR
edge of board
PRESS FIT CONNECTOR
edge of board
PMC-SIERRA DSLAM_CORE REV.3.0 2000

BOTTOM LAYER



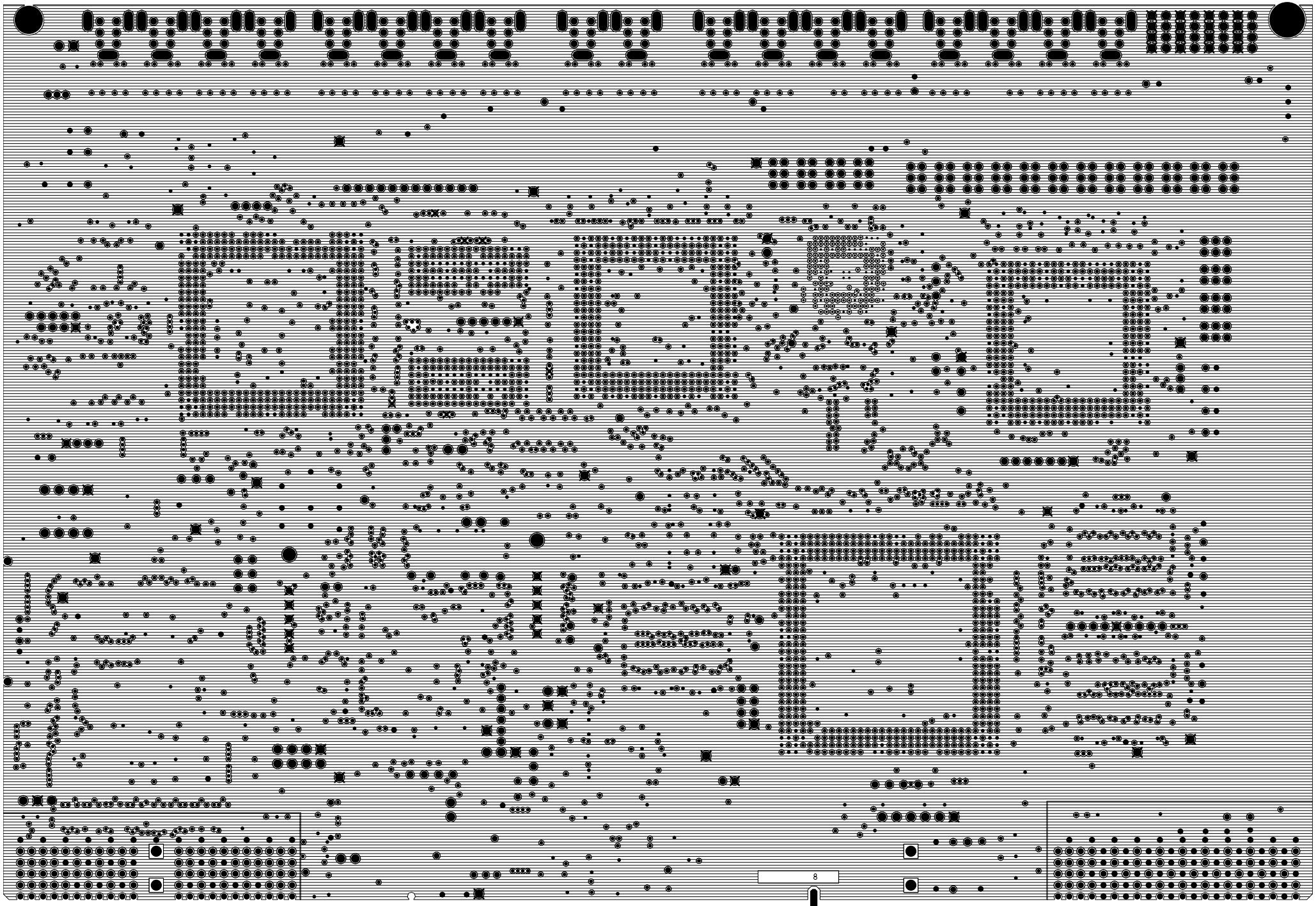
PMC-SIERRA DSLAM_CORE REV.3.0 2000

GND PLANE

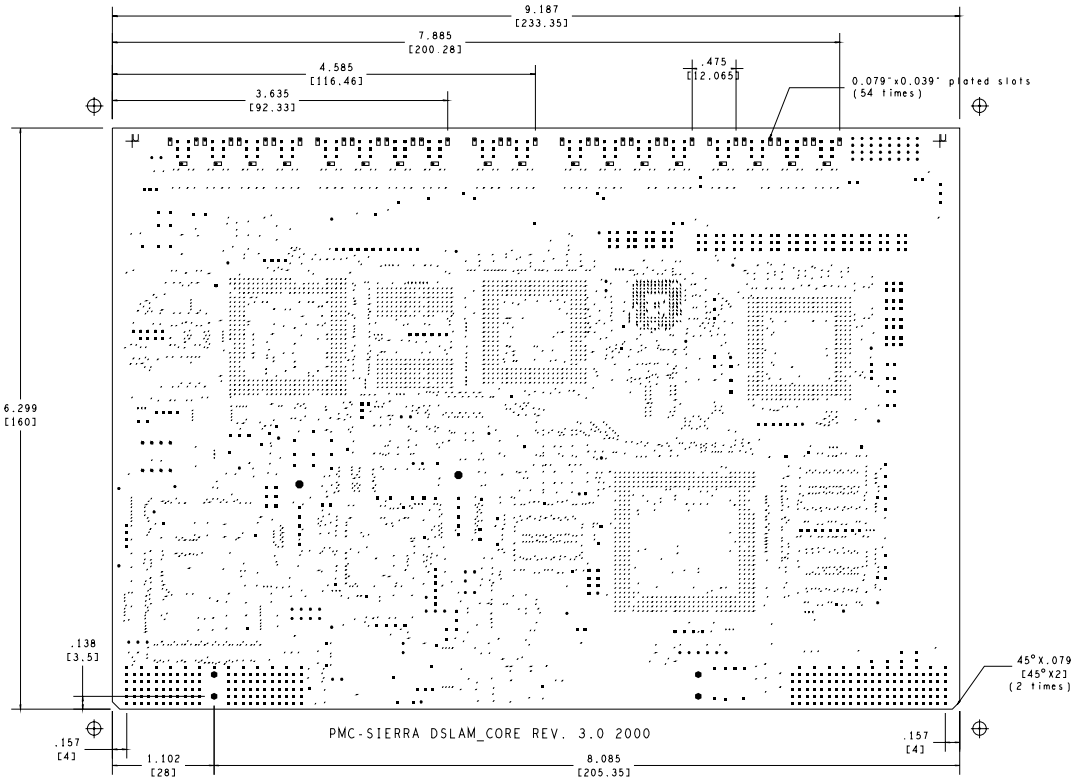


PMC-SIERRA DSLAM_CORE REV.3.0 2000

GND PLANE



REVISIONS					
REV	DESCRIPTION	DATE YY	MM	DD	APPROVED



	Material	Layer Type	Etch Name	Film Type	Thickness	Dielectric Constant
#	COPPER	CONDUCTOR	TOP	POSITIVE	0.72 mil	-------
	FR-4	DIELECTRIC	-------	-------	4.0 mil	4.5
#	COPPER	CONDUCTOR	SIG1	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	6.0 mil	4.5
	COPPER	CONDUCTOR	GND_PLANE	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	3.0 mil	4.5
	COPPER	CONDUCTOR	3V3_PLANE	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	7.0 mil	4.5
#	COPPER	CONDUCTOR	SIG2	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	17.0 mil	4.5
#	COPPER	CONDUCTOR	SIG3	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	7.0 mil	4.5
	COPPER	CONDUCTOR	3V3_A_LANE	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	3.0 mil	4.5
	COPPER	CONDUCTOR	GND1_PLANE	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	6.0 mil	4.5
#	COPPER	CONDUCTOR	SIG4	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	4.0 mil	4.5
#	COPPER	CONDUCTOR	BOTTOM	POSITIVE	0.72 mil	-------

FINISHED HOLES SIZE			
All Units are in mils			
FIGURE	SIZE	PLATED	QTY
·	12.0	PLATED	149
·	13.0	PLATED	4011
·	15.0	PLATED	60
▪	25.0	PLATED	103
▪	26.0	PLATED	244
▪	32.0	PLATED	366
▪	36.0	PLATED	93
▪	39.0	PLATED	54
▪	39.37	PLATED	2
▪	42.0	PLATED	8
⊕	149.606	PLATED	1
⊕	150.0	PLATED	1
●	78.74	NOT PLATED	4
●	94.0	NOT PLATED	2

ARTWORK FILM
TOP LAYER
SIG1 LAYER
GROUND PLANE
3V3 PLANE
SIG2 LAYER
SIG3 LAYER
3V3_A PLANE
GROUND PLANE
SIG4 LAYER
BOTTOM LAYER
SOLDER MASK TOP
SOLDER MASK BOTTOM
SOLDER PASTE TOP
SOLDER PASTE BOTTOM
SILKSCREEN TOP
SILKSCREEN BOTTOM
MECH DRAWING
ASSEMBLY TOP
ASSEMBLY BOTTOM

Note: Controlled impedance traces are used on all signal layers.
They are: for 50 Ohm - 0.017" (top and bottom layer), 0.008" (inner)
for 65 Ohm - 0.008" (top and bottom)
for 75 Ohm - 0.005" all layers

Notes:
1. Copper thickness is 1/2 oz. on outer layers and 1 oz. on internal layers.
2. Total thickness of board shall be 70 mil +0/- 7mil.
3. The outline dimension are spedified on this drawing.
4. Material: See board material details above.
5. All holes shall have 1 mil minimum copper wall thickness.
6. Dielectric constant: See board material details above.
7. Silk screen shall be screened in monoconductive white base ink.
8. Maximum warp and twist of finished PCB shall not exceed 0.010 in/in per IPC-D-300.
9. All material comprising the PCB must be recongized by UL to the 94V-0 rating.

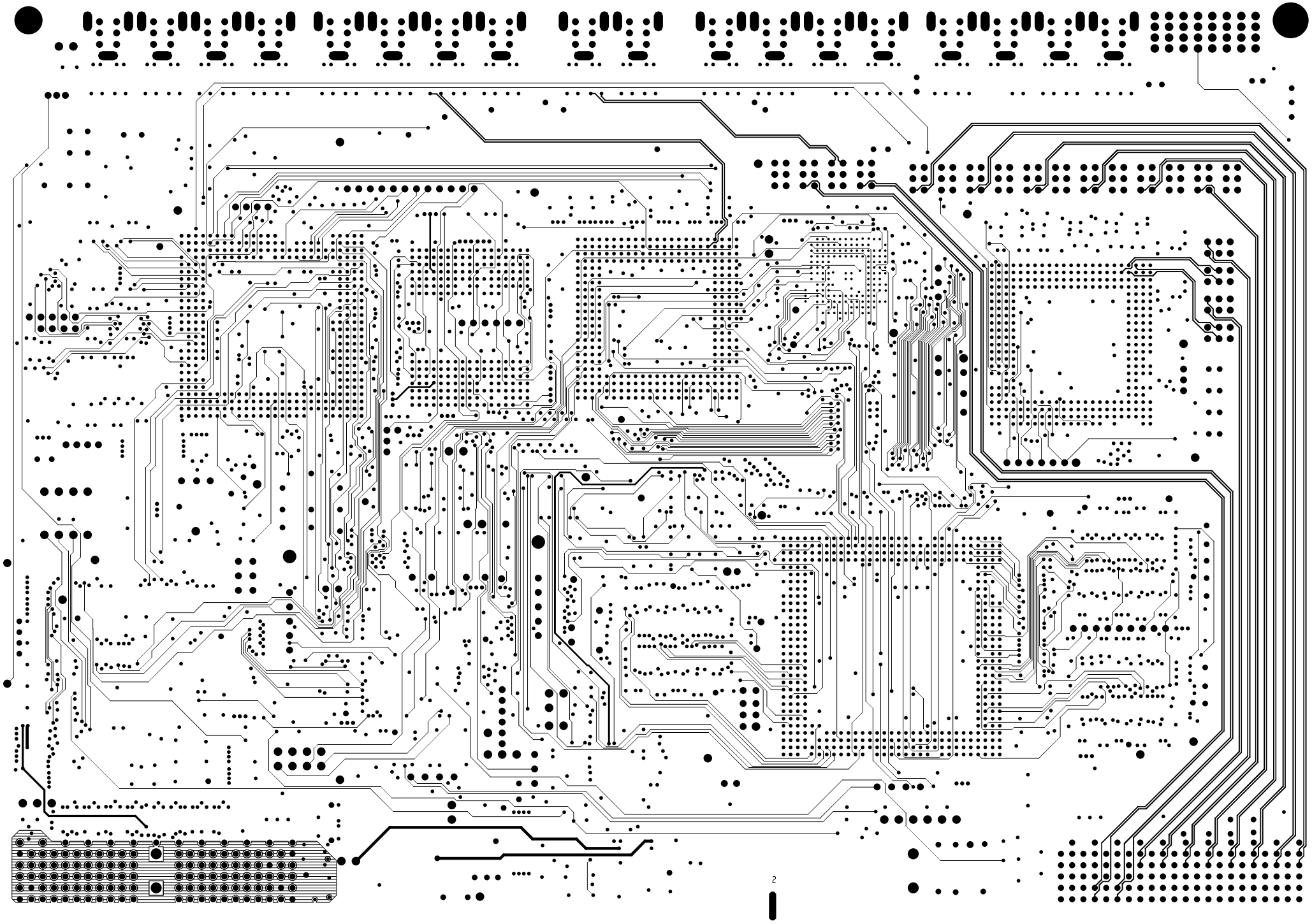
CAUTION !! 10. Ploated holes marked with SQUARE R - 0.026" - should be within -0/+0.003" tolerance.

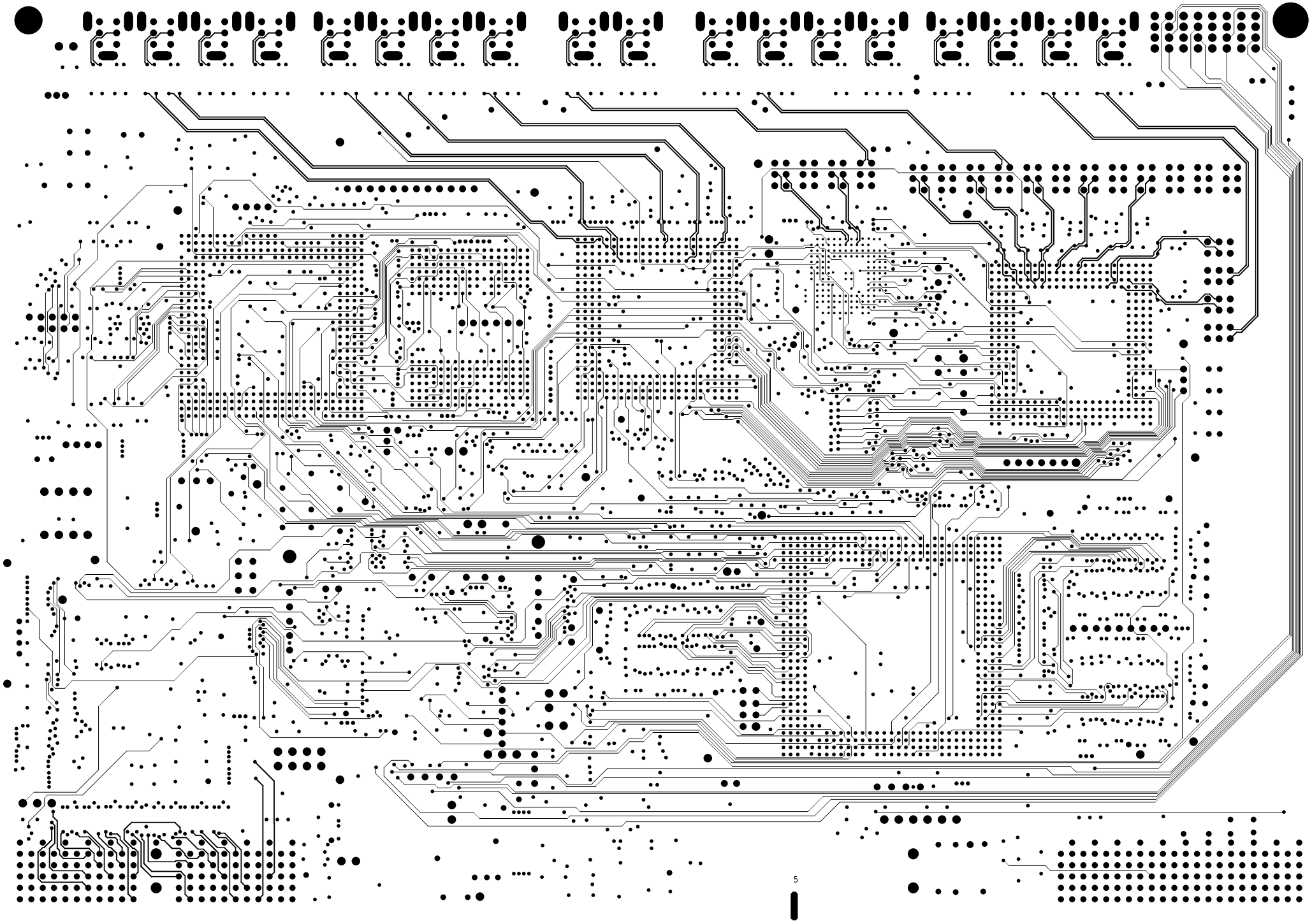
11. Add teardrops - if needed - to compensate for manufacturing process.

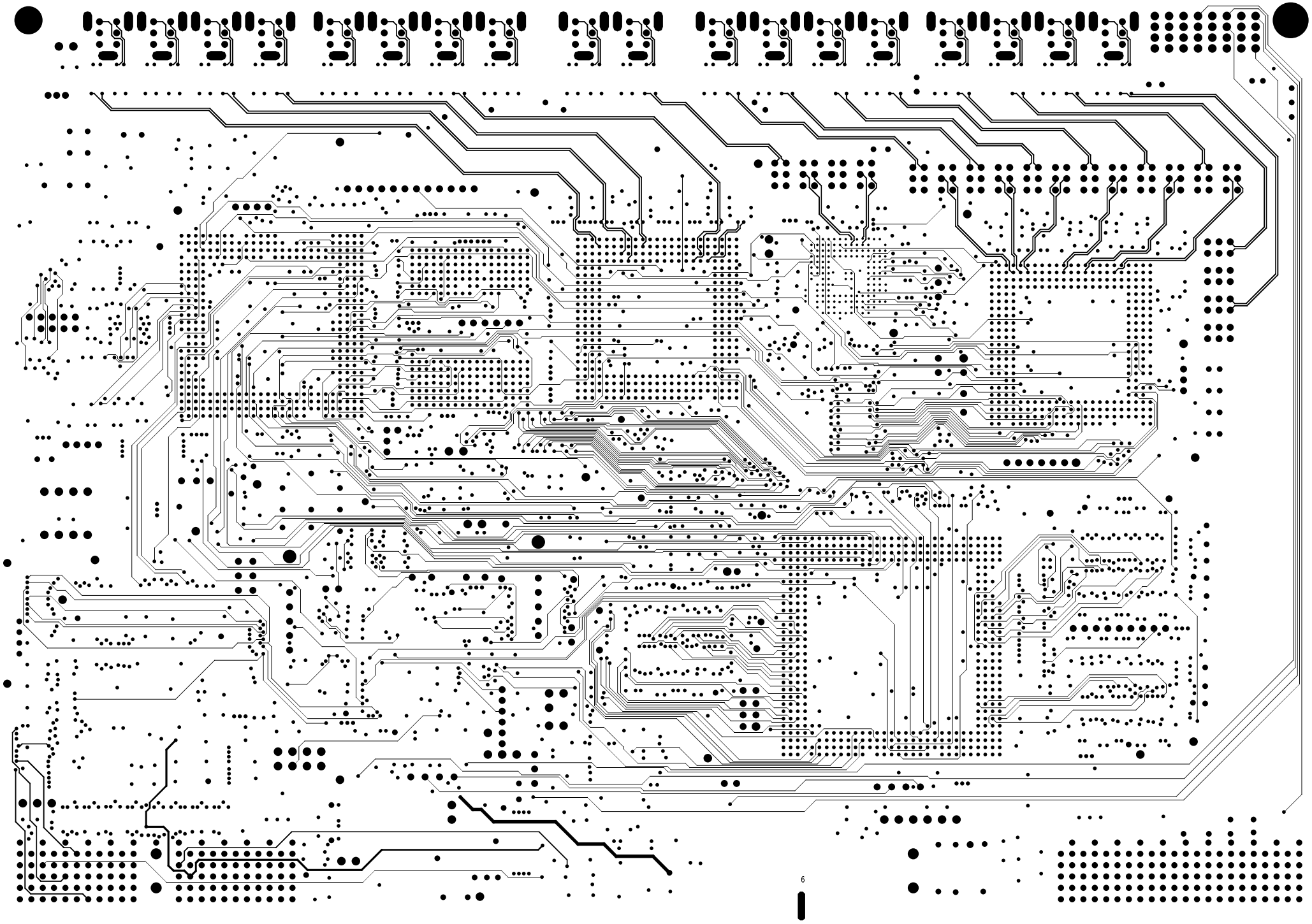
UNLESS OTHERWISE SPECIFIED		DATE YY	MM	DD
DIMENSIONS ARE IN INCHES	DRAWN			
TOLERANCES ON:				
2 PL DECIMALS ±	CHECKED			
3 PL DECIMALS ±	ENGRG			
ANGLES ±	ISSUED			
FRACTIONS ±				

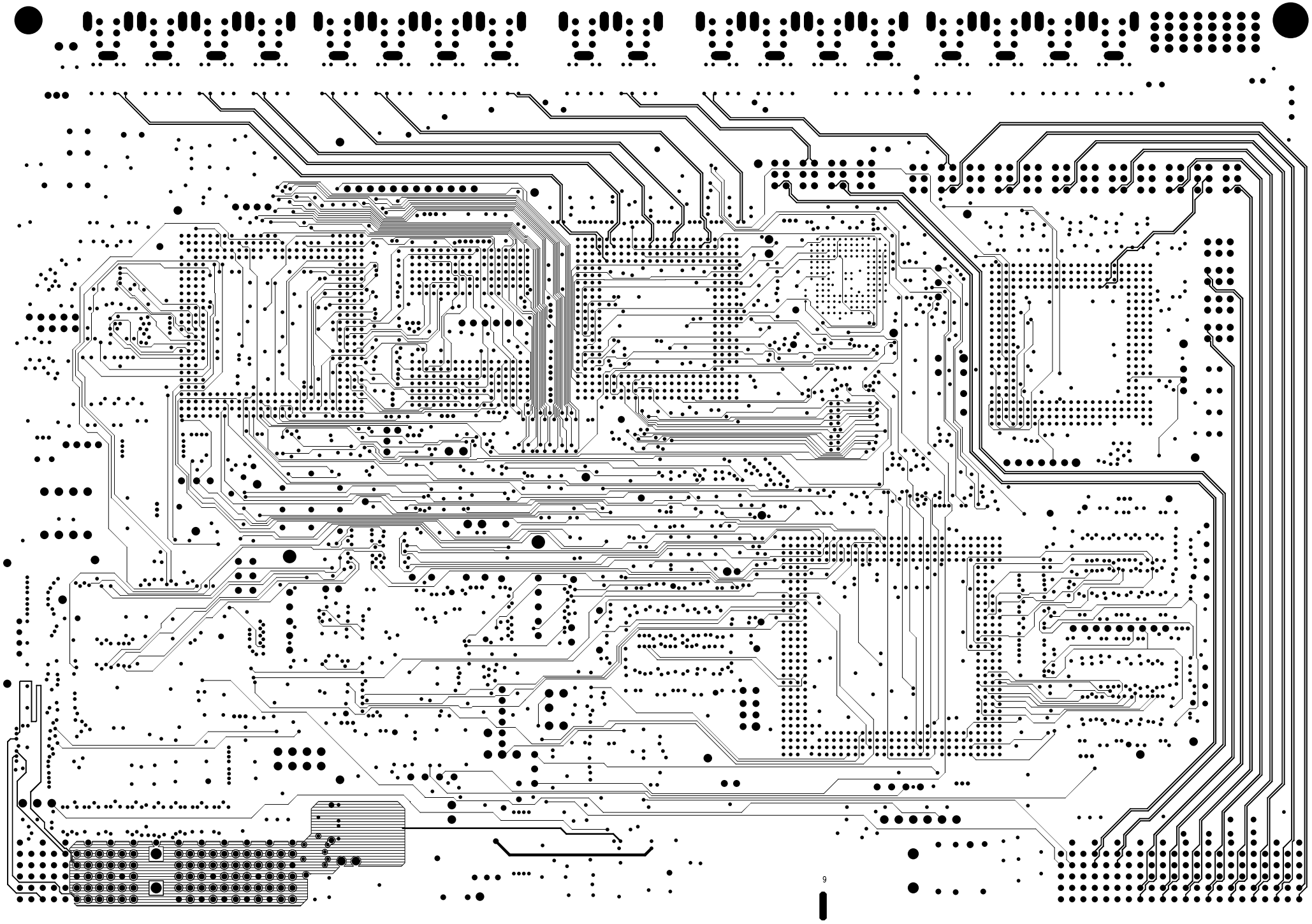
PMC-Sierra, Inc.
105-8555 Baxter Place, Burnaby B.C. Canada, V5A 4V7
Tel: 604 415-6000 Fax: 604 415-6200

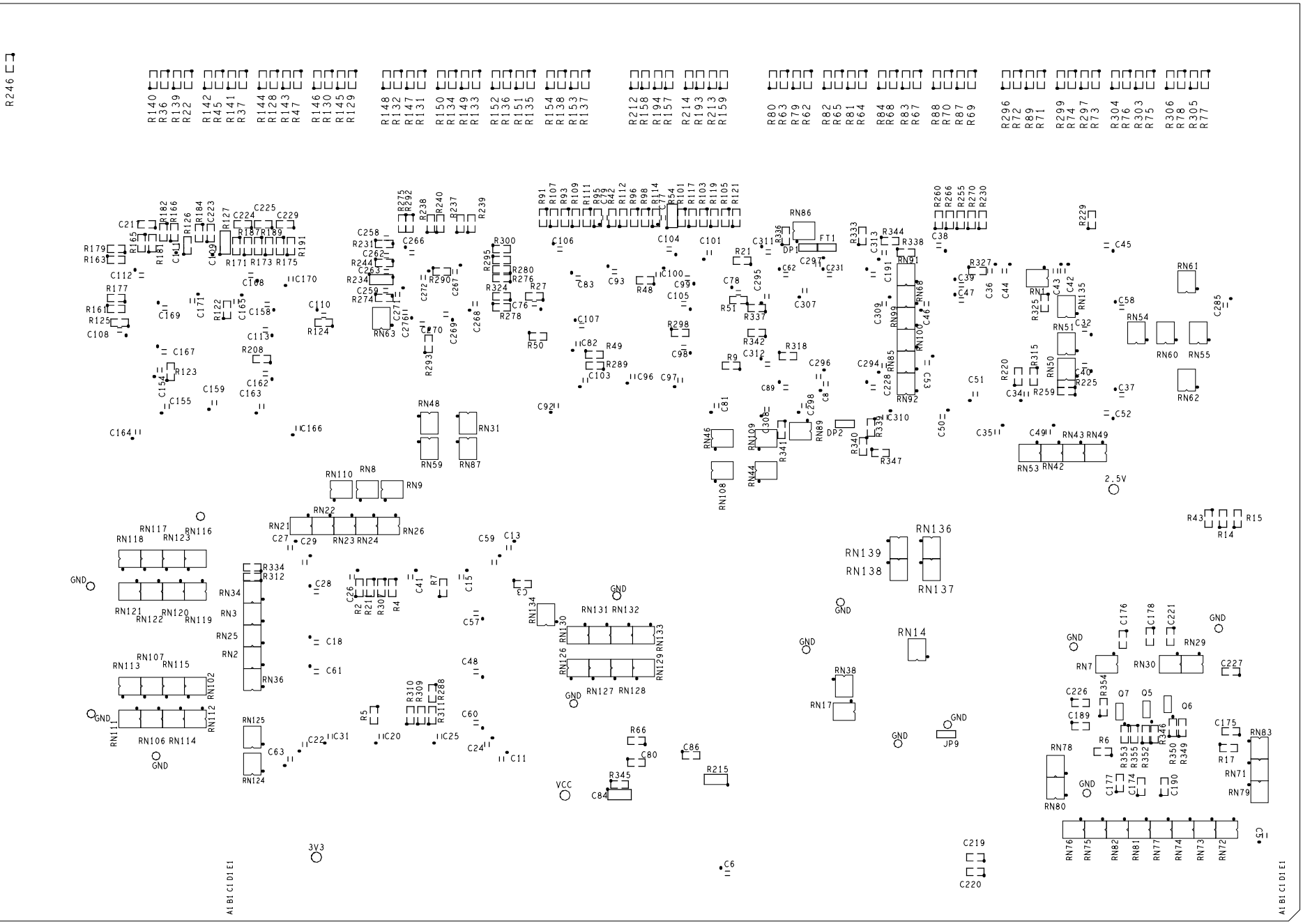
SIZE	FSCM NO	DWG NO
B		
SCALE	NTS	SHEET OF

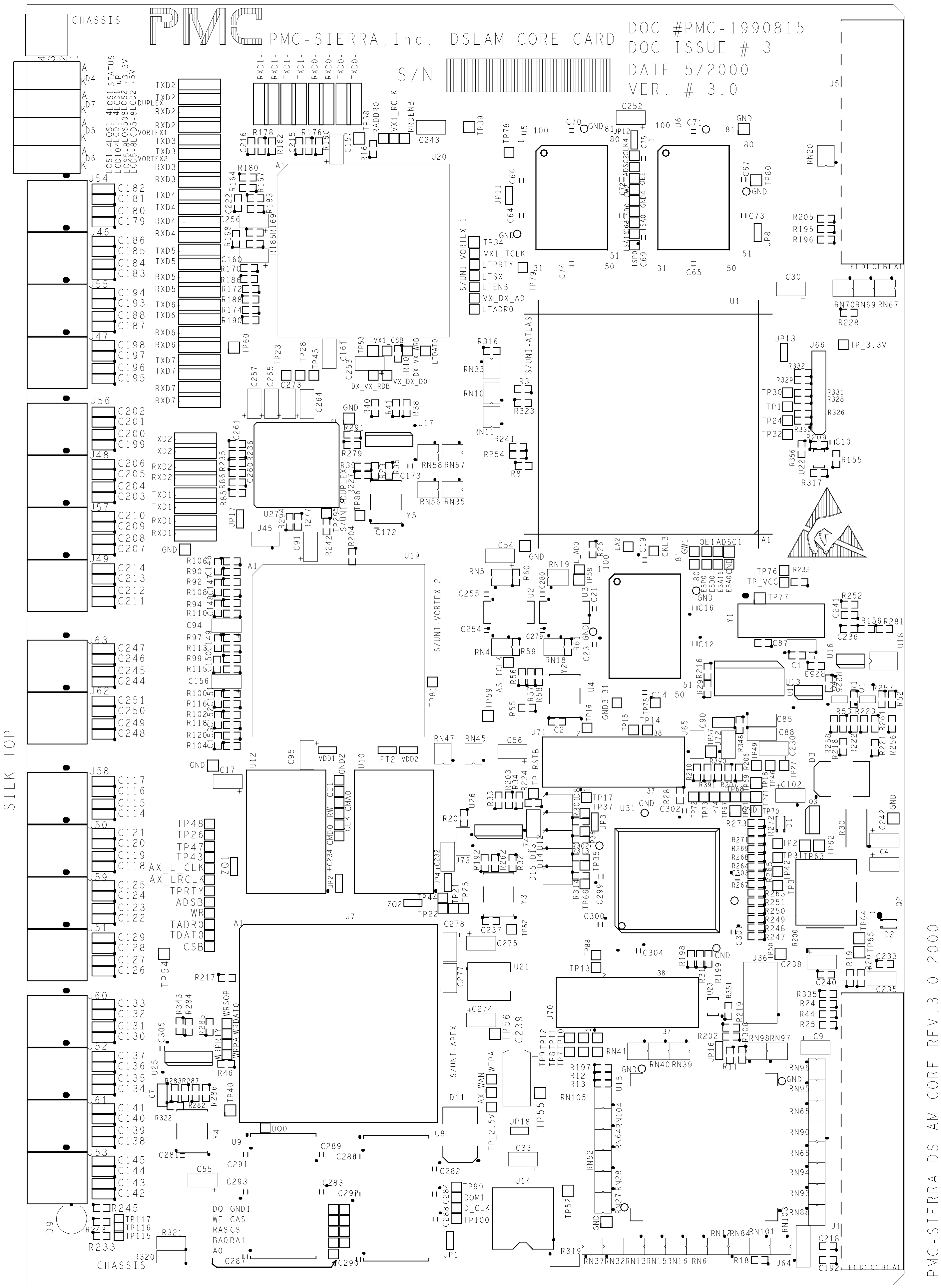




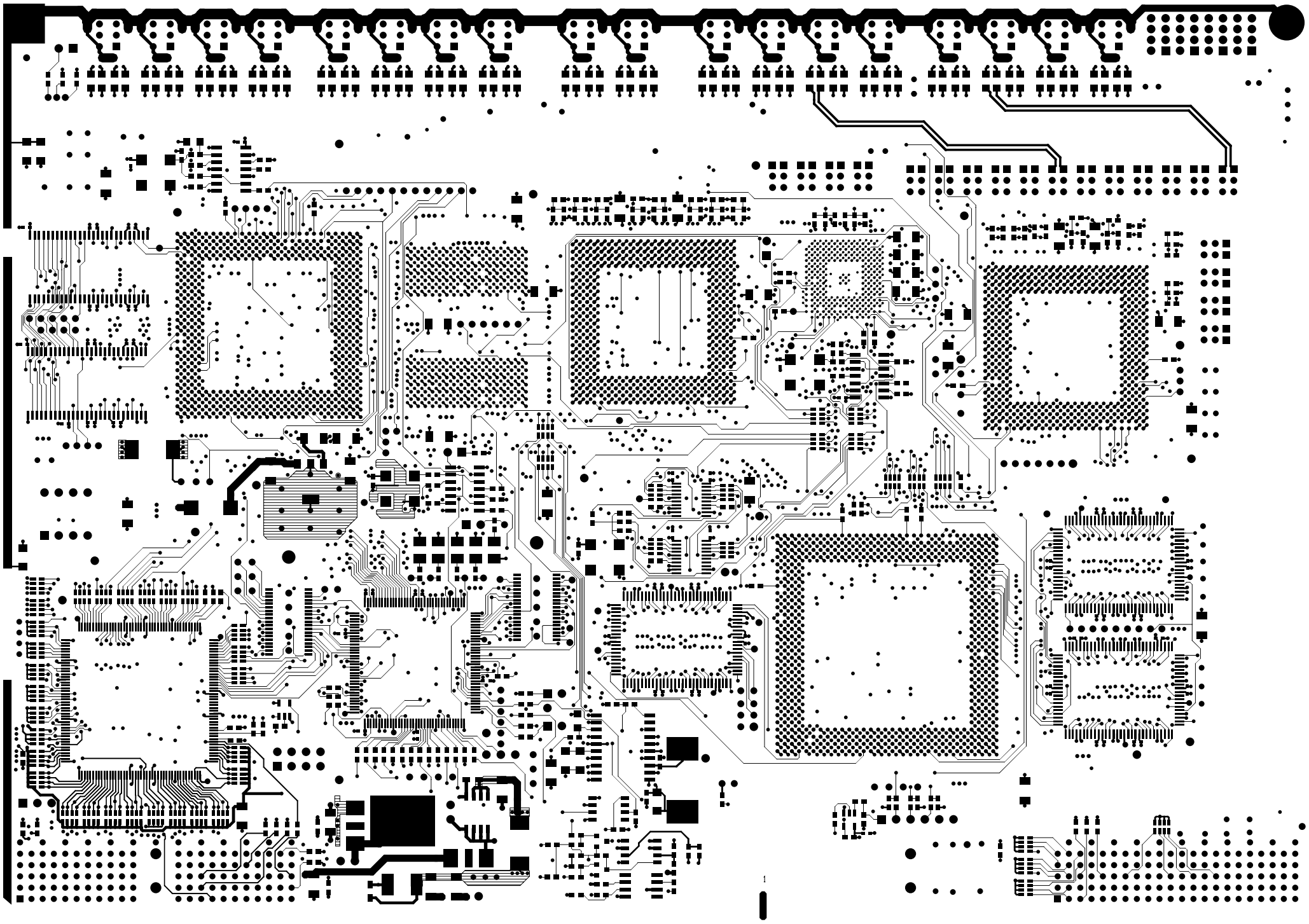







PMC-SIERRA, Inc. DSLAM_CORE CARD
DOC #PMC-1990815
DOC ISSUE # 3
DATE 5/2000
VER. # 3.0
S/N
CHASSIS
SILK TOP
PMC-SIERRA DSLAM_CORE REV.3.0 2000

TOP LAYER



PMC-SIERRA DSLAM_CORE REV.3.0 2000

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