
HA12167FB/HA12169FB

Audio Signal Processor for Cassette Deck (Deck 1 Chip)

HITACHI

ADE-207-110B (Z)

3rd. Edition

June 1997

Description

HA12167FB/HA12169FB is silicon monolithic bipolar IC providing REC volume system, Level meter system and Dolby noise reduction system in one chip.

Functions

- REC equalizer × 2 channel
- Equalizer volume × 2 channel
- Dolby B/C NR × 2 channel
- REC/PB input electronic volume × 2 channel
- Level Meter × 2 channel
- DAC for adjusting bias × 2 channel

Features

- Available to create characteristics of REC equalizer by changing external resistor, no coil
- Equalizer volume is available to calibrate recording automatically with micro-controller
- Electronic volume built-in is available to set the level of recording and play back automatically with micro-controller
- 4 types of input (3 out of 4 are by way of electronic volume)
- Input electronic control switching is irrelevant to REC/PB electronic control switching
- Dolby noise reduction system is available with double cassette decks (Unprocessed signal output available from recording out terminals during PB mode)
- Log-compressed level meter output is range from 0 V to 5 V (Usable as music search switchable gain of 0 dB and 20 dB respectively)
- Normal-speed/high-speed, normal/metal/chrome fully electronic control switching built-in
- NR-ON/OFF, Dolby B/C, MPX ON/OFF fully electronic control switching built-in
- Reduction of the number of pins by transferred serial data to electronic volume control switching and another control switching (Controllable from micro-controller directly)
- Small the number of external parts

HA12167FB/HA12169FB

Ordering Information

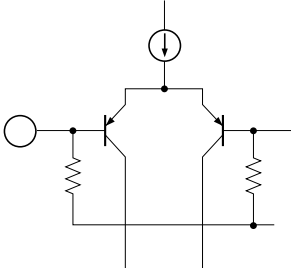
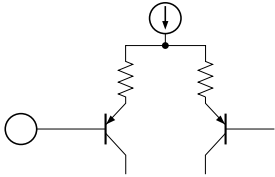
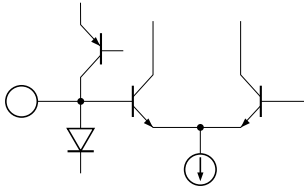
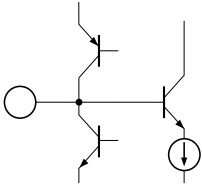
Type	Package	PB-OUT Level	REC-OUT Level	Dolby Level	Operating Voltage	
					Min	Max
HA12167FB	QFP-80	775 mVrms	300 mVrms	300 mVrms	12.0 V	15.0 V
HA12169FB	(14 × 14)	580 mVrms			11.0 V	15.0 V

* Dolby is a trademark of Dolby Laboratories Licensing Corporation.

A license from Dolby Laboratories Licensing Corporation is required for the use of this IC.

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Pin Description ($V_{cc} = 14\text{ V}$, $T_a = 25^\circ\text{C}$, No signal, The value in the show typical value.)

Pin No. (QFP-80)	Terminal Name	Zin	DC Voltage	Equivalent Circuit	Description
65	RPI	100 k Ω	$V_{cc}/2$		Recording input
76					
9	LM IN	100 k Ω			Level meter input
52					
12	EQ IN	100 k Ω			Equalizer input
49					
66, 67, 69 72, 74, 75	VRI	100 k Ω	$V_{cc}/2 + 0.7\text{ V}$		Volume input
30, 31	VCC	—	V_{cc}	—	Power supply
77	REF	—	$V_{cc}/2$	—	Ripple filter
62	NR IN	—	$V_{cc}/2$		NR processor input
79					
3	SS 1	—	$V_{cc}/2$		Spectral skewing amp input
58					
5	CCR	—	$V_{cc}/2$		Current controlled resistor output
56					

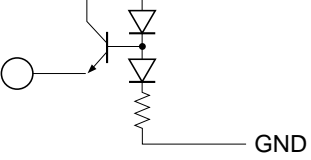
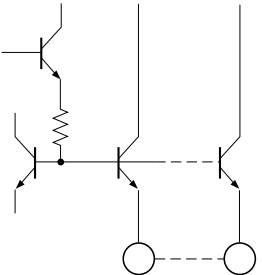
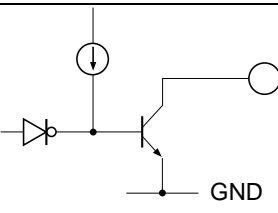
HA12167FB/HA12169FB

Pin Description ($V_{CC} = 14\text{ V}$, $T_a = 25^\circ\text{C}$, No signal, The value in the show typical value.)
(Cont)

Pin No. (QFP-80)	Terminal Name	Zin	DC Voltage	Equivalent Circuit	Description
63	IA OUT	—	$V_{CC}/2$		Input amp output
78					
61	VREF				Reference voltage
80					buffer output
2	PB OUT				Play back
59					(Decode) output
4	SS 2				Spectral skewing
57					amp. output
8	REC OUT				Recording
53					(Encode) output
15	EQ OUT				Equalizer output
46					
1	TP	$1.5\text{ k}\Omega$	$V_{CC}/2$		Bias trap terminal
60					
6	HLS DET	—	2.3 V		Time constant pin for rectifier
55					
7	LLS DET				
54					

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Pin Description ($V_{CC} = 14\text{ V}$, $T_a = 25^\circ\text{C}$, No signal, The value in the show typical value.)
(Cont)

Pin No. (QFP-80)	Terminal Name	Zin	DC Voltage	Equivalent Circuit	Description
64	BIAS	—	0.28 V		Dolby NR reference current input
14	IREF	—	1.2 V		EQ reference current input
27	MF				EQ parameter current input
26	fQ				
25	f/Q				
24	GH				
23	GL				
22	GP				
35	BIAS ADJ (N)	—	1.2 V		Bias DAC parameter current input
36	BIAS ADJ (M)				
37	BIAS ADJ (C)				
21	HM	—	—		EQ parameter selector
20	HC				
19	HN				
18	NM				
17	NC				
16	NN				

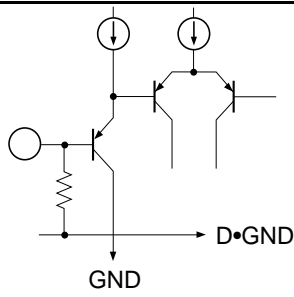
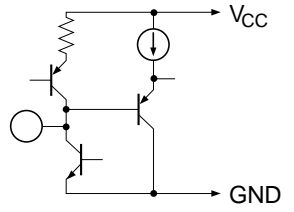
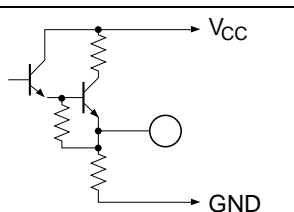
HA12167FB/HA12169FB

Pin Description ($V_{CC} = 14\text{ V}$, $T_a = 25^\circ\text{C}$, No signal, The value in the show typical value.)
(Cont)

Pin No. (QFP-80)	Terminal Name	Zin	DC Voltage	Equivalent Circuit	Description
68	CONT	3.3 k Ω	$V_{CC}/2 - 1.5\text{ V}$ to $V_{CC}/2$		DAC output volume control input
73					
13	EQ CONT	1.65 k Ω			
48					
10	LM DET	—	0.2 V		Time constant pin for level meter
51					
11	LM OUT	—	0.2 V		Level meter output
50					
45	NR ON/OFF	100 k Ω	—		Mode control time constant
44	C/B				
43	MPX				

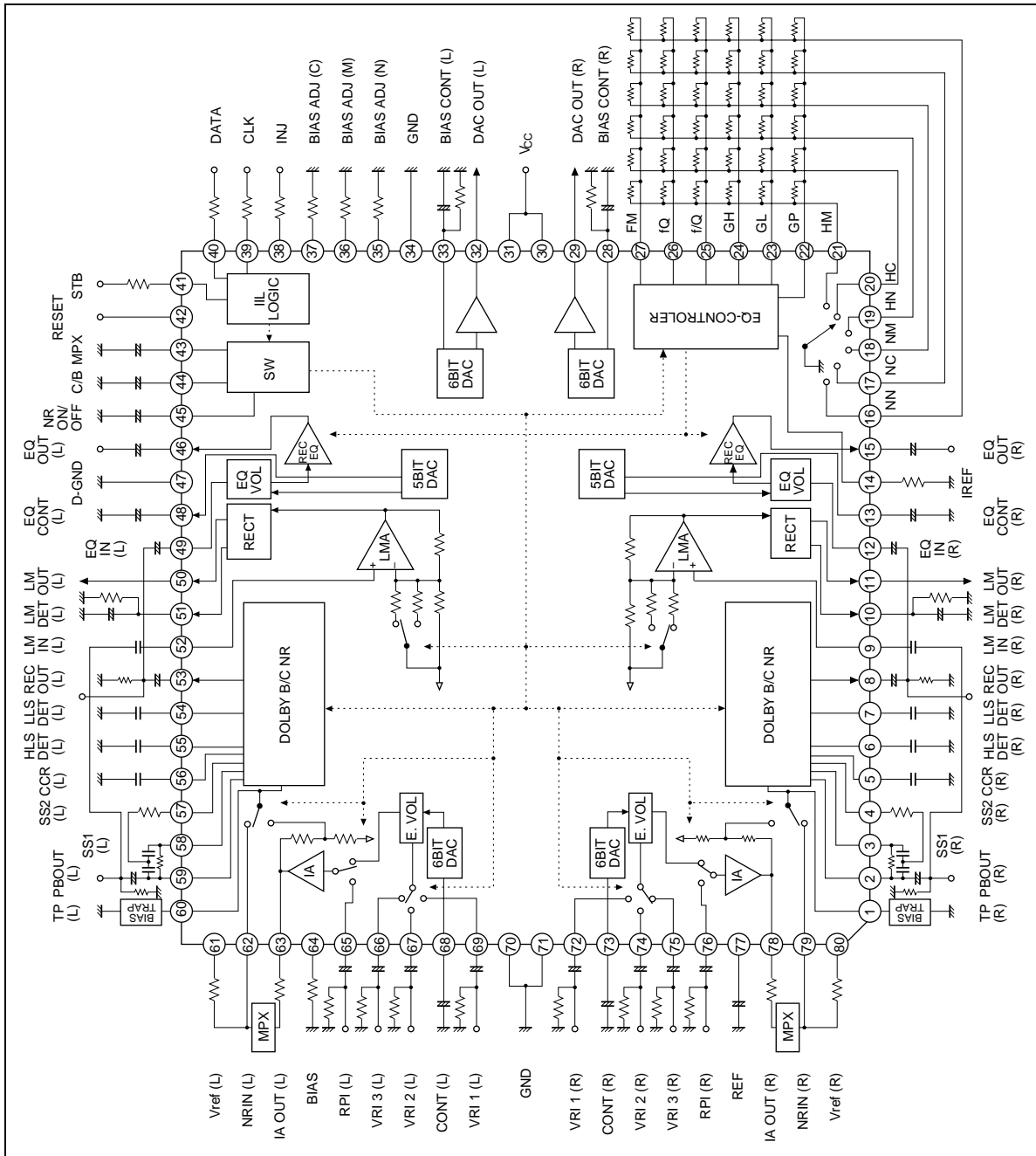
HA12167FB/HA12169FB

Pin Description ($V_{CC} = 14\text{ V}$, $T_a = 25^\circ\text{C}$, No signal, The value in the show typical value.)
(Cont)

Pin No. (QFP-80)	Terminal Name	Zin	DC Voltage	Equivalent Circuit	Description
42	RESET	100 k Ω	—		Mode control input
41	STB				
40	DATA				
39	CLK				
38	INJ	—	0.7 V	—	Injection current input I^2L
47	D-GND	—	0.0 V	—	Digital (Logic) ground
70	GND	—	0.0 V	—	Ground
71, 34					
28	BIAS CONT	—	—		Bias DAC output
33					
29	DAC OUT	—	—		Bias DAC buffer out
32					

HA12167FB/HA12169FB

Block Diagram

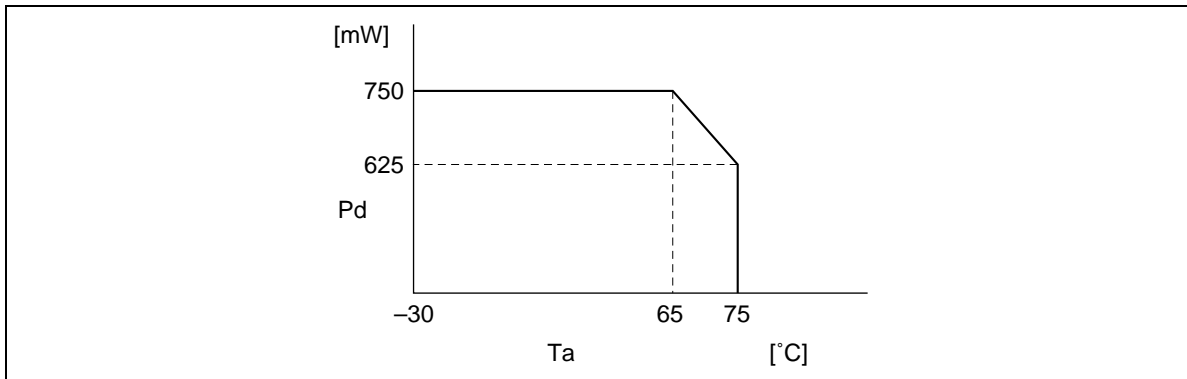


Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Note
Supply voltage	V_{cc} max	15	V	
Power dissipation	Pd	750	mW	1
Operating temperature	Topr	-30 to +75	°C	
Storage temperature	Tstg	-55 to +125	°C	

Note: For T_a is higher than 65°C, reduce Pd at the rate of 12.5 mW/°C.

Please, see the below graph.



Electrical Characteristics (Ta = 25°C, V_{cc} = 14 V, Dolby Level 300 mVrms at RECOU) (Cont)

Item	Test Conditions											Application Terminal									
	Specification											Input				Output					
	Symbol	Min	Typ	Max	Unit	REC /PB	RV /PV	MPX /NR	B/C	Input Meter	Tape Speed	Input Pin	Input EQ DAC	Bias fin	REC OUT Level	R	L	R	L	Note	
Serial digital input level	V _{3H}	4.0	—	5.3	V	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLK, DATA, STB	39
	V _{3L}	-0.2	—	1.0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	40
PB-output level	V _{out}	500	580	670	mVrms	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	—	—	High	76
		665	775	900	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Low	65
PB-out of fset	V _{ofs}	-100	0.0	+100	mV	PB	PV	OFF	OFF	C	RPI	NOR	NOR	NOR	63	0	0	—	—	No signal	—
																					2
Channel balance	ΔGv	-1.0	0.0	1.0	dB	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	76
REC volume gain	G _{rec VR (Max)}	17.5	19.1	21.5	dB	REC	RV	ON	OFF	B	VR11	NOR	NOR	NOR	0	0	0	1	k	V _{in} = 100 mVrms	72
	G _{rec VR (Min)}	-56.0	-50.0	-47.0	dB	REC	RV	ON	OFF	B	VR11	NOR	NOR	NOR	62	0	0	1	k	V _{in} = 2 Vrms	72
PB volume gain	G _{VR PB (Max)}	27.0	29.0	31.0	dB	PB	PV	ON	OFF	B	VR11	NOR	NOR	NOR	0	0	0	1	k	V _{in} = 100 mVrms	72
	G _{VR PB (Min)}	15.0	17.0	19.0	dB	PB	PV	ON	OFF	B	VR11	NOR	NOR	NOR	62	0	0	1	k	V _{in} = 100 mVrms	72
REC volume mute level	C _{Rec VR (MUT)}	—	-82	-75	dB	REC	RV	ON	OFF	B	VR11	NOR	NOR	NOR	63	0	0	1	k	V _{in} = 2 Vrms	72
REC volume input level	V _{in max (VR)}	11.0	12.0	—	dB	REC	RV	ON	OFF	B	VR11	NOR	NOR	NOR	42	0	0	1	k	THD = 1%	72
Signal to noise ratio of REC volume	S/N (VR)	78.0	84.0	—	dB	REC	RV	ON	OFF	B	VR11	NOR	NOR	NOR	—	0	0	(1	k)	V _{in} = 100 mVrms	72
																				Rg = 5.1 k, A-WTG	69
T.H.D. of REC volume	THD (VR)	—	0.04	0.3	%	REC	RV	ON	OFF	B	VR11	NOR	NOR	NOR	—	0	0	1	k	V _{in} = 100 mVrms	72
																					69

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Electrical Characteristics (Ta = 25°C, V_{CC} = 14 V, Dolby Level 300 mVrms at RECOU) (Cont)

Item	Specification										Test Conditions										Application Terminal				
	Symbol		Min	Typ	Max	Unit	REC	RV	/PB	/PV	MPX	NR	B/C	Input	Tape	Input	EQ	Bias	REC	REC	Input		Output		Note
	Min	Max	Unit	REC	RV	/PB	/PV	MPX	NR	B/C	Input	Meter	Speed	Tape	Pin	DAC	DAC	DAC	OUT	Level	R	L	R	L	
Equalizer gain	G _v EQ	23.5	25.5	27.5	dB	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	500	—	V _{in} = -32 dBs	12	49	15	46	
	G _v EQ	23.5	25.5	27.5		REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	1 k	—	V _{in} = -32 dBs	12	49	15	46	
	G _v EQ	25.0	27.0	29.0		REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	5 k	—	V _{in} = -32 dBs	12	49	15	46	
	G _v EQ	31.0	33.5	36.0		REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	12 k	—	V _{in} = -32 dBs	12	49	15	46	
Equalizer volume variable a range	ΔG _v EQ	6	8	10	dB	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0/30	0	1 k	—	V _{in} = -32 dBs	12	49	15	46	
	V _{in} Max (EQ)	-10.0	-9.0	—	dBs	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	16	0	1 k	—	THD = 1%	12	49	15	46	
Equalizer volume mute gain	G _v EQ	—	-75	-62	dB	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	31	0	1 k	—	V _{in} = -9 dBs 1 kHz BPF	12	49	15	46	
	SIN (EQ)	57.0	62.0	—	dB	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	—	—	R _g = 5.1 kΩ, A-WTG	12	49	15	46	
THD of equalizer	THD (EQ)	—	0.2	0.5	%	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	16	0	1 k	—	V _{in} = -26 dBs	12	49	15	46	
Equalizer of fset	V _{ofs} (EQ)	-400	0.0	+400	mV	REC	RV	OFF	OFF	B	RPI	NOR	NOR	NOR	63	0	0	—	—	No signal	—	—	15	46	4
Level meter output	LM	2.50	2.75	3.00	V	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	1 k	0	—	9	52	11	50	
	LM	3.55	3.85	4.15	V	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	1 k	12	—	9	52	11	50	
LM	0.70	1.00	1.30	V	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	1 k	-20	—	9	52	11	50		
	(-20 dB) ¹																								
LM	2.45	2.75	3.05	V	REC	RV	ON	OFF	B	RPI	20 dB	NOR	NOR	63	0	0	1 k	-20	—	9	52	11	50		
	(-20 dB) ²																								

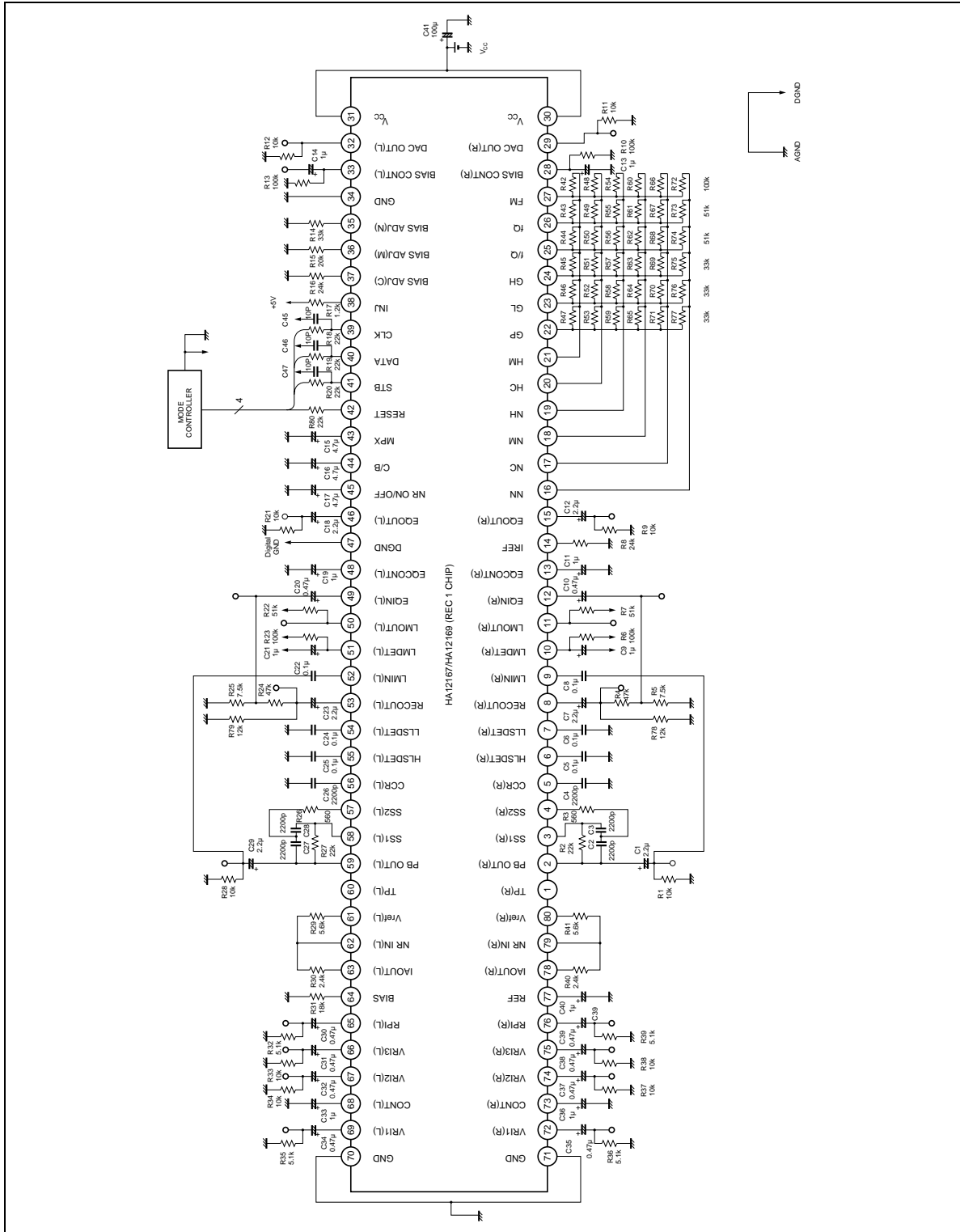
Electrical Characteristics (Ta = 25°C, V_{cc} = 14 V, Dolby Level 300 mVrms at RECOU) (Cont)

Item	Specification										Test Conditions										Application Terminal				
	Symbol		Min	Typ	Max	Unit	REC	RV	MPX	NR	B/C	Input	Meter	Speed	Tape	Input	EQ	Bias	fin	REC	Input		Output		Note
	Min	Max	Min	Max	Unit	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	DAC	DAC	DAC	Hz	OUT	R	L	R	L		
Level meter of fset	LMoIs 1	—	150	300	mV	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	—	—	No signal	—	—	11	50	
	LMoIs 2	—	200	350		REC	RV	ON	OFF	B	RPI	20 dB	NOR	NOR	63	0	0	—	—	No signal	—	—	11	50	
DAC output Max	V _o Max	11.0	12.0	13.0	V	REC	RV	OFF	OFF	B	VR11	NOR	NOR	MET	63	0	63	—	—	—	—	—	29	32	
DAC output Min	V _o Min	—	0.5	1.0	V	REC	RV	OFF	OFF	B	VR11	NOR	NOR	MET	63	0	0	—	—	—	—	—	29	32	

Note: 1. HA12167: V_{cc}=12 V
 HA12169: V_{cc}=11 V
 2. V_{cc}=15 V
 3. Adjust the input volume to Dolby level.
 4. V_{cc}=15 V

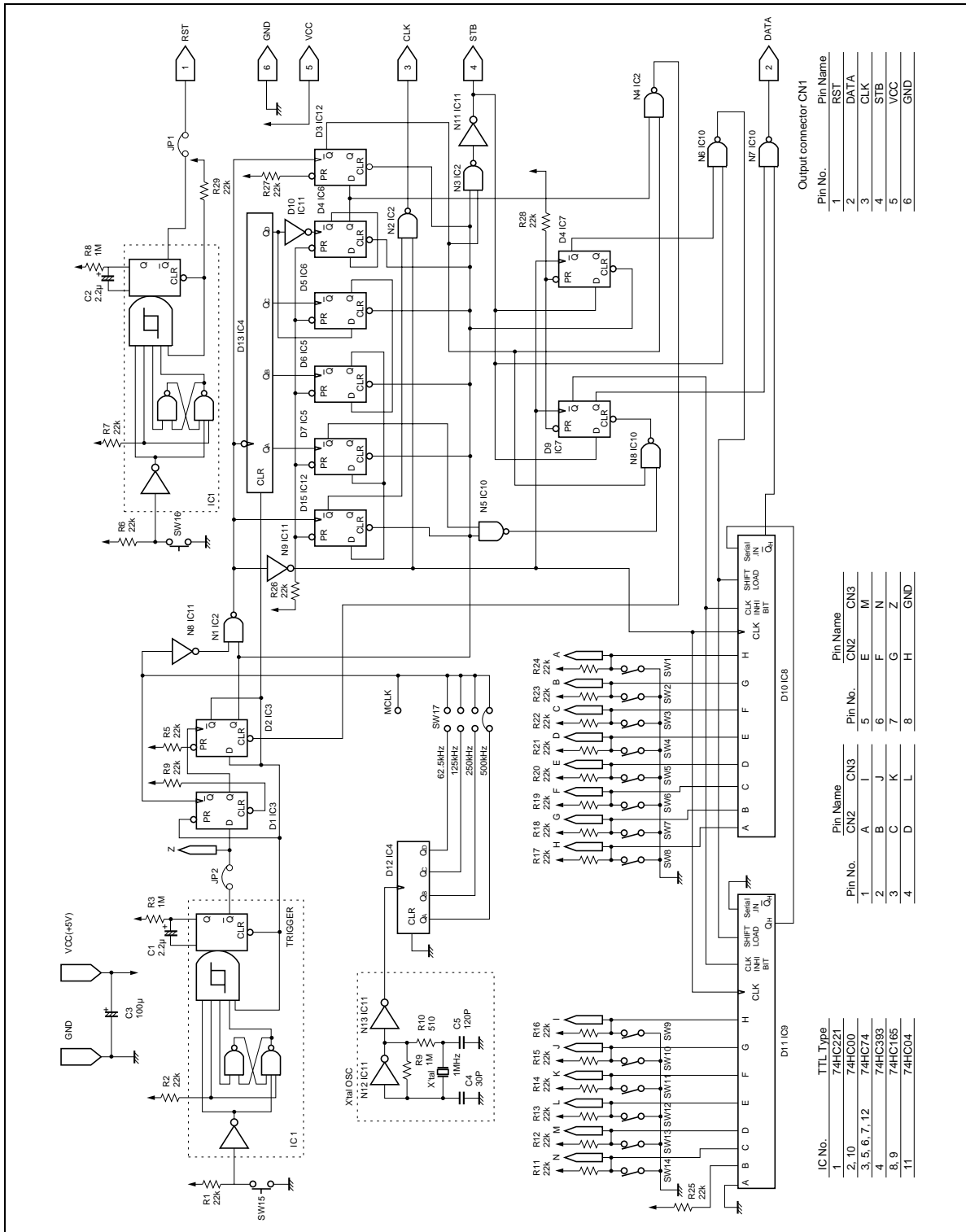
HA12167FB/HA12169FB

Test Circuit



HA12167FB/HA12169FB

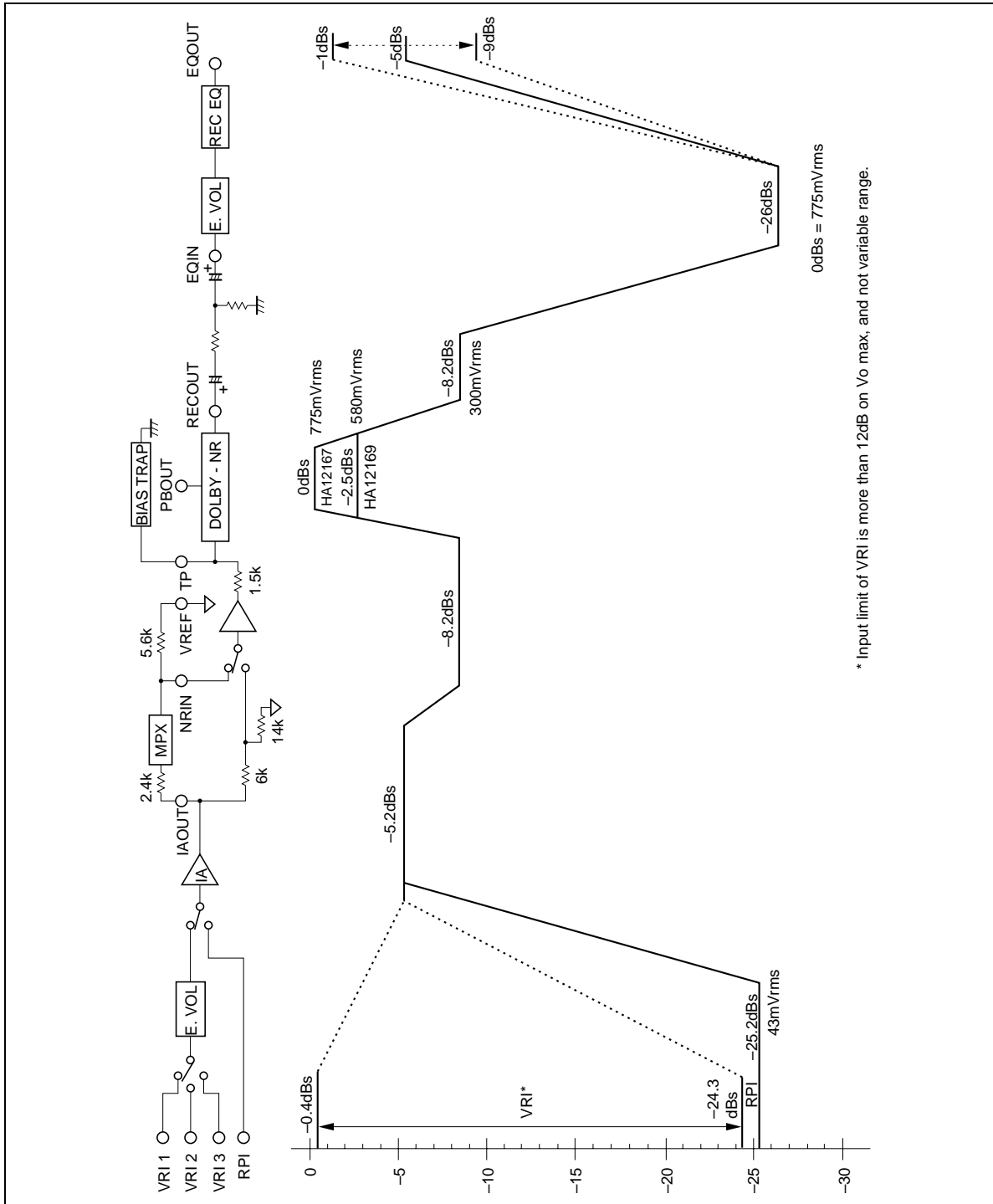
Mode Controller



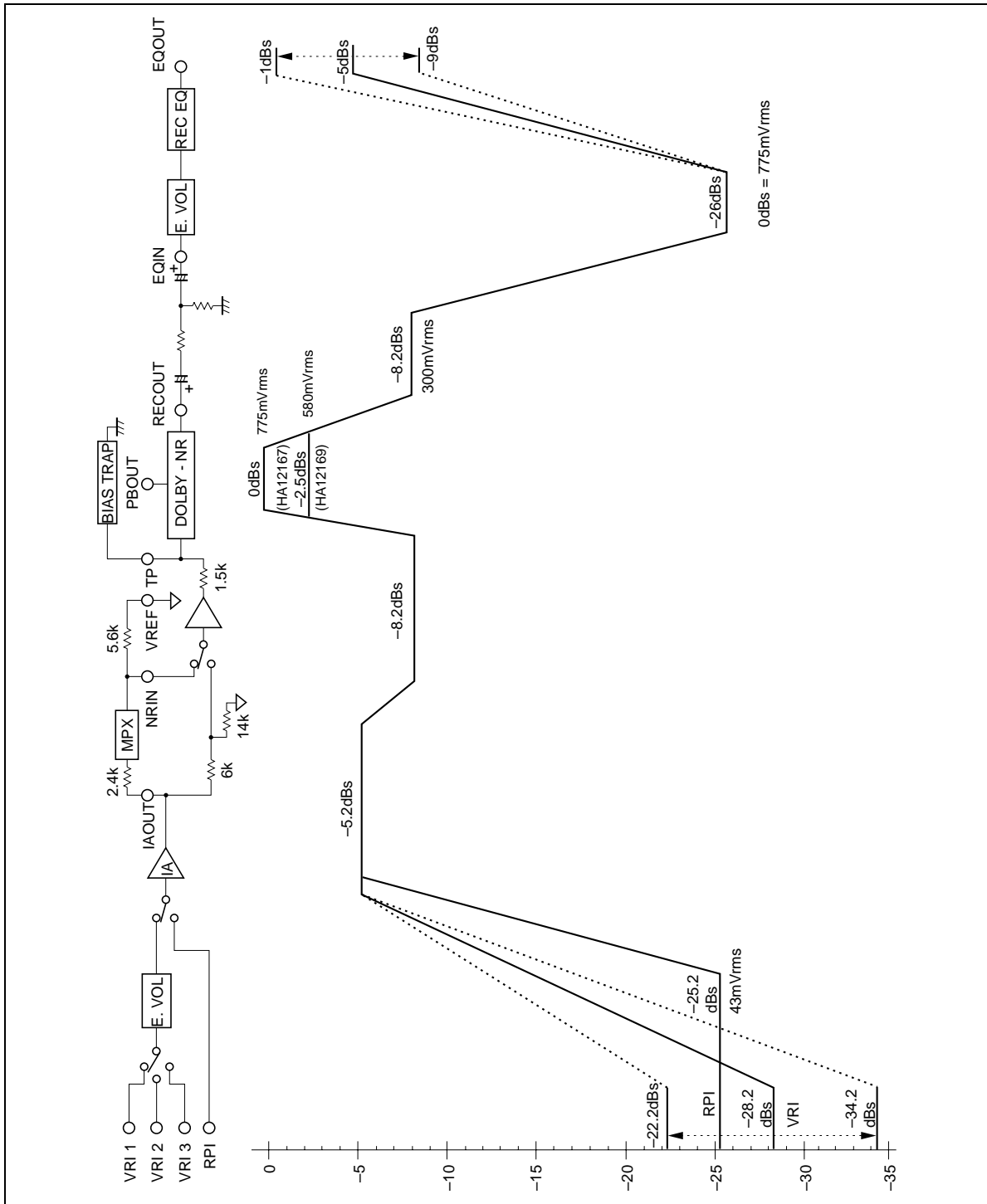
HA12167FB/HA12169FB

Level Diagram

REC Mode (1 kHz NR-OFF)



PB Mode (1 kHz NR-OFF)



HA12167FB/HA12169FB

Application Note

Power Supply Range

HA12167FB/HA12169FB are designed to operate on either single supply or split supply.

The operating range of the supply voltage is shown in table 1.

Table 1 Supply Voltage

Type No.	Single Supply	Split Supply
HA12167FB	12 V to 15 V	± 6.0 V to 7.5 V
HA12169FB	11 V to 15 V	± 6.0 V to 7.5 V

The lower limit of supply voltage depends on the line output reference level.

The minimum value of the overload margin is specified as 12 dB by Dolby Laboratories. HA12167 series are provided with two line output level, which will permit an optimum overload margin for power supply conditions.

Reference Voltage

For the single supply operation these devices provide the reference voltage of half the supply voltage that is the signal grounds. As the peculiarity of these devices, the capacitor for the ripple filter is very small about 1/100 compared with their usual value. The Reference voltage are provided for the left channel and the right channel separately. The block diagram is shown as figure 1.

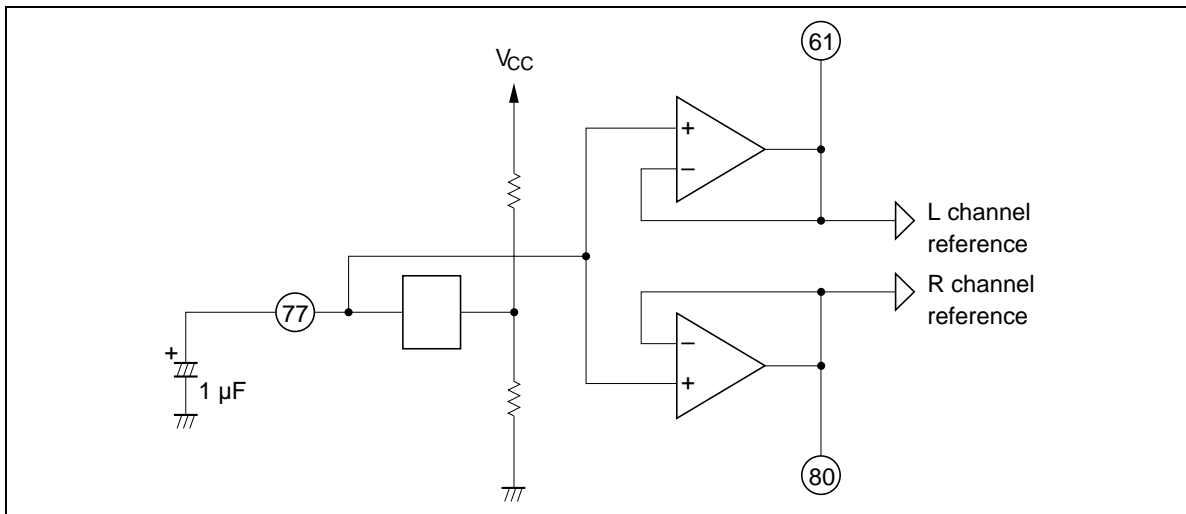


Figure 1 The Block Diagram of Reference Voltage Supply

Operating Mode Control

HA12167FB/HA12169FB provides fully electronic switching circuits. All switches are controlled by serial data.

Table 2 Threshold Voltage (VTH)

Pin No.	Lo	Hi	Unit
42	-0.2 to 1.5	3.5 to 5.3	V
39, 40, 41	-0.2 to 1.0	4.0 to 5.3	V

- Notes:
1. Voltages shown above are determined by internal circuits of LSI when take pin 47 (DGND pin) as reference pin. On split supply use, same VTH can be offered by connecting DGND pin to GND pin.
This means that it can be controlled directly by micro processor.
 2. Each pins are on pulled down with 100 kΩ internal resistor.
Therefore, it will be low-level when each pins are open.
 3. Note on serial data inputting
 - (a) The clock frequency on CLK must be less than 500 kHz.
 - (b) Over shoot level and under shoot level of input signal must be the value shown below.

When connecting microcomputer or Logic-IC with HA12167FB/HA12169FB directly, there is apprehension of rash-current under some transition timing of raising voltage or falling voltage at V_{CC} ON/OFF.

For this countermeasure, connect 10 kΩ to 20 kΩ resistor with each pins. It is shown in test circuit on this data sheet.

In case of changing NR-ON/OFF at the C-mode, for the countermeasure of the noise of pop, perform the following processes.

In case of changing NR-OFF to NR-ON at C-mode. C-mode, NR-OFF → B-mode, NR-OFF → B-mode, NR-ON → C-mode, NR-ON.

In case of changing NR-ON to NR-OFF at C-mode. C-mode, NR-ON → B-mode, NR-ON → B-mode, NR-OFF → C-mode, NR-OFF.

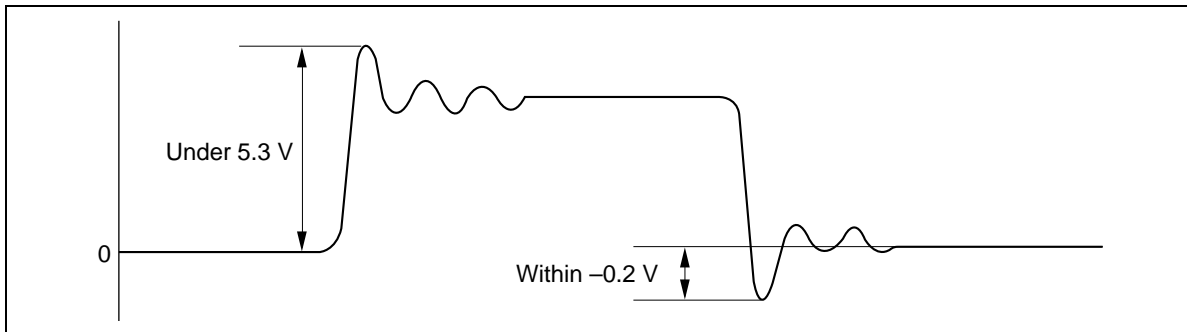


Figure 2 Input Level

HA12167FB/HA12169FB

Serial Data Formatting

14 bit shift register is employed.

CLK and data are stored during STB being high and data is latched when STB goes high to low.

Reset goes reset a state when reset low and high releases reset. (High fixed at use time)

Attention Point of Serial Interface

- Reset goes low condition when a power supply is ON or OFF.
- Characteristics select of Bias DAC is connected with equalizer tape selector.
- Bias DAC register is all low when a time of tape select.
- Bias DAC register is all low and Bias DAC out is dropped low level at compulsion by force.
- Input pin select, REC/PB select and Input volume gain select does not select at the same time.
- Input volume must go mute condition when selected of RPI is input pin select.

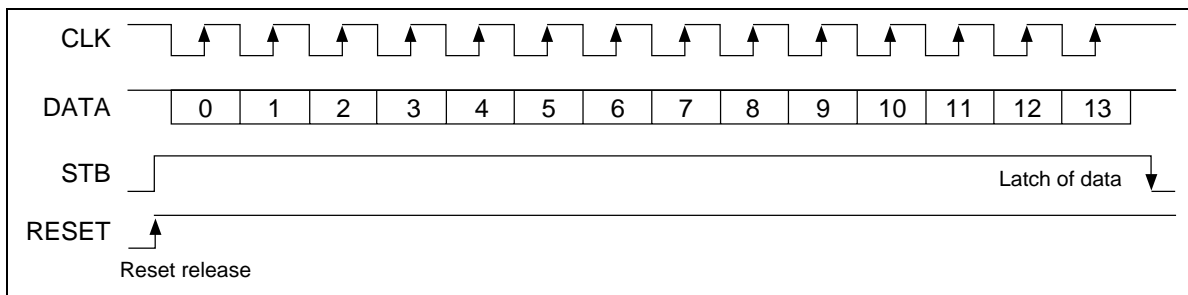


Figure 3 Serial Data Timming Chart Figure

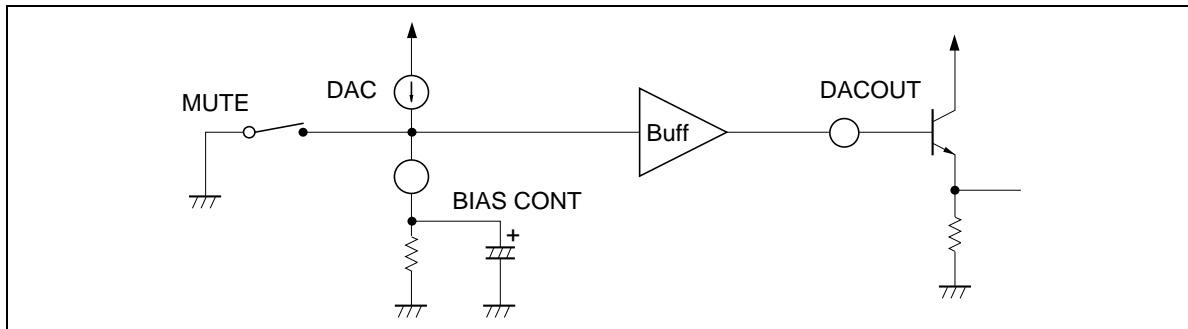


Figure 4 Bias DAC Output Circuit

Serial Data Formatting

Bit No.	Mode Control	Input Voltage		Equalizer Voltage		Basic DAC														
		Reset	Reset	Reset	Reset															
0	Tape selector 1 <table border="1" style="margin-left: 20px;"> <tr><td>bit 0</td><td>_____</td><td>L</td></tr> <tr><td>bit 1</td><td>H _____ L</td><td></td></tr> <tr><td>H</td><td>Metal Normal</td><td></td></tr> <tr><td>L</td><td>Crom Normal</td><td></td></tr> </table>	bit 0	_____	L	bit 1	H _____ L		H	Metal Normal		L	Crom Normal		L	L channel	I-bit 0 L	L channel	E-bit 0 L	L channel	B-bit 0 L
bit 0	_____	L																		
bit 1	H _____ L																			
H	Metal Normal																			
L	Crom Normal																			
1	Tape selector 2	L		I-bit 1 L		E-bit 1 L		B-bit 1 L												
2	Tape speed <table border="1" style="margin-left: 20px;"> <tr><td>H</td><td>Hi speed selection</td><td>L</td></tr> <tr><td>L</td><td>Normal speed selection</td><td></td></tr> </table>	H	Hi speed selection	L	L	Normal speed selection		L		I-bit 2 L		E-bit 2 L		B-bit 2 L						
H	Hi speed selection	L																		
L	Normal speed selection																			
3	Meter sensitivity <table border="1" style="margin-left: 20px;"> <tr><td>H</td><td>Meter sensitivity 20 dB up</td><td>L</td></tr> <tr><td>L</td><td>Meter sensitivity normal</td><td></td></tr> </table>	H	Meter sensitivity 20 dB up	L	L	Meter sensitivity normal		L		I-bit 3 L		E-bit 3 L		B-bit 3 L						
H	Meter sensitivity 20 dB up	L																		
L	Meter sensitivity normal																			
4	Input selector 1 <table border="1" style="margin-left: 20px;"> <tr><td>bit 4</td><td>_____</td><td>L</td></tr> <tr><td>bit 5</td><td>H _____ L</td><td></td></tr> <tr><td>H</td><td>VRI3 RPI</td><td></td></tr> <tr><td>L</td><td>VRI2 VRI1</td><td></td></tr> </table>	bit 4	_____	L	bit 5	H _____ L		H	VRI3 RPI		L	VRI2 VRI1		L		I-bit 4 L		E-bit 4 L		B-bit 4 L
bit 4	_____	L																		
bit 5	H _____ L																			
H	VRI3 RPI																			
L	VRI2 VRI1																			
5	Input selector 2	L		I-bit 5 H		— —		B-bit 5 L												
6	REC/PB <table border="1" style="margin-left: 20px;"> <tr><td>H</td><td>PB mode selection</td><td>H</td></tr> <tr><td>L</td><td>REC mode selection</td><td></td></tr> </table>	H	PB mode selection	H	L	REC mode selection		H	R channel	I-bit 0 L	R channel	E-bit 0 L	R channel	B-bit 0						
H	PB mode selection	H																		
L	REC mode selection																			
7	Input voltage gain <table border="1" style="margin-left: 20px;"> <tr><td>H</td><td>PB mode volume gain</td><td>H</td></tr> <tr><td>L</td><td>Rec mode volume gain</td><td></td></tr> </table>	H	PB mode volume gain	H	L	Rec mode volume gain		H		I-bit 1 L		E-bit 1 L		B-bit 1 L						
H	PB mode volume gain	H																		
L	Rec mode volume gain																			
8	MPX <table border="1" style="margin-left: 20px;"> <tr><td>H</td><td>ON</td><td>L</td></tr> <tr><td>L</td><td>OFF</td><td></td></tr> </table>	H	ON	L	L	OFF		L		I-bit 2 L		E-bit 2 L		B-bit 2 L						
H	ON	L																		
L	OFF																			
9	NR <table border="1" style="margin-left: 20px;"> <tr><td>H</td><td>ON</td><td>L</td></tr> <tr><td>L</td><td>OFF</td><td></td></tr> </table>	H	ON	L	L	OFF		L		I-bit 3 L		E-bit 3 L		B-bit 3 L						
H	ON	L																		
L	OFF																			
10	B/C <table border="1" style="margin-left: 20px;"> <tr><td>H</td><td>C</td><td>L</td></tr> <tr><td>L</td><td>B</td><td></td></tr> </table>	H	C	L	L	B		L		I-bit 4 L		E-bit 4 L		B-bit 4 L						
H	C	L																		
L	B																			
11	—	—		I-bit 5 H		— —		B-bit 5 L												
12	Register selector 1 <table border="1" style="margin-left: 20px;"> <tr><td>bit 12</td><td>_____</td><td></td></tr> <tr><td>bit 13</td><td>H _____ L</td><td></td></tr> <tr><td>H</td><td>Bias DAC</td><td>Input volume</td></tr> <tr><td>L</td><td>Equalizer volume</td><td>Mode control</td></tr> </table>	bit 12	_____		bit 13	H _____ L		H	Bias DAC	Input volume	L	Equalizer volume	Mode control							
bit 12	_____																			
bit 13	H _____ L																			
H	Bias DAC	Input volume																		
L	Equalizer volume	Mode control																		
13	Register selector 2																			

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Input Volume Register

I-bit 5	I-bit 4	I-bit 3	I-bit 2	I-bit 1	I-bit 0	Gain
L	L	L	L	L	L	Increase
L	L	L	L	L	H	↑
L	L	L	L	H	L	:
L	L	L	L	H	H	:
:	:	:	:	:	:	:
:	:	:	:	:	:	↓
H	H	H	H	H	L	Decrease
H	H	H	H	H	H	Mute

Equalizer Volume Register

E-bit 4	E-bit 3	E-bit 2	E-bit 1	E-bit 0	Gain
L	L	L	L	L	Increase
L	L	L	L	H	↑
L	L	L	H	L	:
L	L	L	H	H	:
:	:	:	:	:	:
:	:	:	:	:	↓
H	H	H	H	L	Decrease
H	H	H	H	H	Mute

Bias DAC Register

B-bit 5	B-bit 4	B-bit 3	B-bit 2	B-bit 1	B-bit 0	Bias
L	L	L	L	L	L	Mute
L	L	L	L	L	H	Decrease
L	L	L	L	H	L	↑
L	L	L	L	H	H	:
:	:	:	:	:	:	:
:	:	:	:	:	:	:
H	H	H	H	H	L	↓
H	H	H	H	H	H	Increase

MPX ON/OFF Switch

MPX-OFF mode means that signal from input amp doesn't go through the MPX filter, but signal goes through the NR circuit after being attenuated 3 dB by internal resistor. Refer to figure 5. For not cause any level difference between MPX-ON mode and MPX-OFF mode, it is requested to use MPX-filter which has definitely 3 dB attenuated. And when applying other usage except figure 5,

take consideration to give bias voltage to NR-IN terminal by resistor or so on because internal of NR-IN terminal has no bias resistor.

Application as for the Dubbing Cassette Deck

HA12167FB/HA12169FB series has unprocessor signal from recording out terminals during playback mode. So, it is simply applied for dubbing cassette decks.

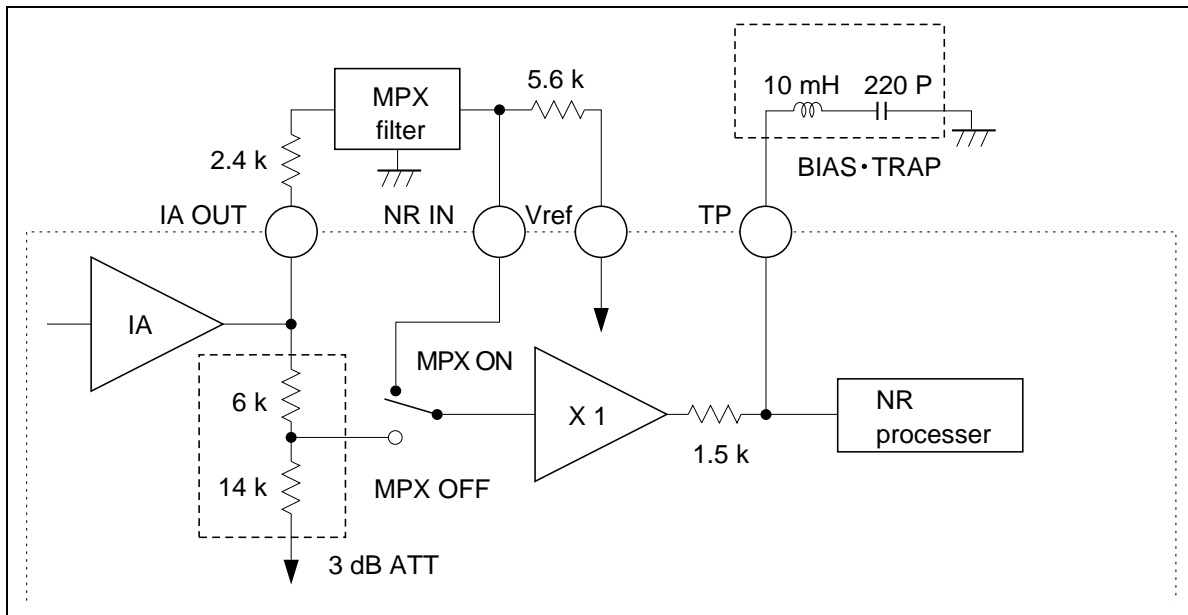


Figure 5 MPX ON/OFF Switch Block Diagram

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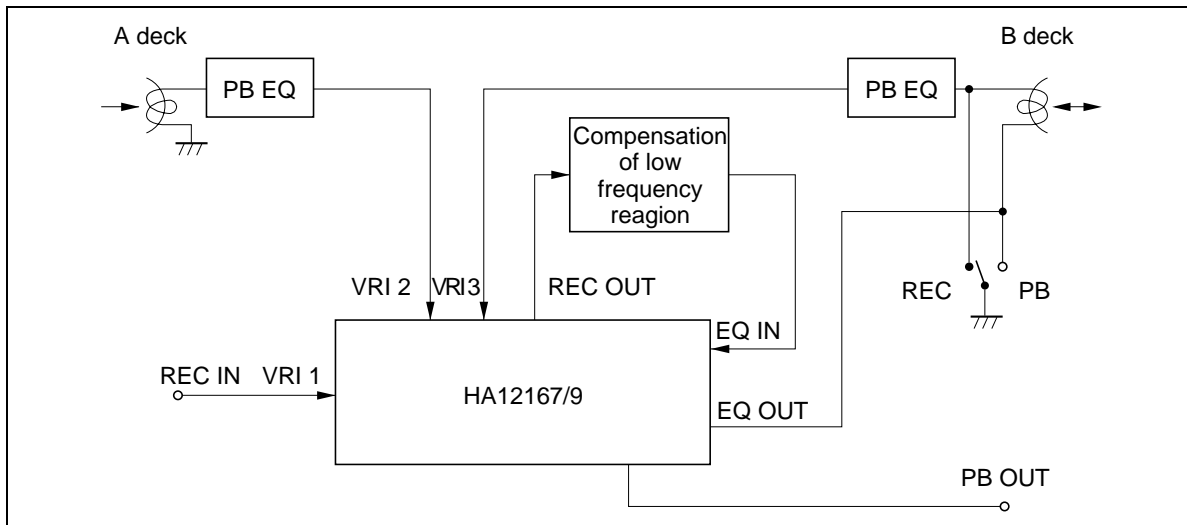


Figure 6 Application for Dubbing Deck

Injector Current

HA12167FB/HA12169FB has logic circuit which is fabricated by I^2L into IC. To operate this circuit, it is required enough injector current. Injector current goes into from the INJ pin (pin 38) and external resistor is required to connect to this pin for adequate current. The value of external resistor is obtained by using following equations. And put them with $\pm 10\%$ tolerance value which is calculated. V_{INJ} can allow to connect to V_{CC} shown below. Large injector current fear to cause mis-operation of Logic under the condition of high temperature. Also, small injector current fear to cause mis-operation (stop operation). Under the condition of low temperature. Therefore, pay attention to have good stability of V_{INJ} .

$$R_{INJ} = \frac{V_{INJ} - 0.7}{3.6} \text{ [k}\Omega\text{]} \quad \text{Single supply}$$

$$R_{INJ} = \frac{V_{INJ} + V_{EE} - 0.7}{3.6} \text{ [k}\Omega\text{]} \quad \text{Split supply}$$

Gain Control of Electronic Volume

HA12167FB/HA12169FB is designed in order to change the gain by DAC fabricated into IC. To reduce the click noise when changing volume gain instantaneously, required to connect the capacitor and resistor (CR time constant) to CONT pin (pin 13, 48, 68, 73). These terminals are also be used as output pin of DAC. Therefore, by forcing voltage and current to these terminals, it is applicable to control volume gain directly. But, voltage forced to these terminals must be from $V_{CC}/2 - 2 \text{ V}$ to $V_{CC}/2$ (for split supply use, -2 V to 0 V) in this case. And, this case, change of a gain depending on a temperature gets large.

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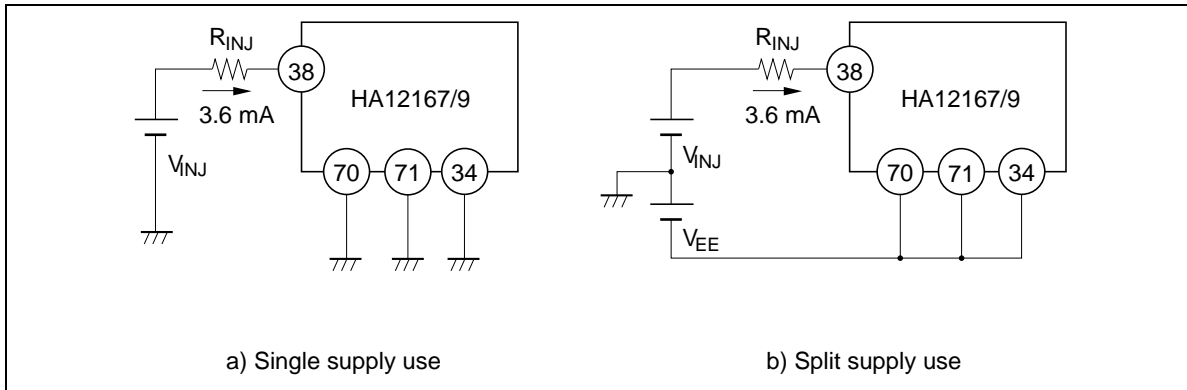


Figure 7 Injector Current Application

The Tolerances of External Components for Dolby NR-Block

For adequate Dolby NR tracking response, take external components shown below.

For C5, C6, C24, and C25, please employ a few object of the leak, though you can be useful for an electrolytic-capacitor.

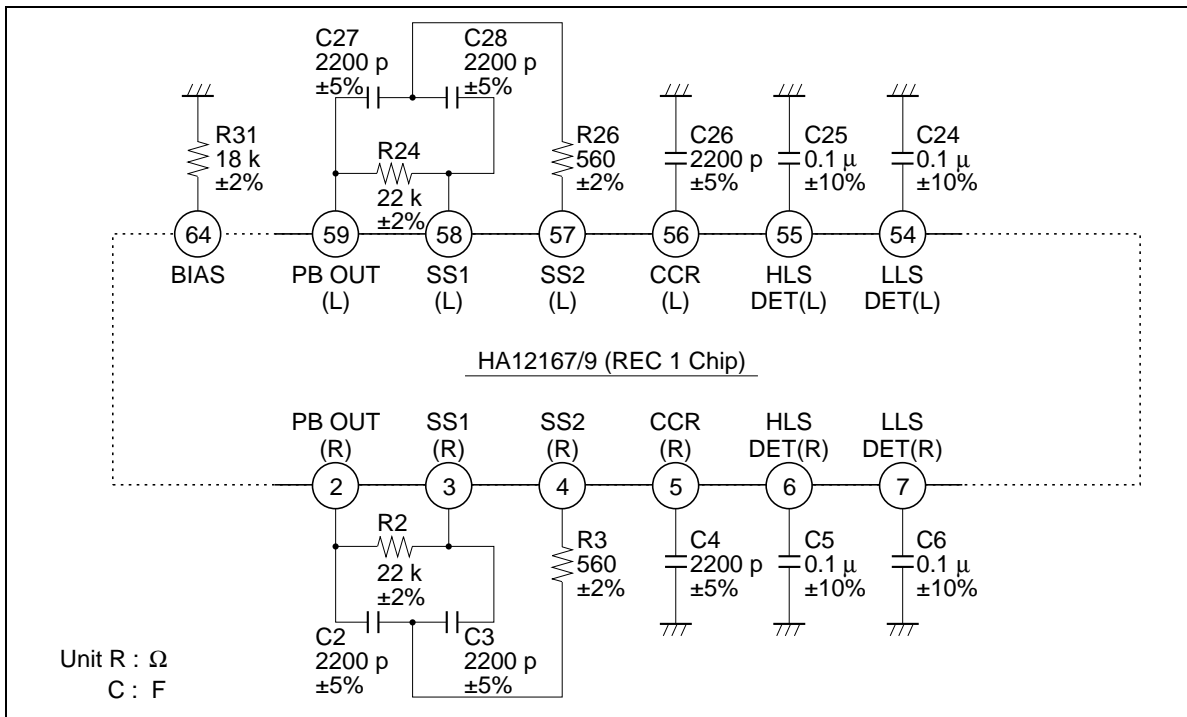


Figure 8 Tolerances of External Components

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BIAS DAC

The full-scale of DAC is computed by the formula mentioned below.

$$V_{29} = \frac{2.4}{R_{14 \text{ to } 16}} \times R_{10} \quad [\text{V}]$$

$$V_{32} = \frac{2.4}{R_{14 \text{ to } 16}} \times R_{13} \quad [\text{V}]$$

R₁₄: Normal Tape (pin 35)

R₁₅: Metal Tape (pin 36)

R₁₆: Chrome Tape (pin 37)

The maximum source current of DAC output (pin 29, 32) is 2 mA. Therefore the Bias-osc is driven through external transistor of emitter-follower.

Level Meter

The coupling capacitor of LMIN pin (9 pin and 52 pin).

For these capacitors, please employ a small object of the leak.

The Application of Equalizer Frequency Response

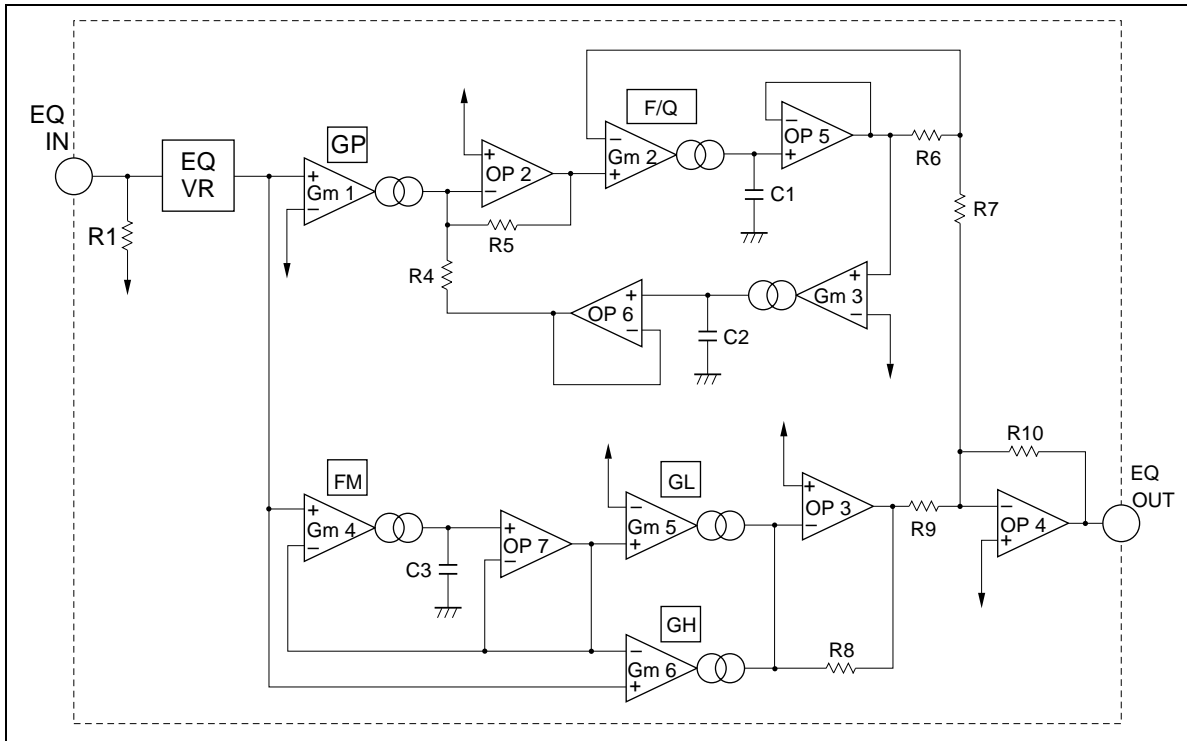


Figure 9 REC Equalizer Block Diagram

Transfer Function:

$$\frac{V_{out}}{V_{in}} = G_v \left(G_{m5} \cdot \frac{R_8 \cdot R_{10}}{R_9} \cdot \frac{1 + \frac{C_3}{G_{m4}} \cdot \frac{G_{m6}}{G_{m5}} \cdot S}{1 + \frac{C_3}{G_{m4}} \cdot S} + G_{m1} \cdot \frac{R_4 \cdot R_{10}}{R_6 + R_7} \cdot \frac{\frac{C_3}{G_{m4}} \cdot S}{1 + \frac{R_4}{R_5} \cdot \frac{R_7}{R_6 + R_7} \cdot \frac{C_2}{G_{m3}} \cdot S + \frac{R_4}{R_5} \cdot \frac{C_1}{G_{m2}} \cdot \frac{C_2}{G_{m3}} \cdot S^2} \right)$$

$$= \frac{9}{R_{REF}} \left(R_{GL} \cdot \frac{1 + 6.67 \times 10^{-10} \frac{R_{FM} \cdot R_{GH}}{R_{GL}} \cdot S}{1 + 6.67 \times 10^{-10} \frac{R_{GL}}{R_{FM}} \cdot S} + R_{GP} \cdot \frac{3.0 \times 10^{-10} \cdot R_{FQ} \cdot S}{1 + 4.5 \times 10^{-11} \cdot R_{FQ} \cdot S + 2.5 \times 10^{-20} \cdot R_{FQ} \cdot R_{F/Q} \cdot S^2} \right)$$

Note: R_{REF} 14 pin bias resistance
 G_v Gain of EQ-VR

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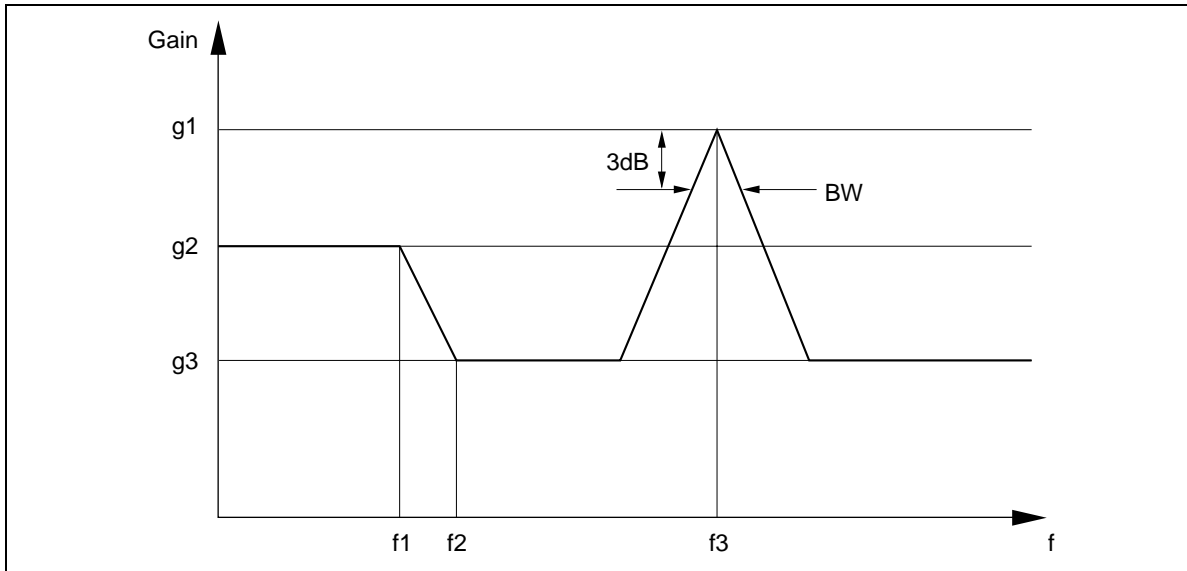


Figure 10 REC Equalizer Frequency Response

$$\left. \begin{aligned} g1 &= \frac{9}{R_{REF}} (6.67 \times R_{GP} + R_{GH}) \\ g2 &= \frac{9 \times R_{GL}}{R_{REF}} \\ g3 &= \frac{9 \times R_{GH}}{R_{REF}} \end{aligned} \right\} \text{when Gain of EQ - VR is center}$$

$$f1 = \frac{1}{2\pi \times 6.67 \times 10^{-10} \times R_{FM}}$$

$$f2 = \frac{R_{GL}}{2\pi \times 6.67 \times 10^{-10} \times R_{FM} \times R_{GH}}$$

$$f3 = \frac{1}{2\pi} \cdot \frac{0.3}{\sqrt{2.25 \times 10^{-21} \times R_{FQ} \times R_{F/Q}}}$$

$$BW = \frac{1}{4\pi \times 2.78 \times 10^{-10} \times R_{F/Q}}$$

$$Q = \frac{f3}{BW} = 3.51 \times \sqrt{\frac{R_{F/Q}}{R_{FQ}}}$$

Equalizer Characteristics Control Using a Bias DAC

When only one of the bias DAC channels is used, any one of the six parameters (FM, fQ, f/Q, GH, GL, and GP) that set the equalizer's characteristics can be controlled by the unused bias DAC.

The figure below gives one example.

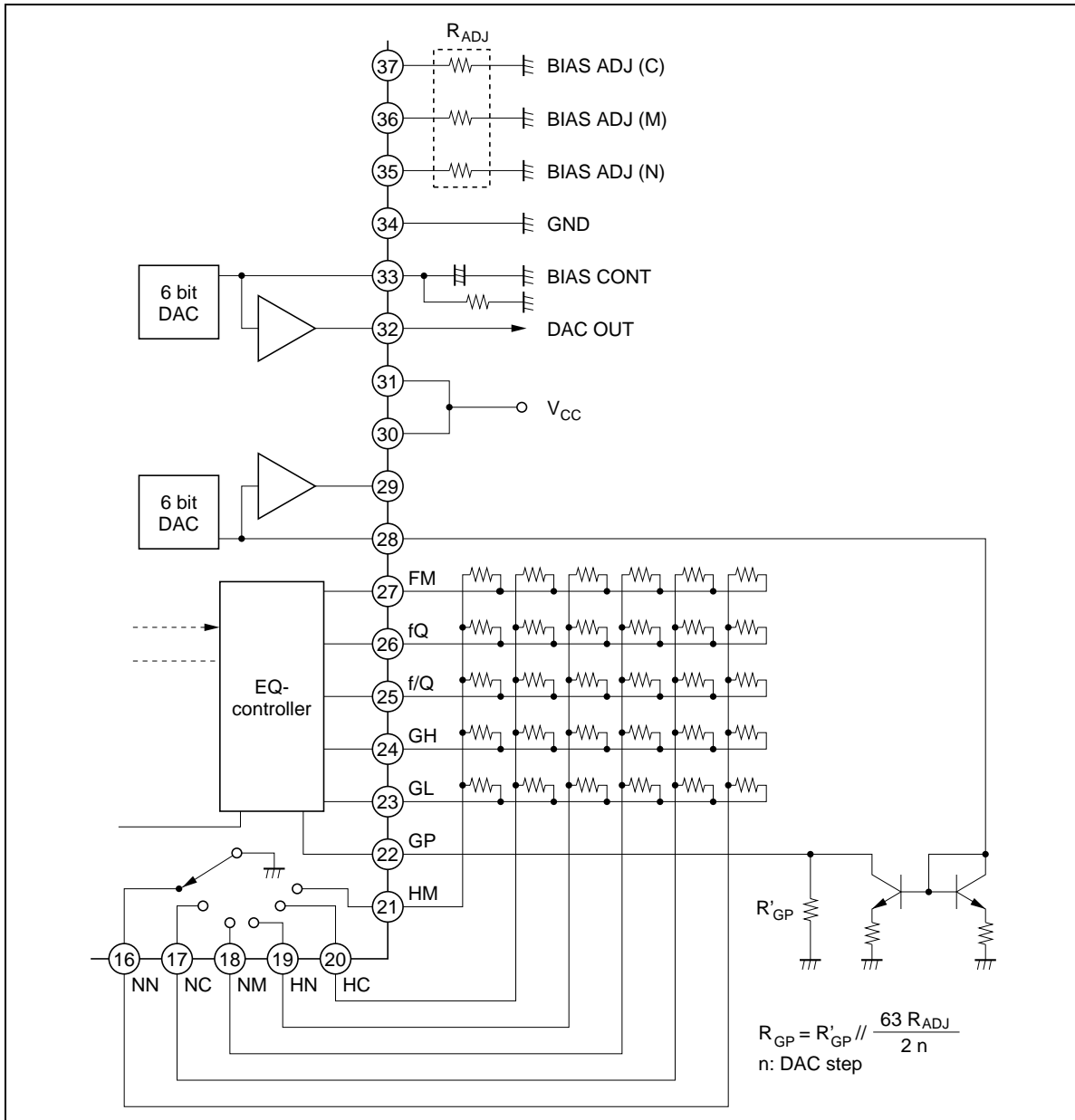


Figure 11 Bias DAC Control of the GP Parameter

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Figures 12, 13, and 14 show the characteristics when GP is controlled by a bias DAC.

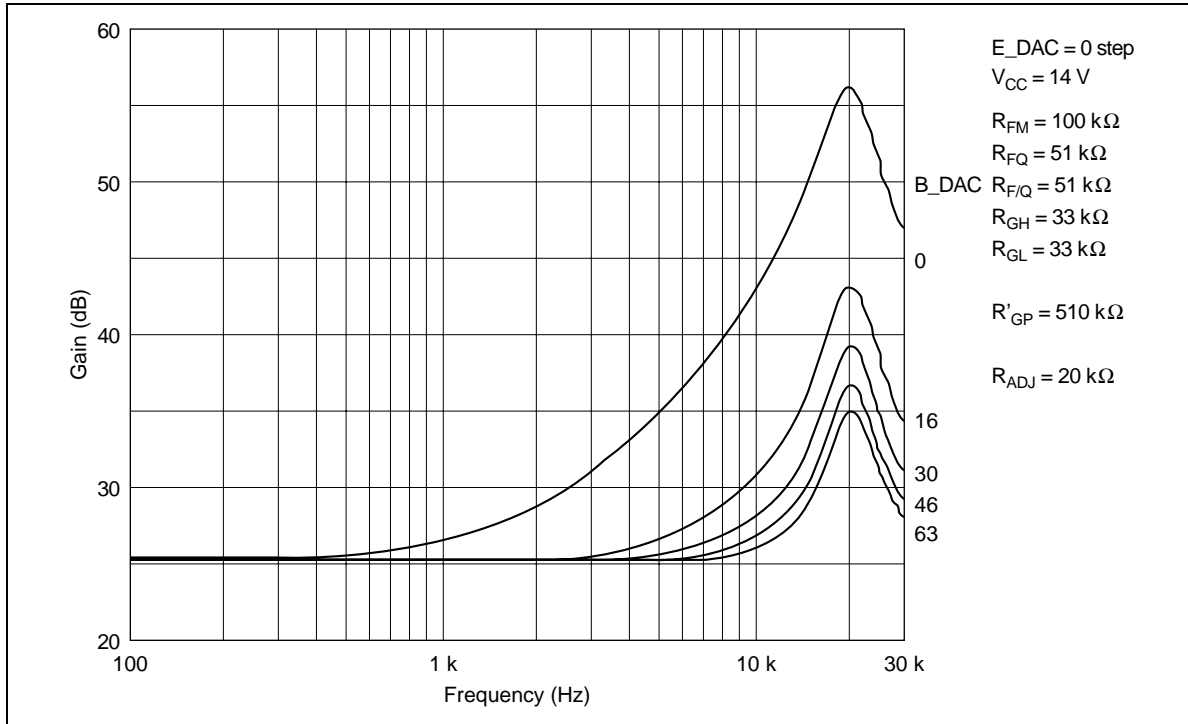


Figure 12 Equalizer Gain vs. Frequency

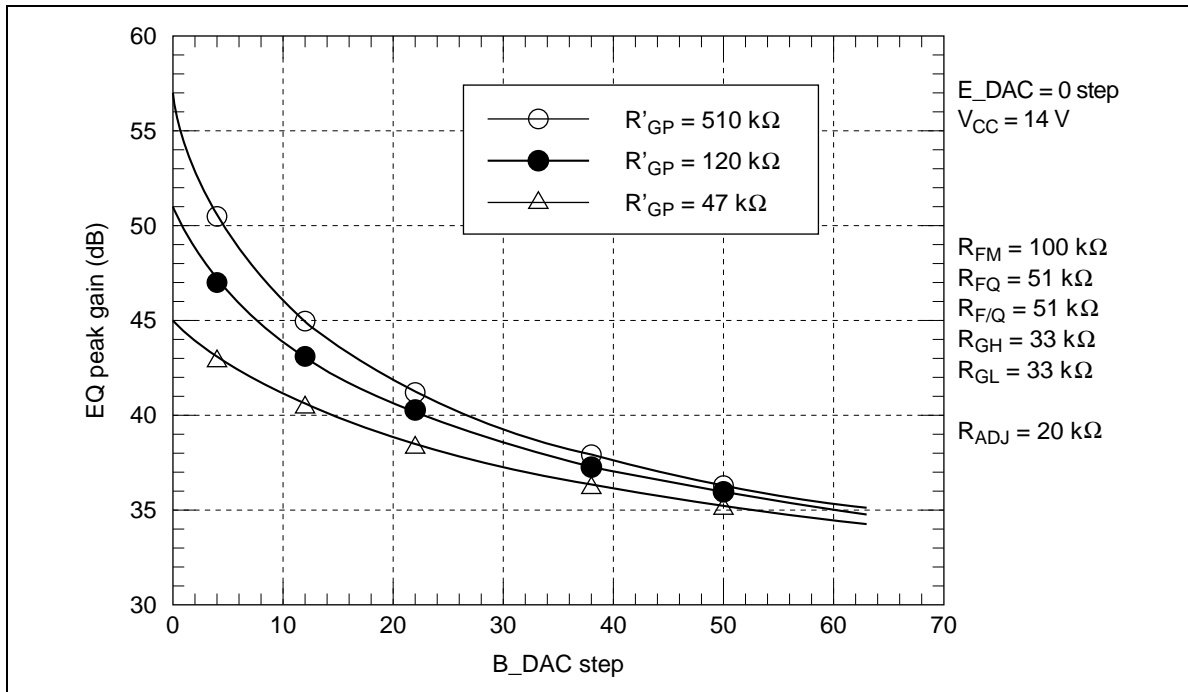


Figure 13 Equalizer Peak Gain vs. DAC Step Characteristics (1)

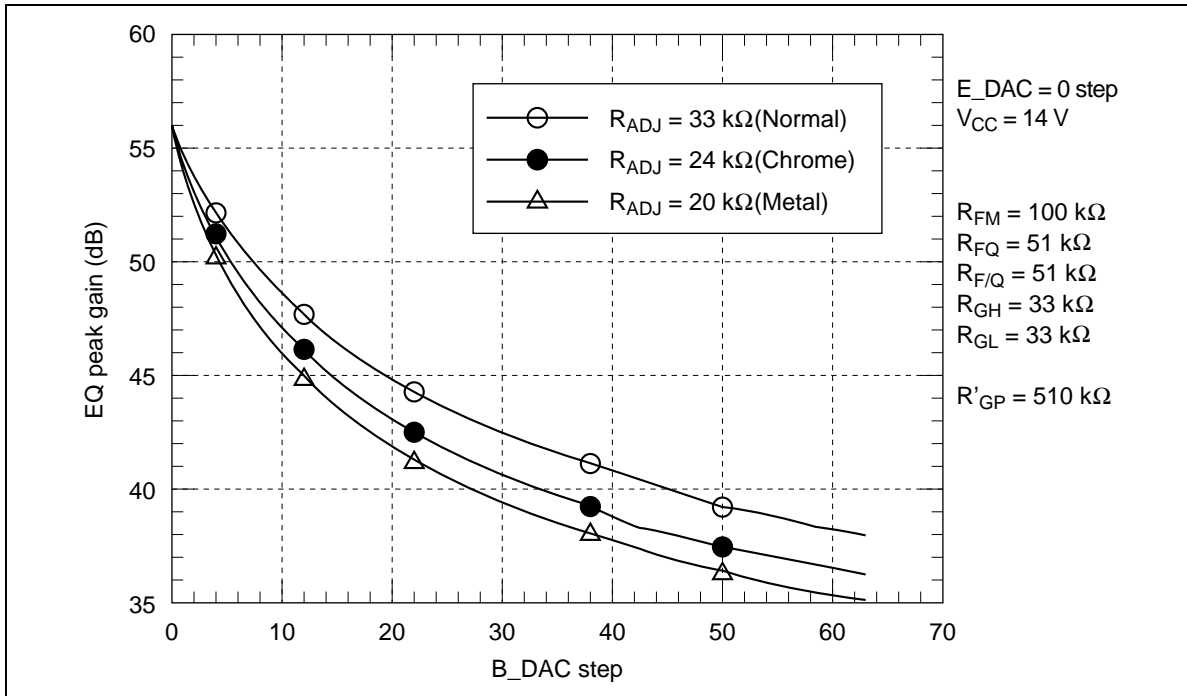


Figure 14 Equalizer Peak Gain vs. DAC Step Characteristics (2)

When the (variable) width of the DAC step is to be changed, the gain at step 0 or at step 63 must be changed. The step 0 gain can be changed using R'_{GP} as shown in figure 13. Also, R'_{GP} can be switched using the tape selector, as shown in figure 15. However, it is necessary to take into account that the value of R_{ADJ} , which sets the step 63 gain, is also used for the output bias. When the load resistance on pin 33 is R_L , the following formula gives the output bias, V_{BMAX} .

$$V_{BMAX} = 2.4 \times R_L / R_{ADJ}$$

Therefore, it is possible to compensate the output bias, V_{BMAX} for the R_{ADJ} setting by changing R_L .

Note: R_{ADJ} should be in the range 16 kΩ to 75 kΩ.

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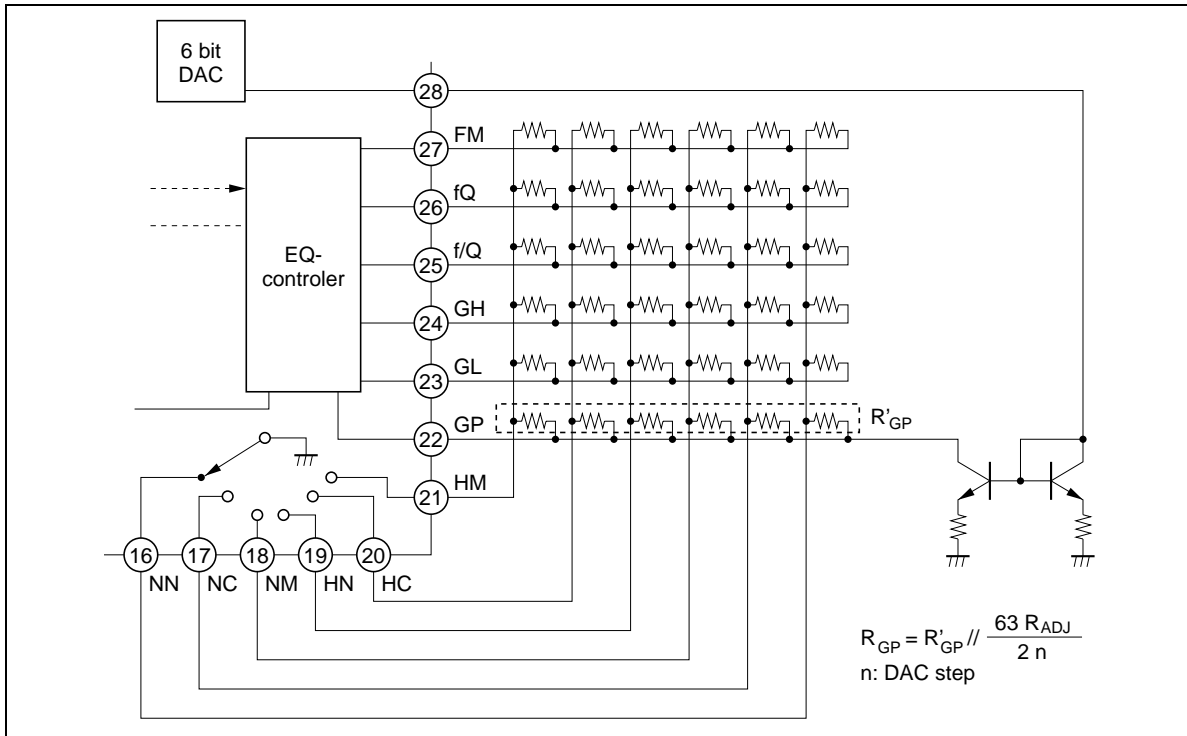
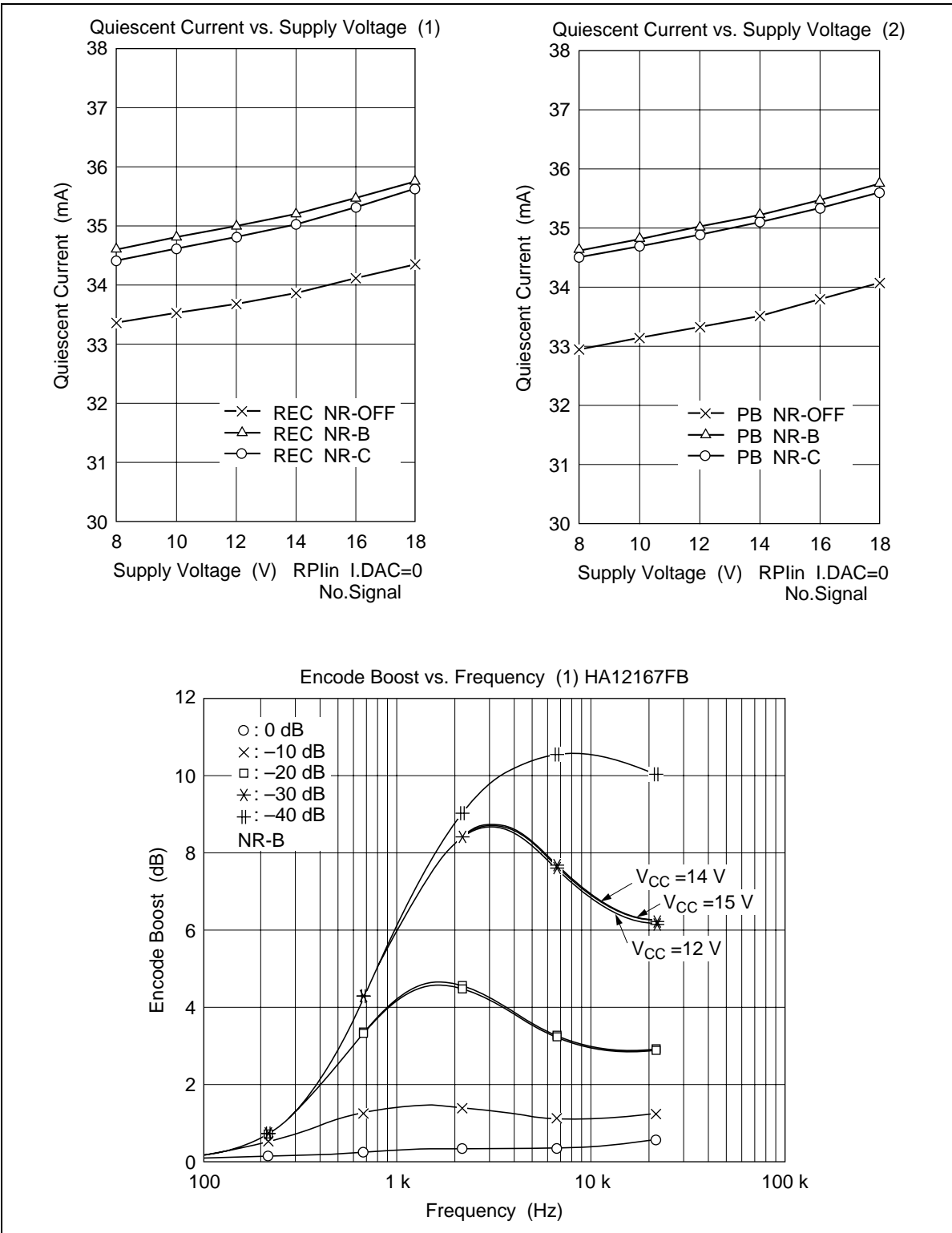
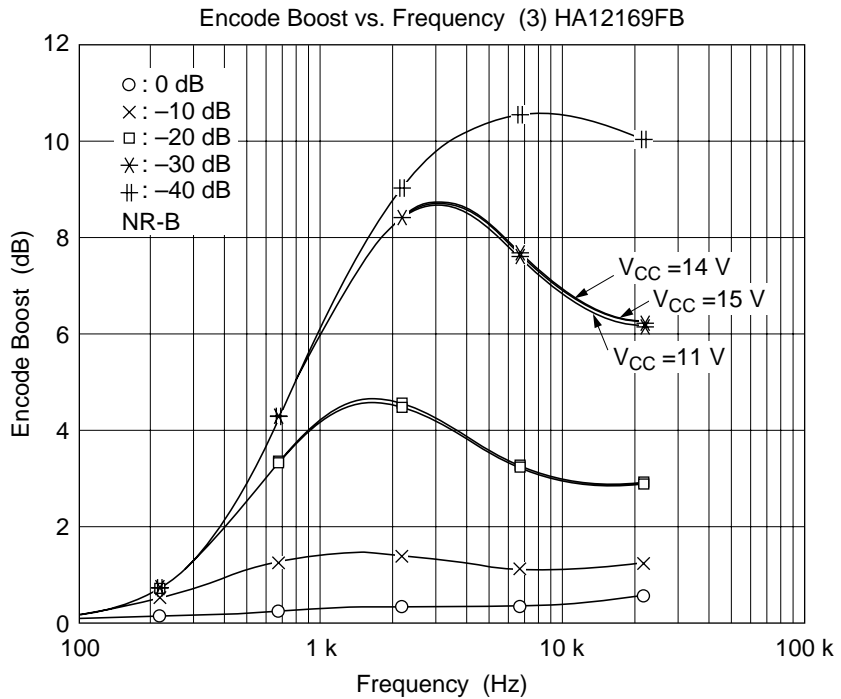
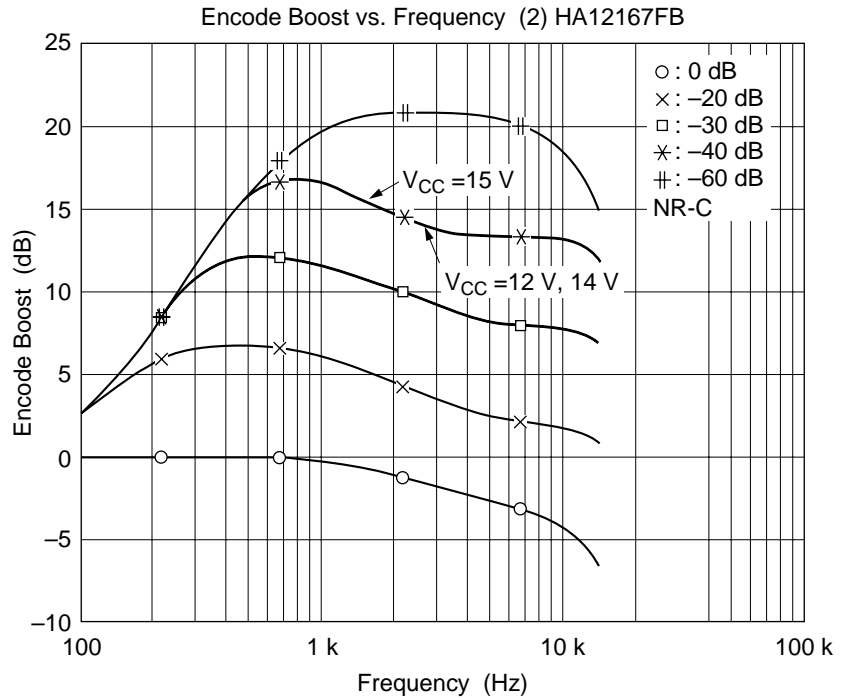
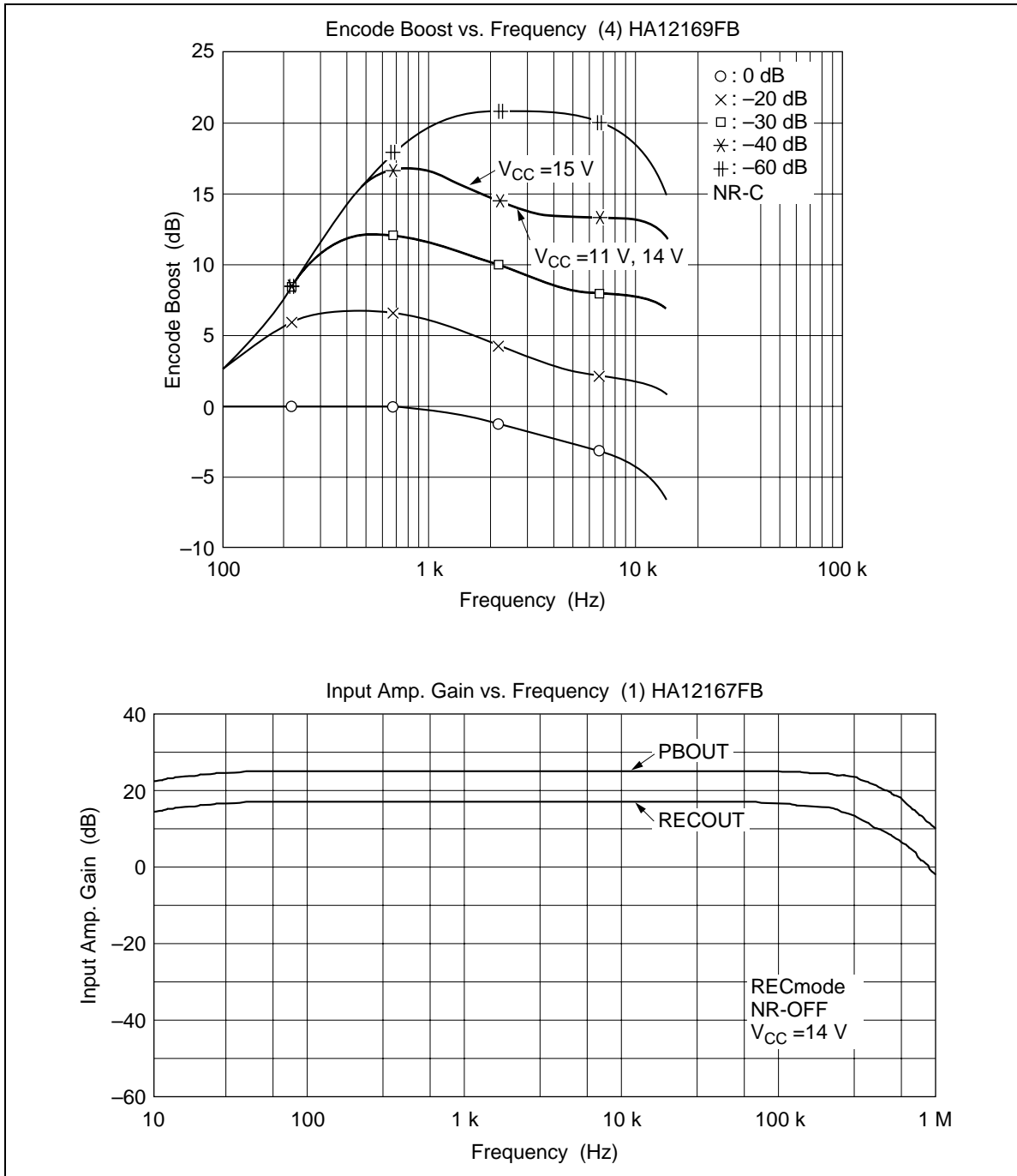


Figure 15 Switch by Tape Select

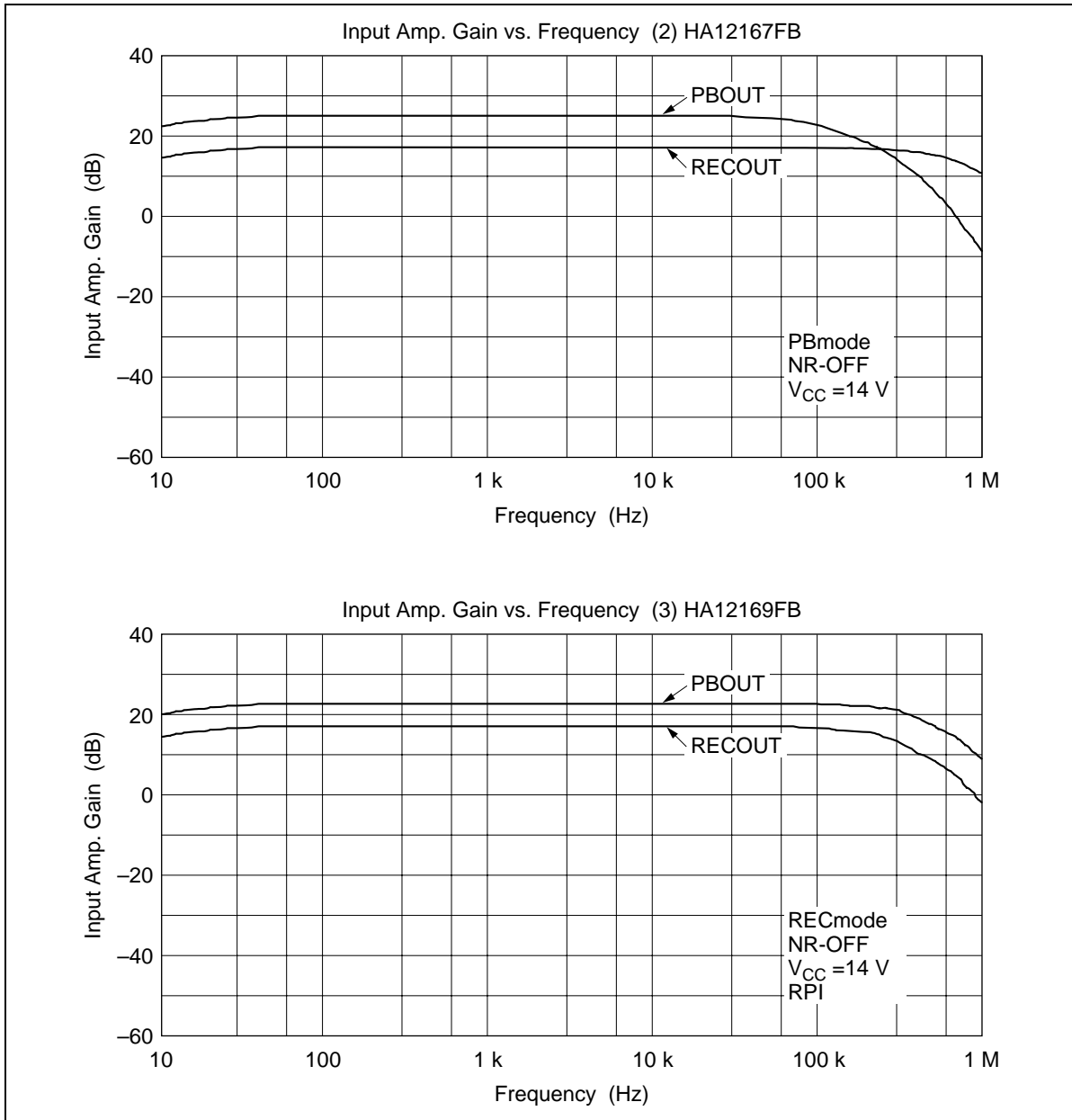


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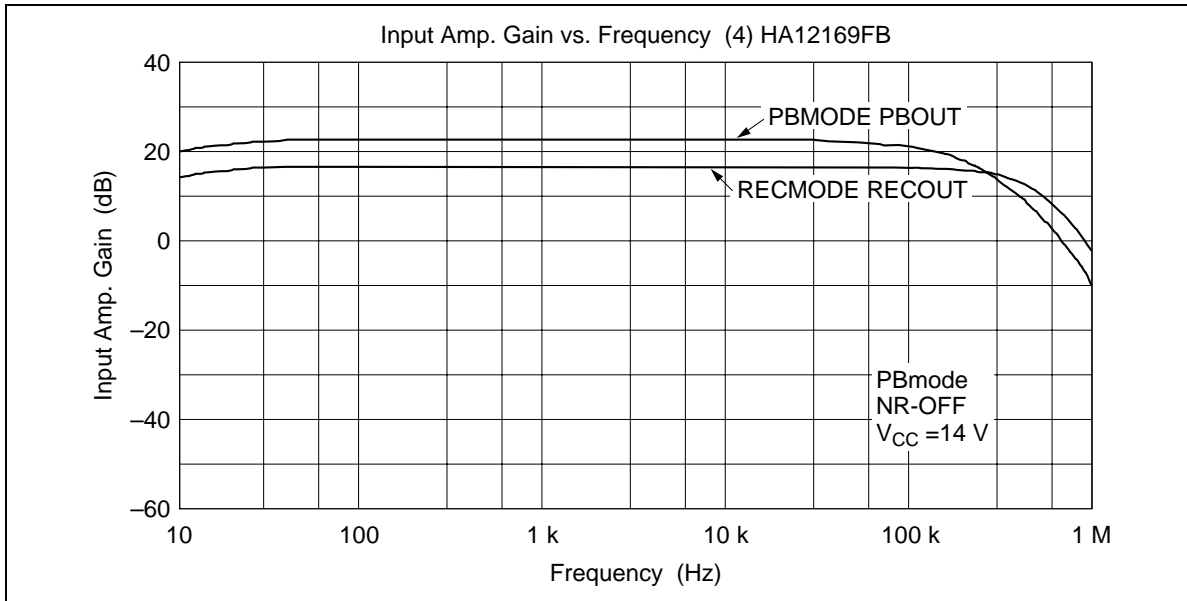




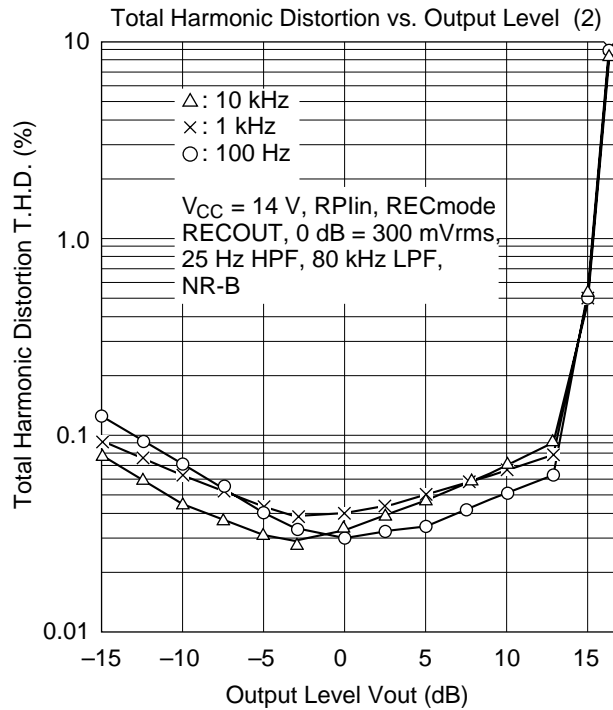
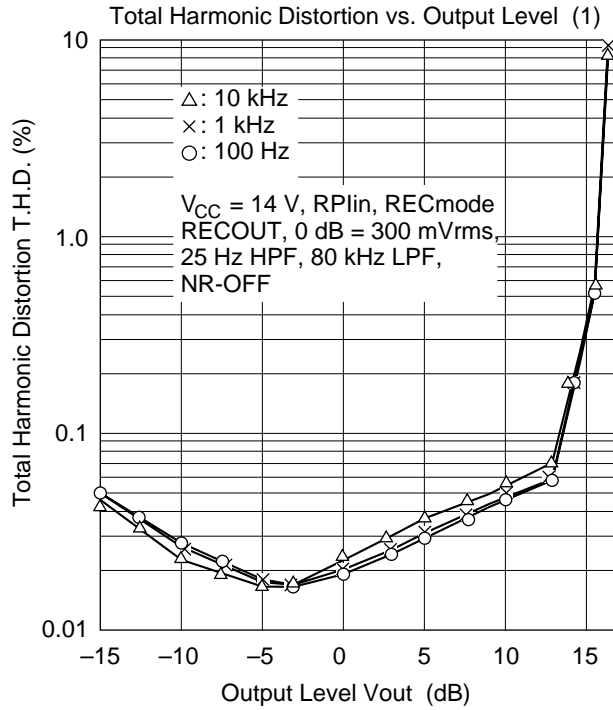
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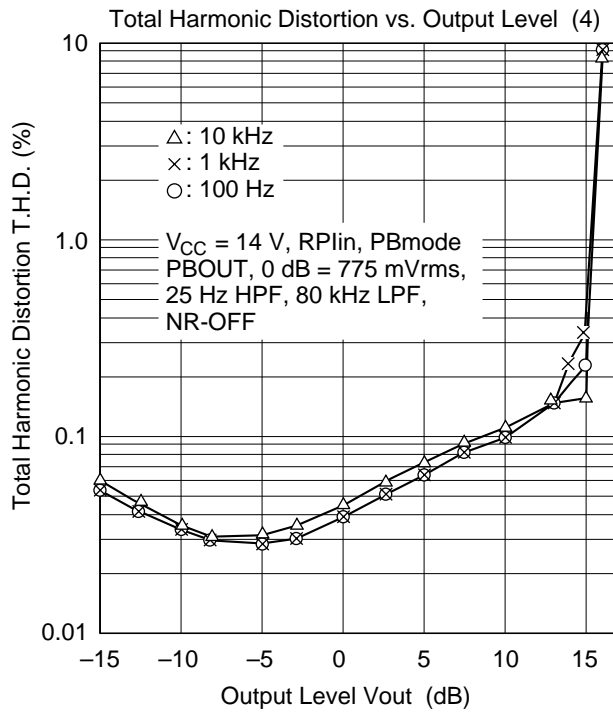
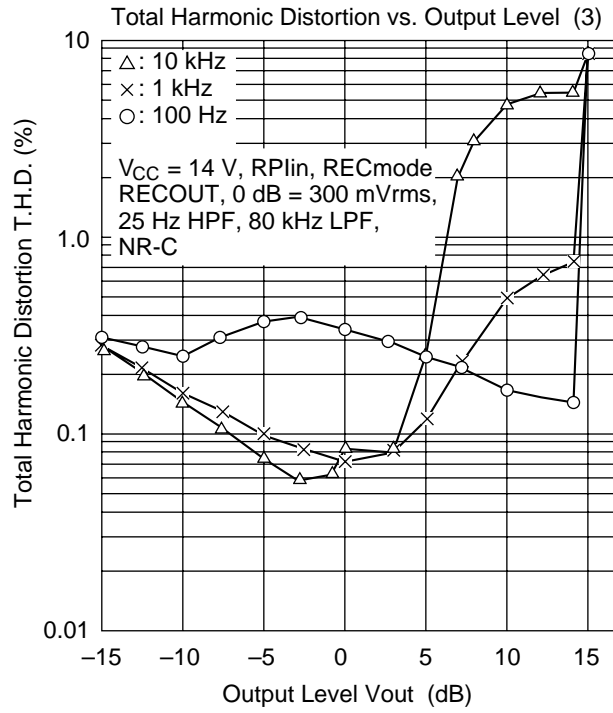


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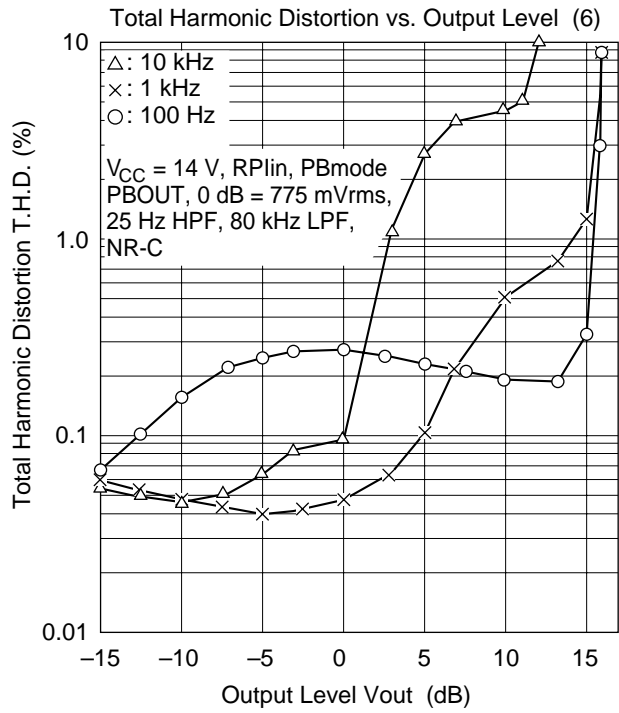
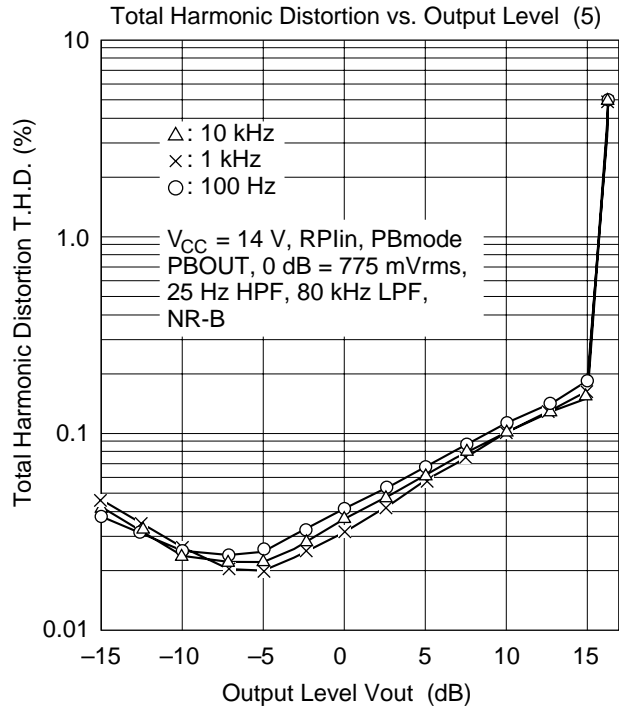


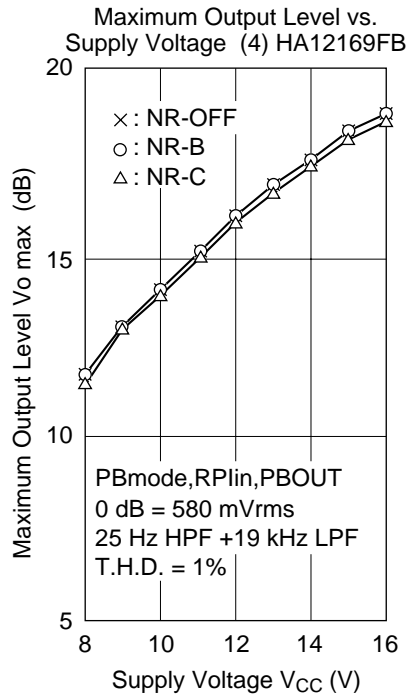
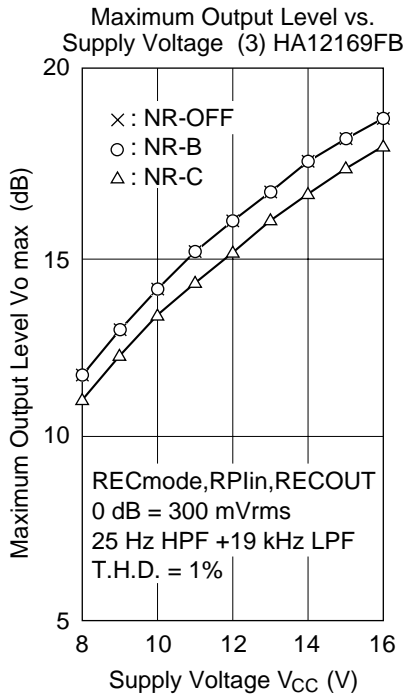
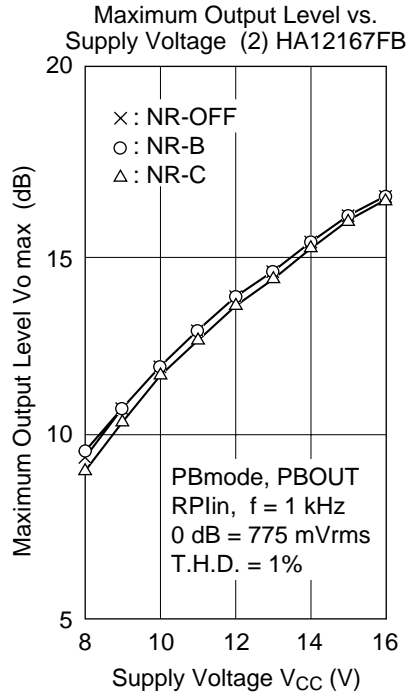
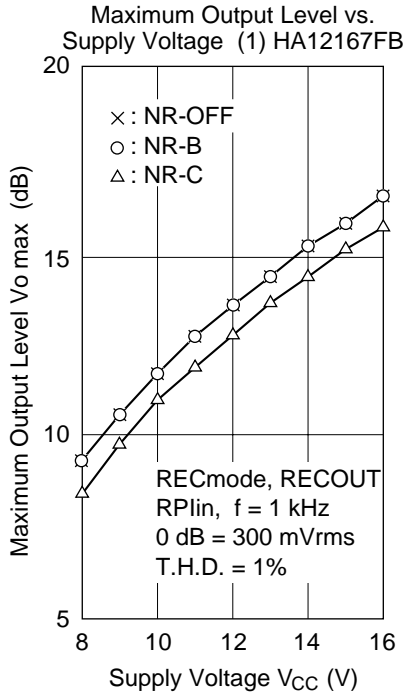
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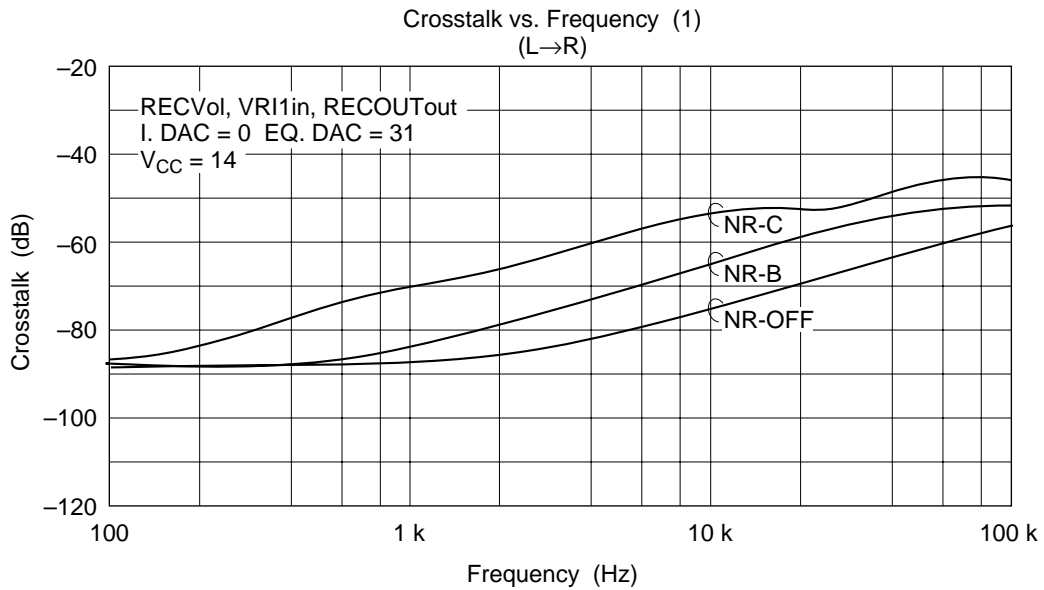
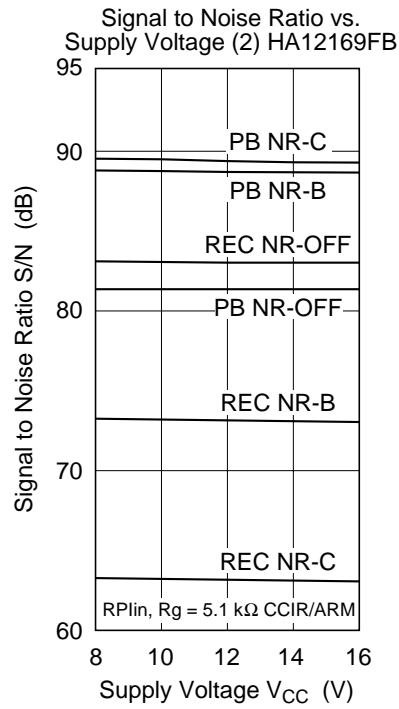
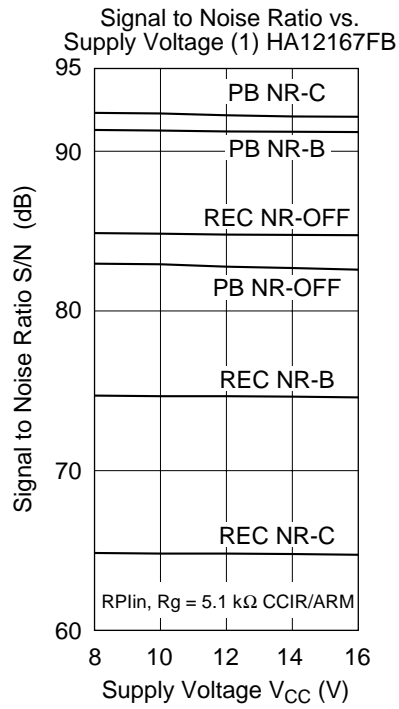


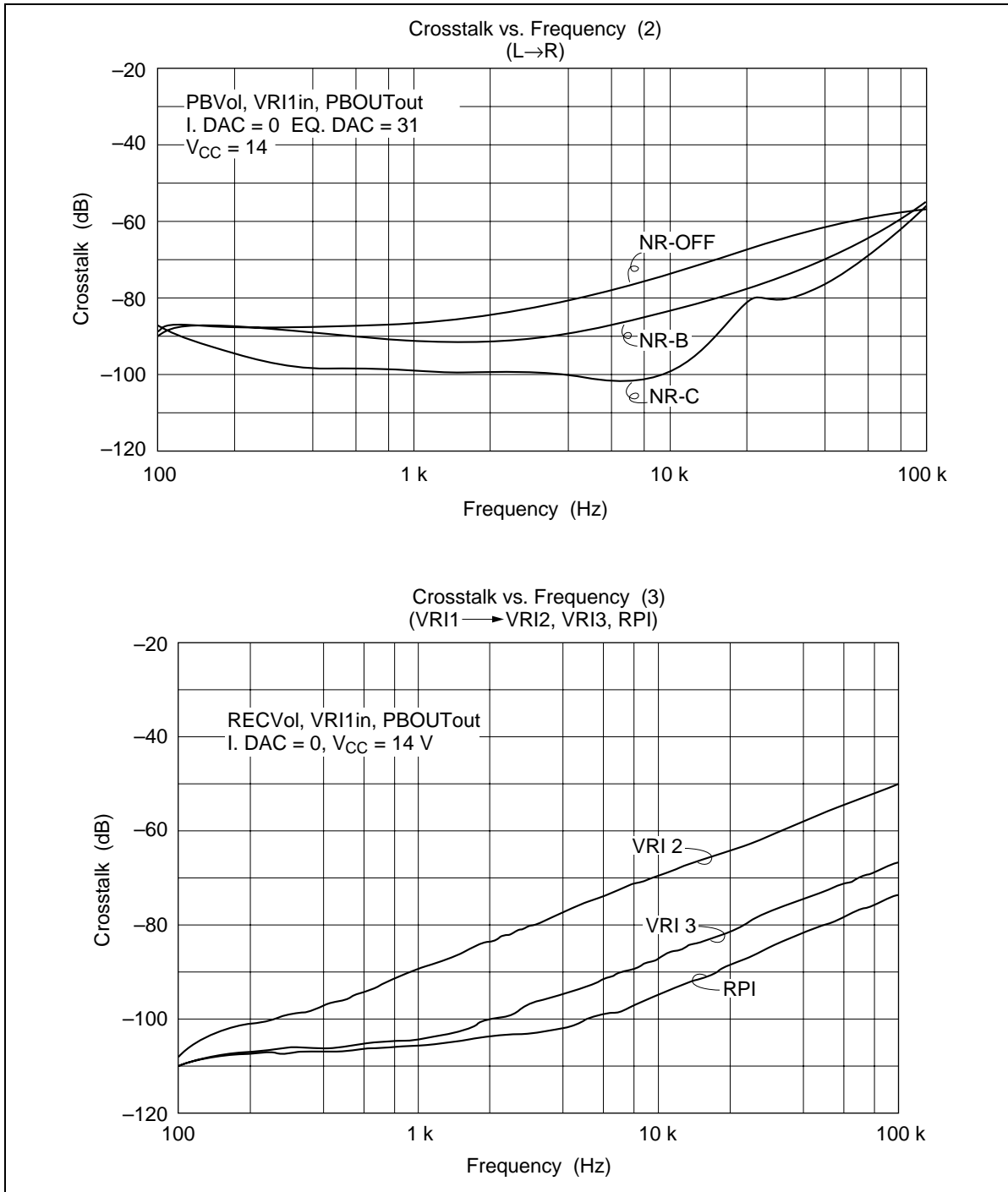
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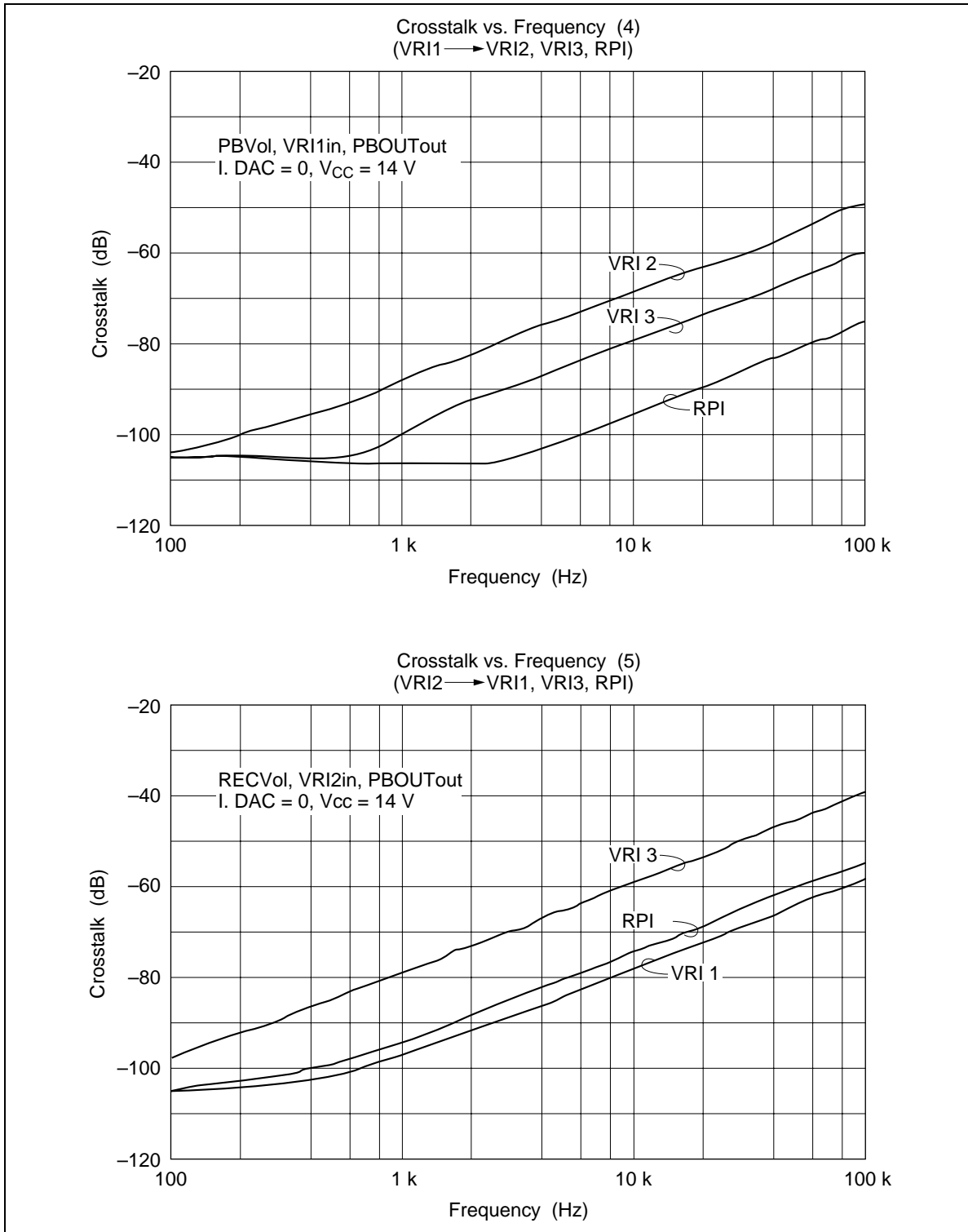


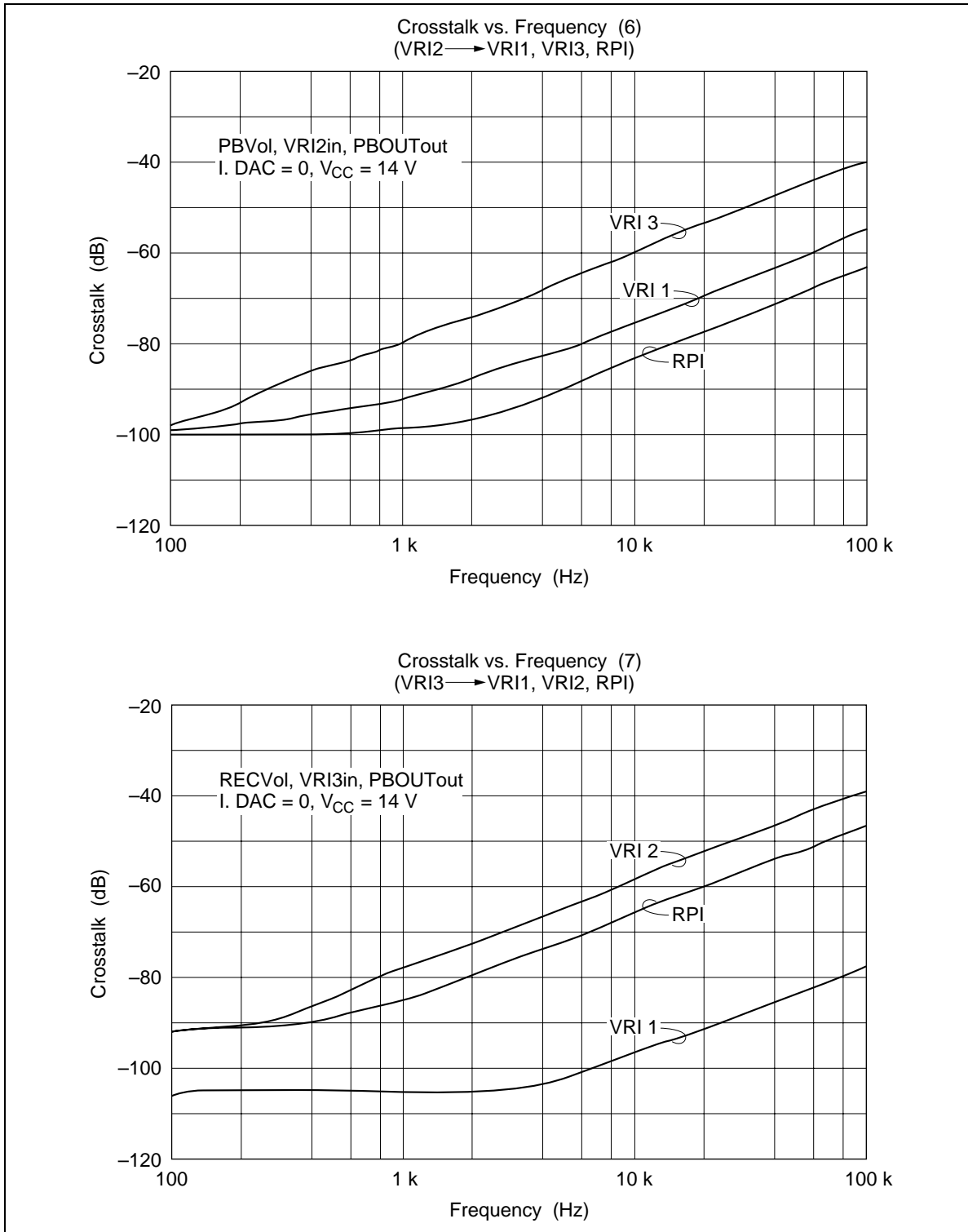
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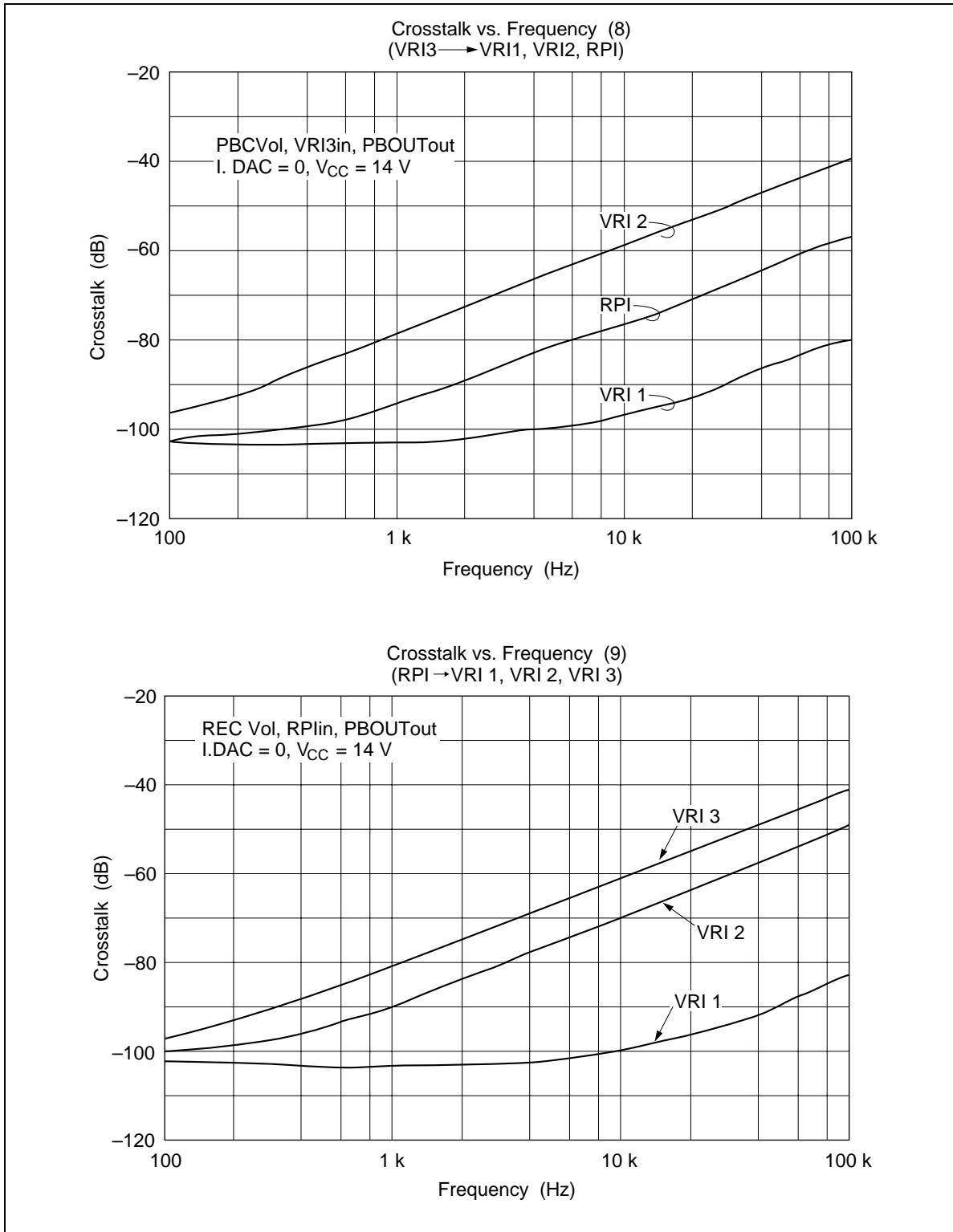


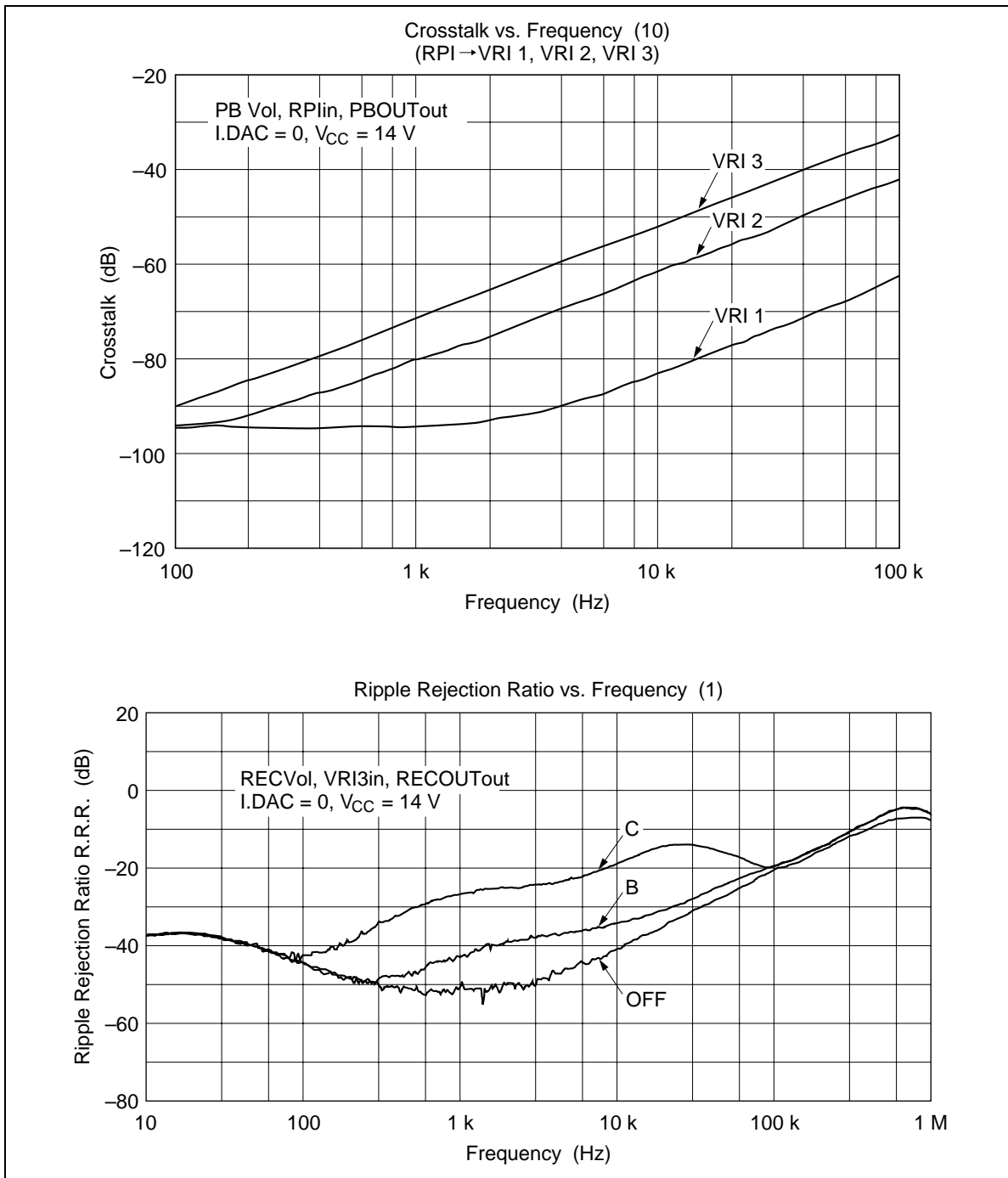
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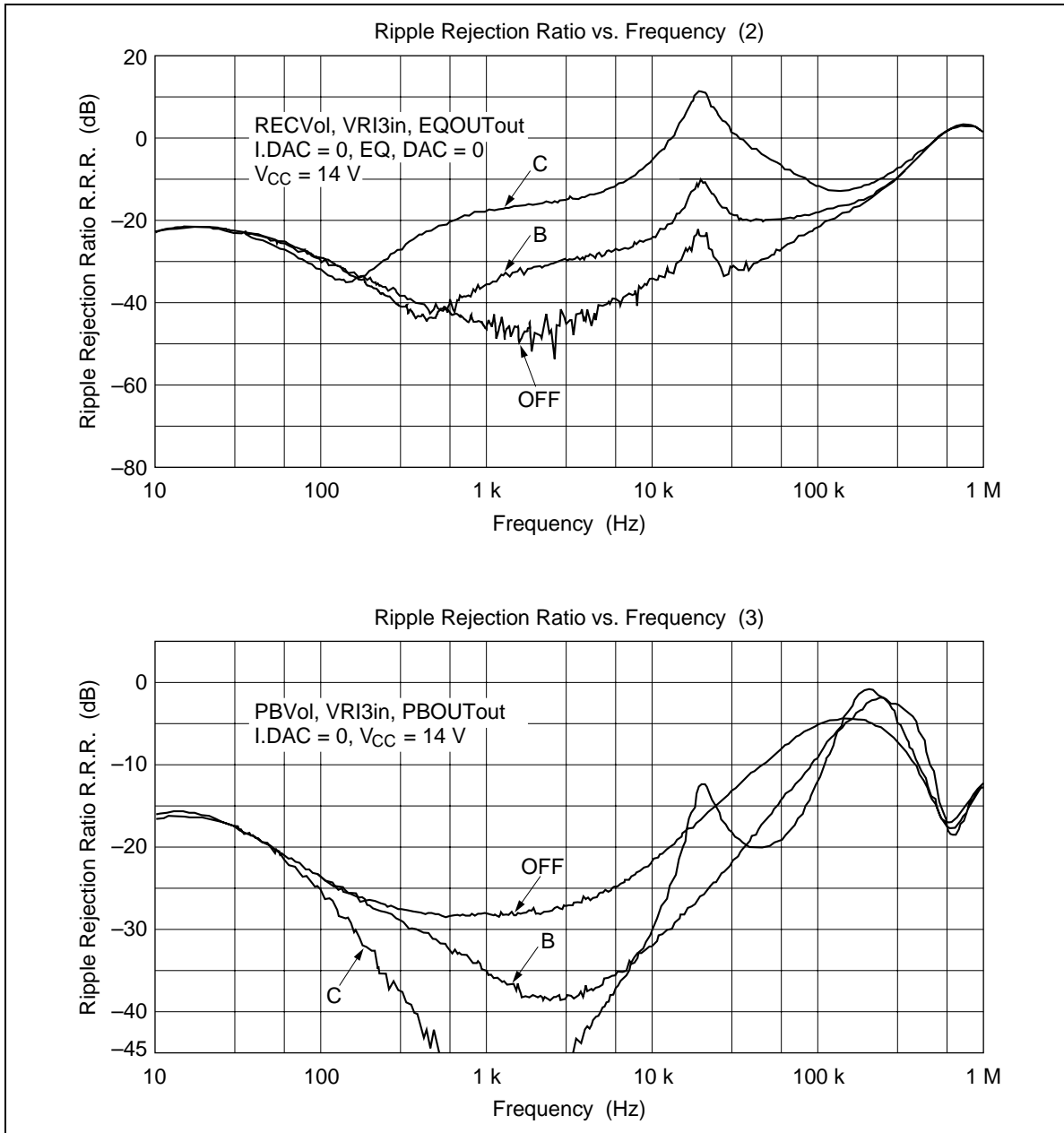


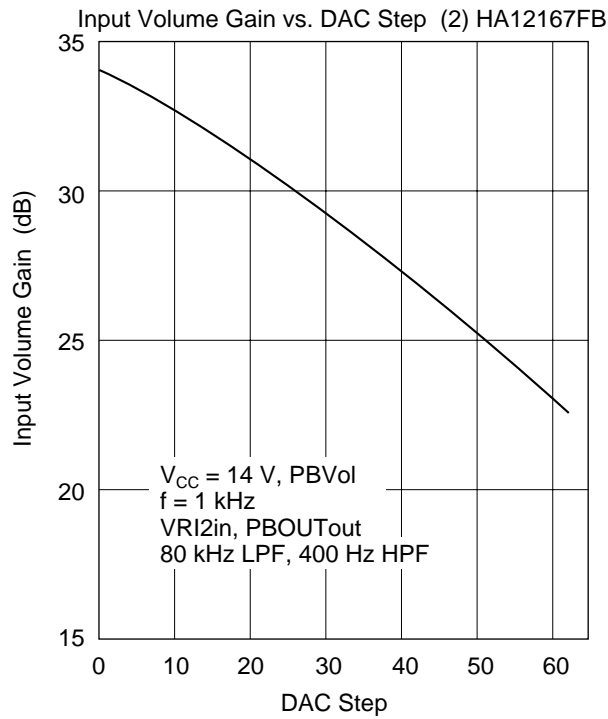
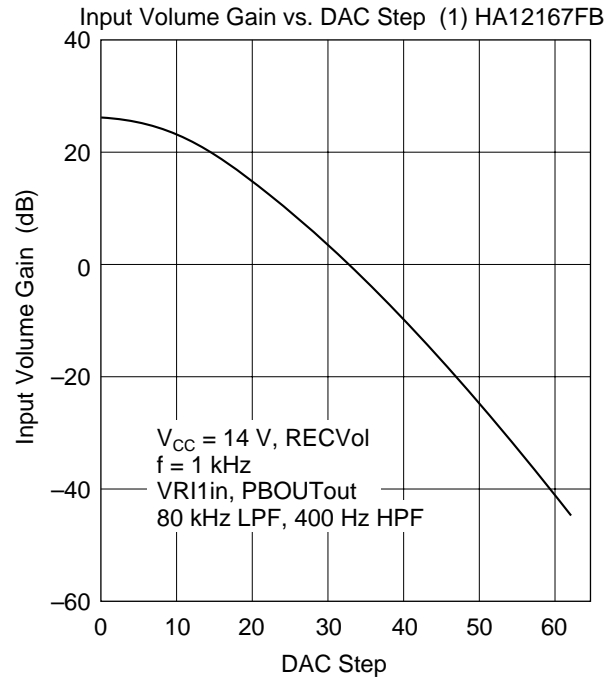
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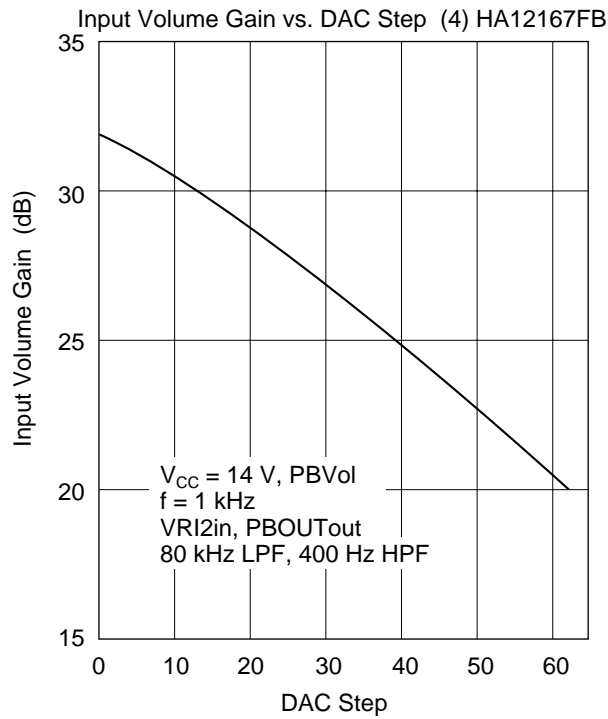
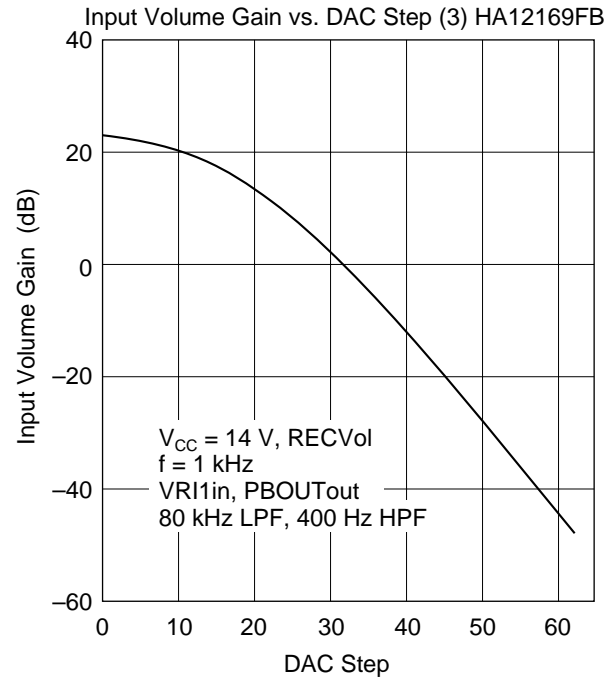


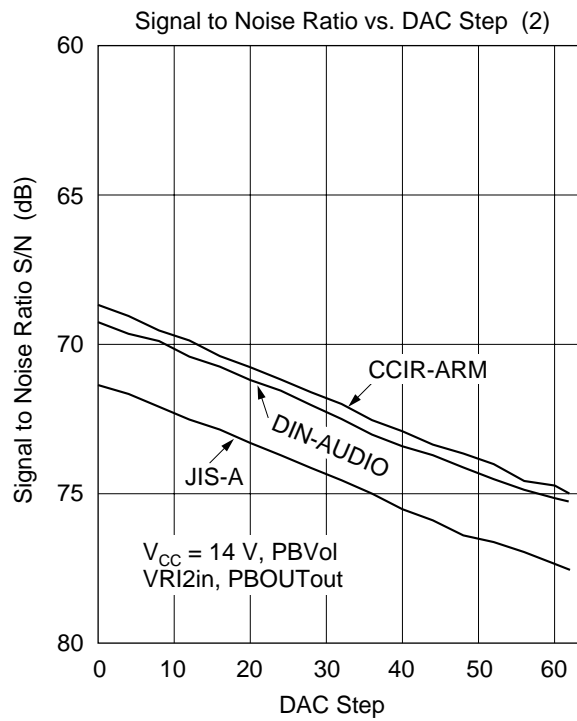
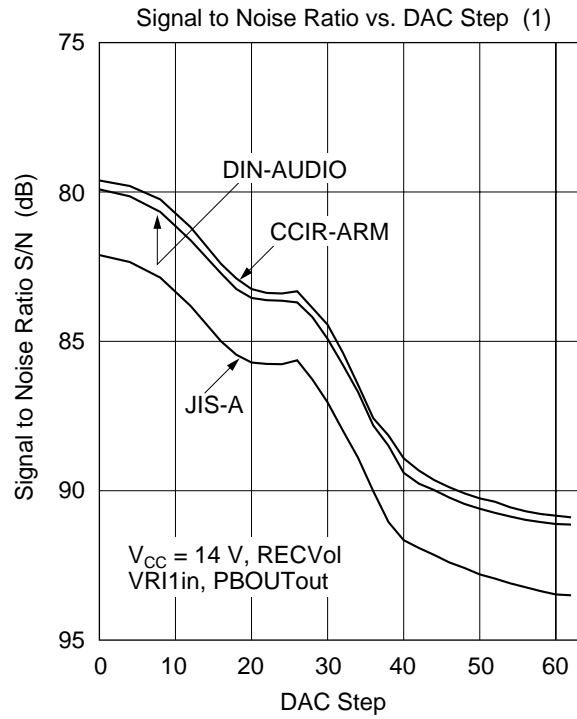
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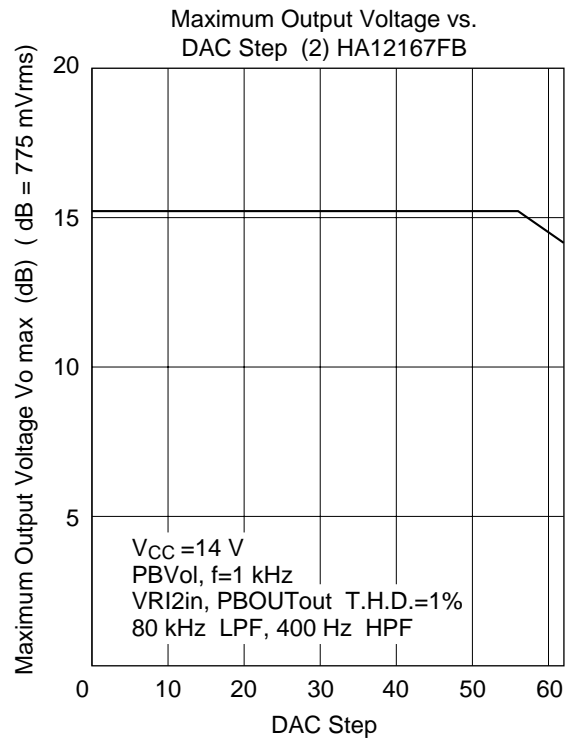
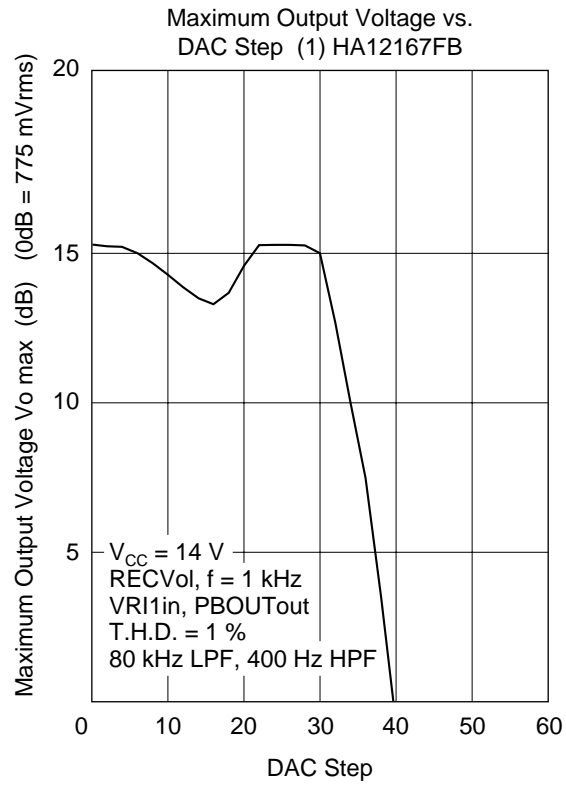


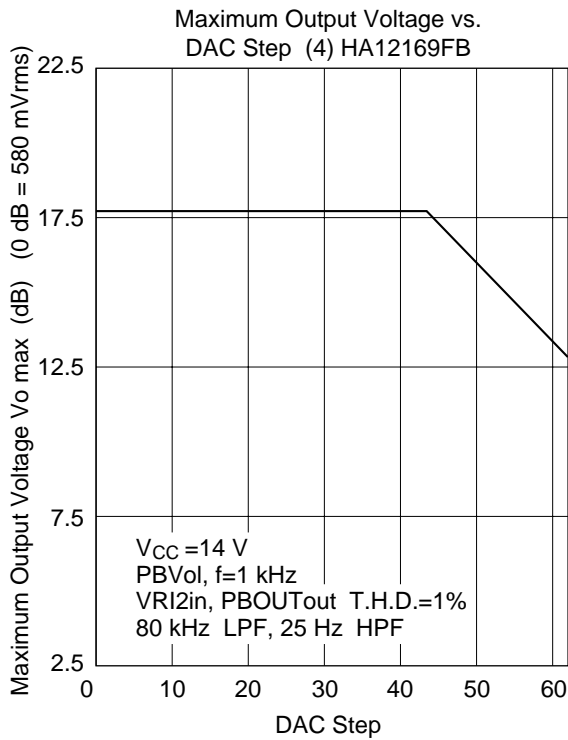
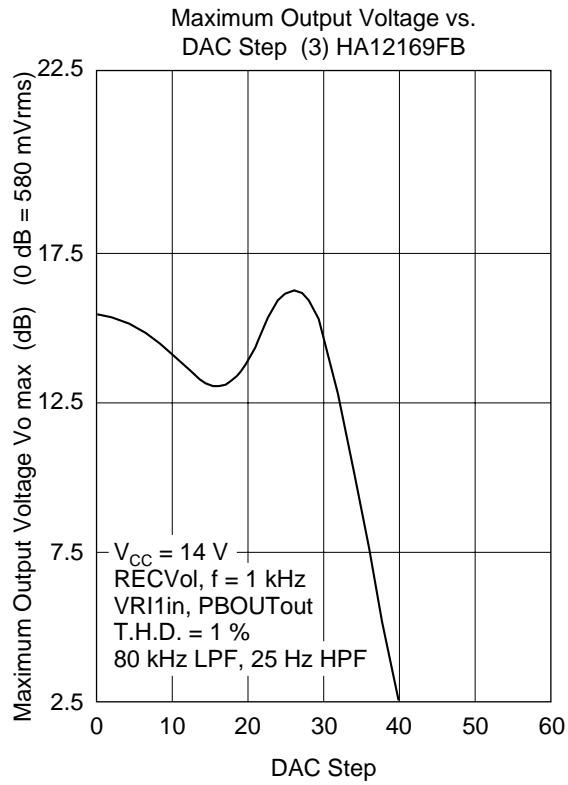
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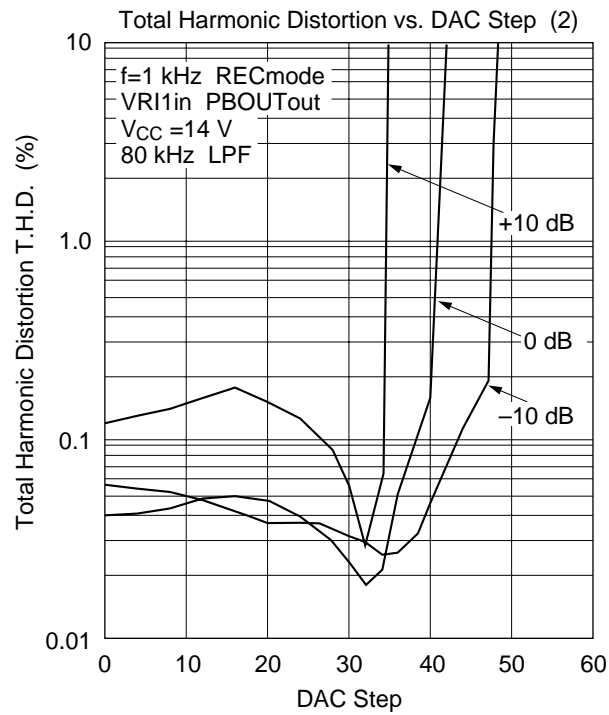
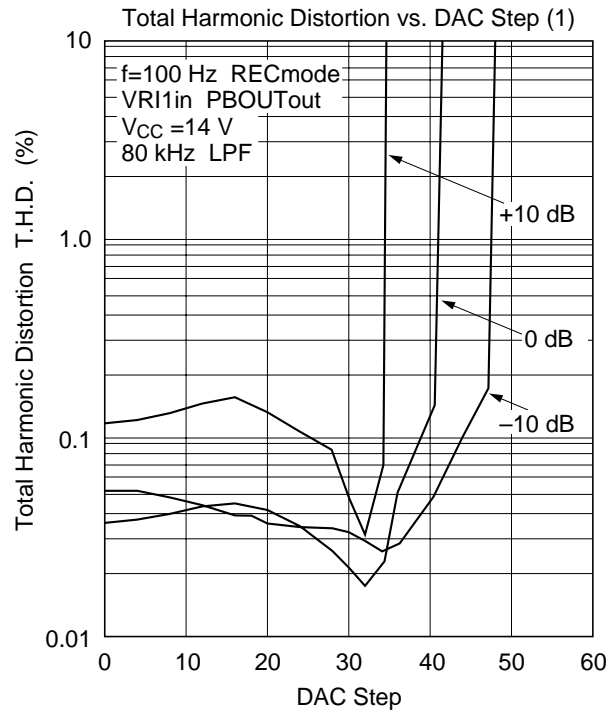


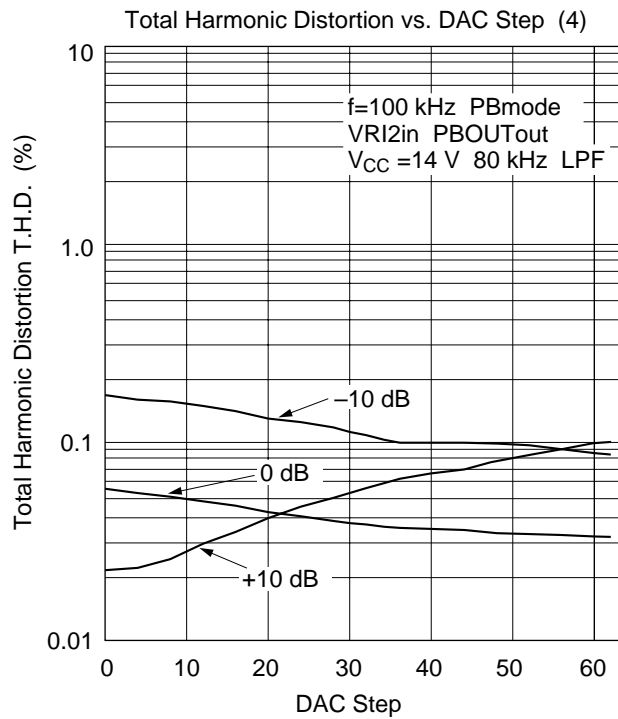
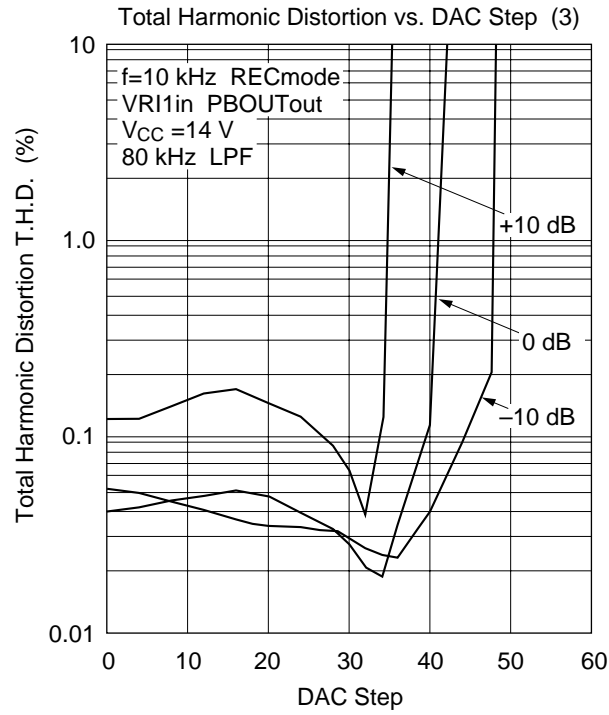
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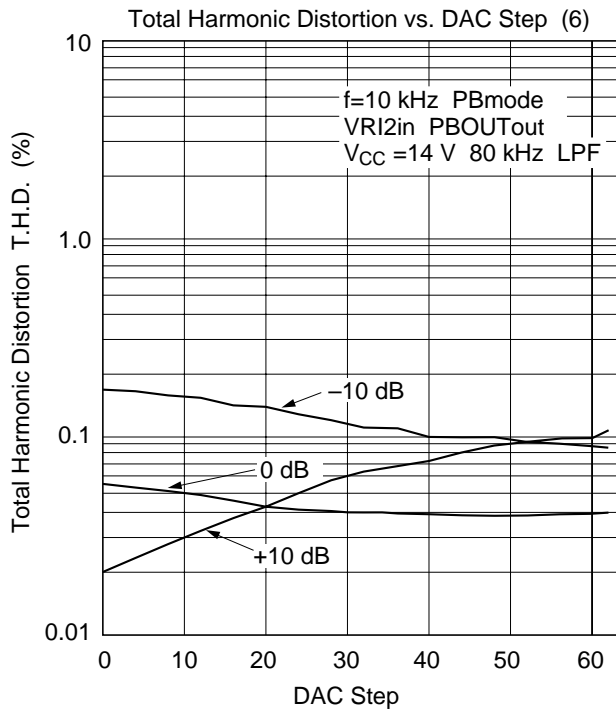
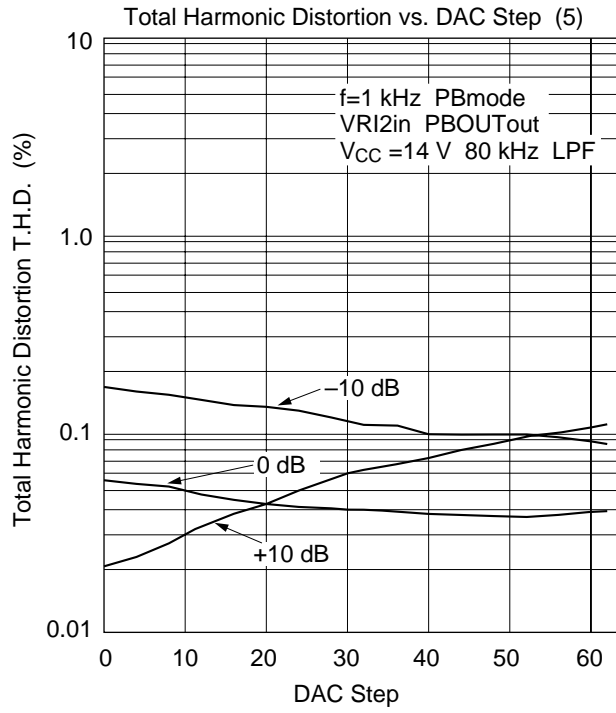


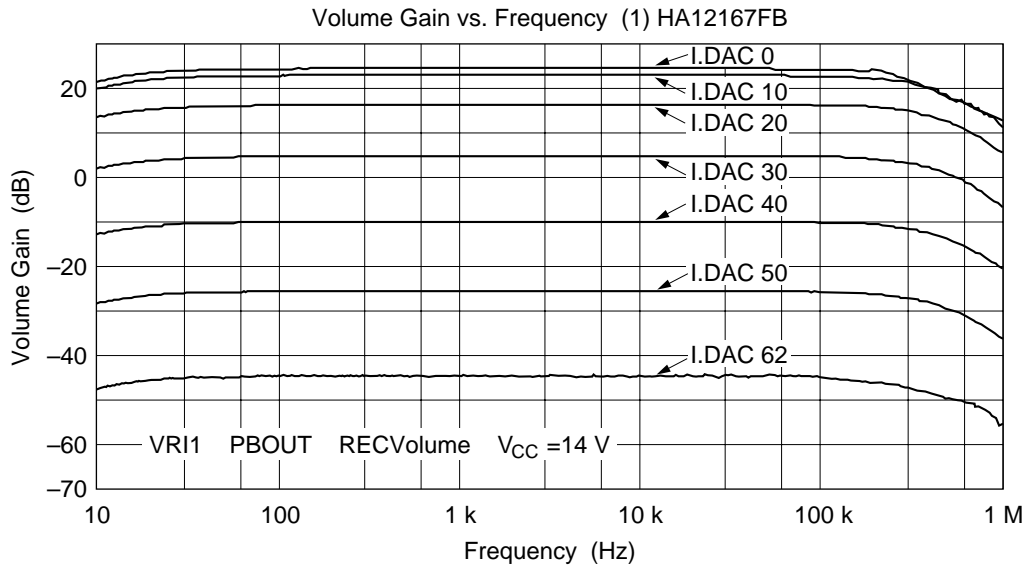
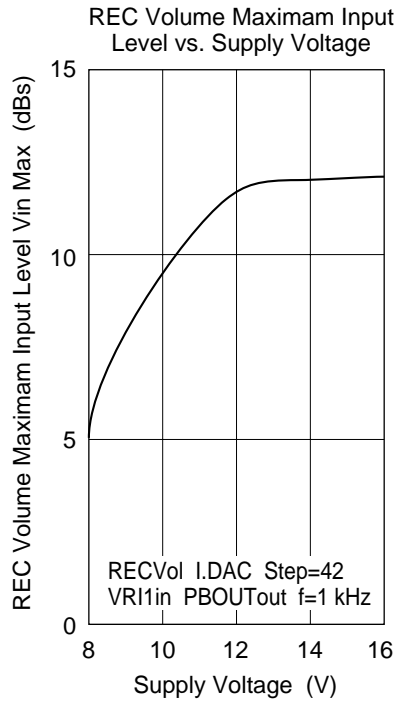
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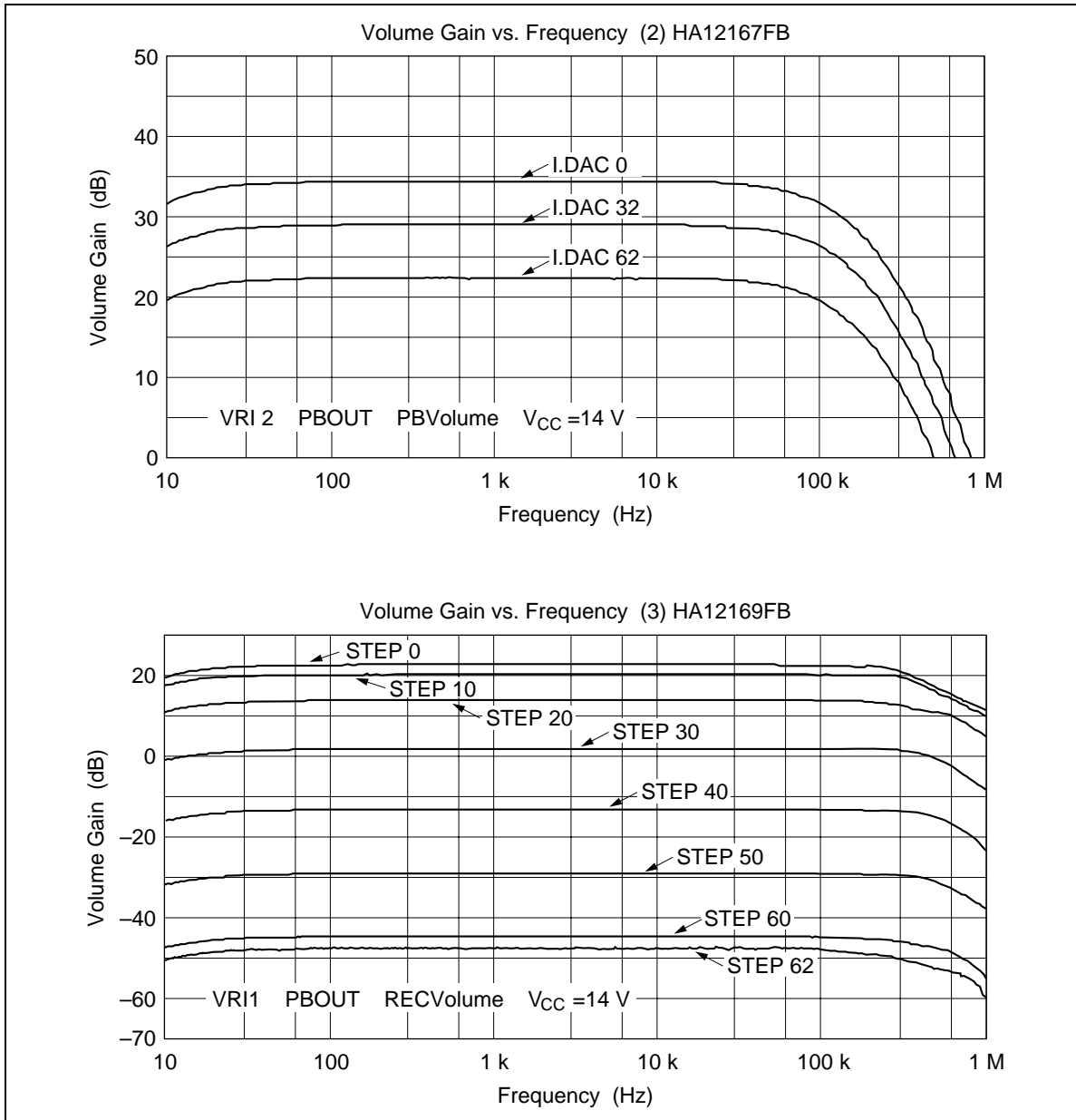


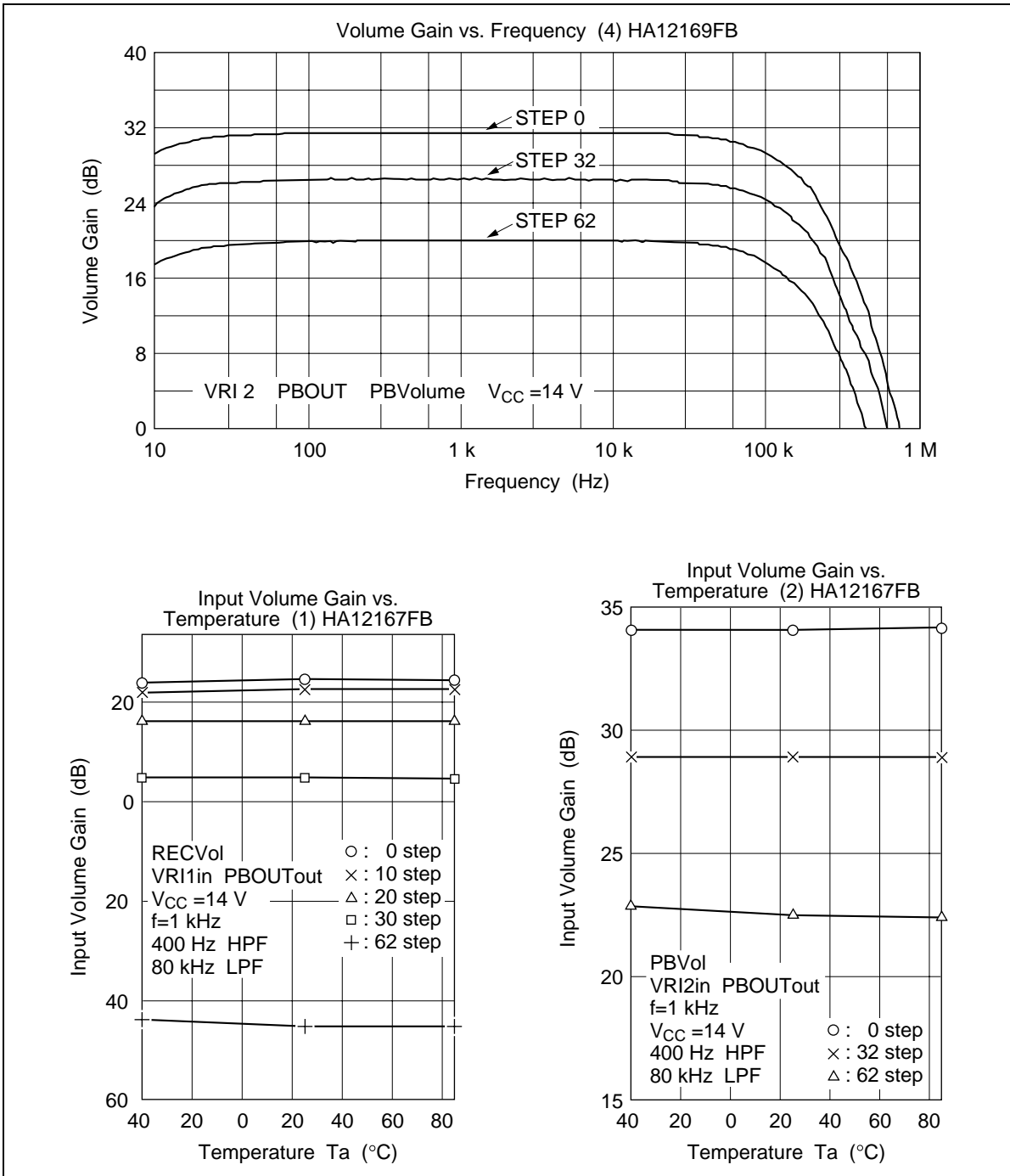
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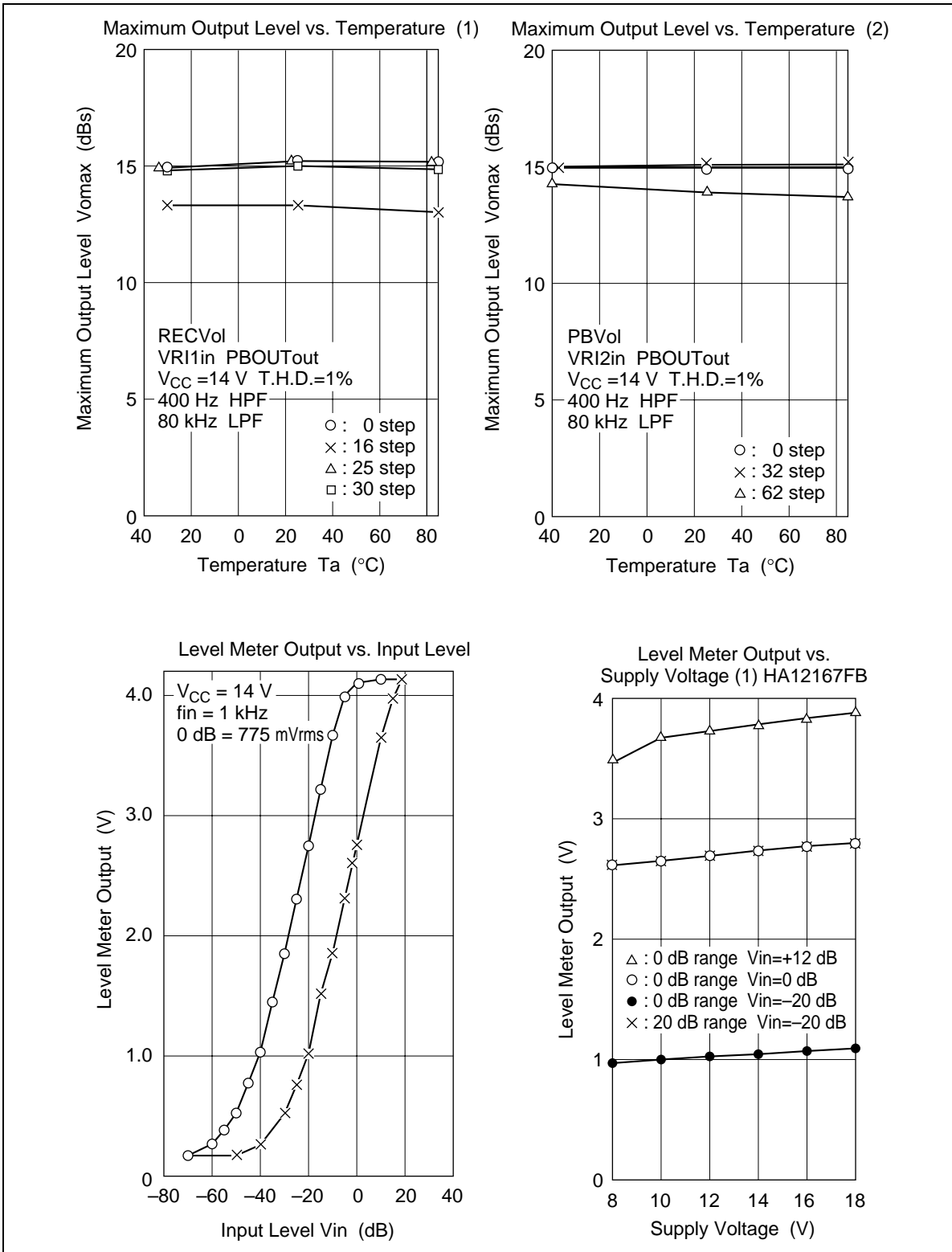


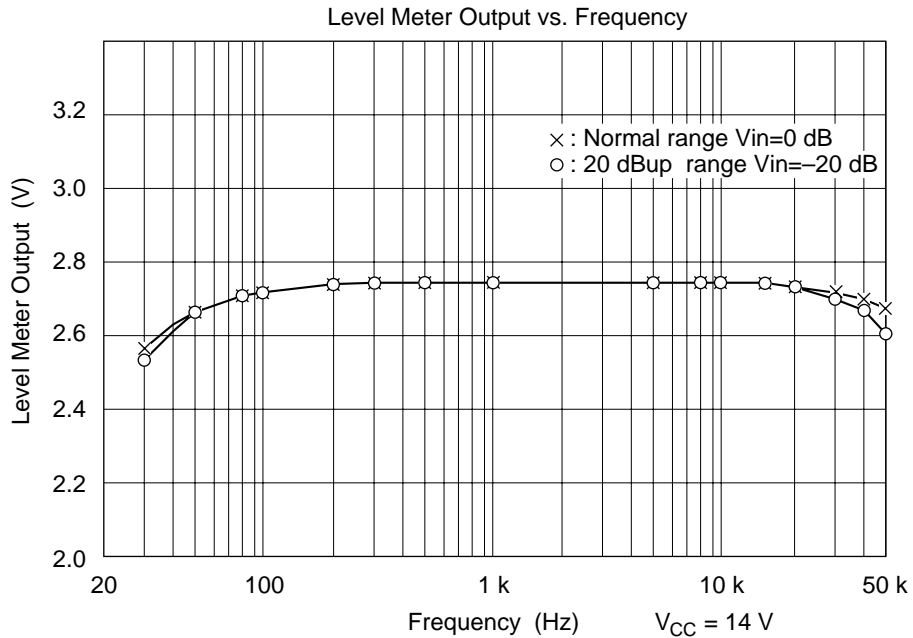
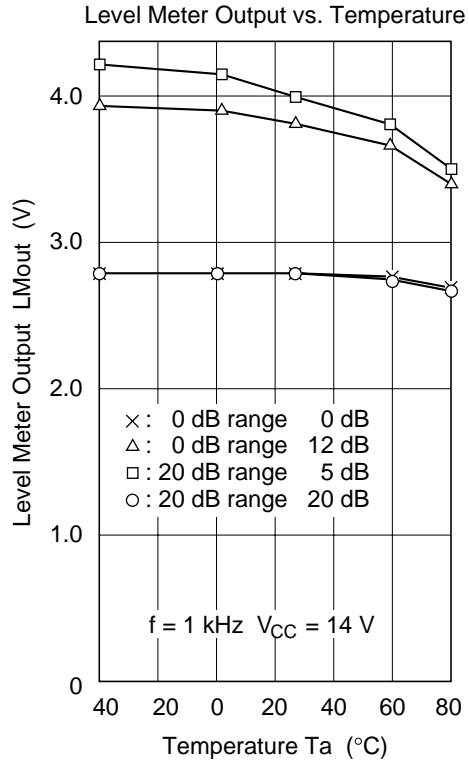
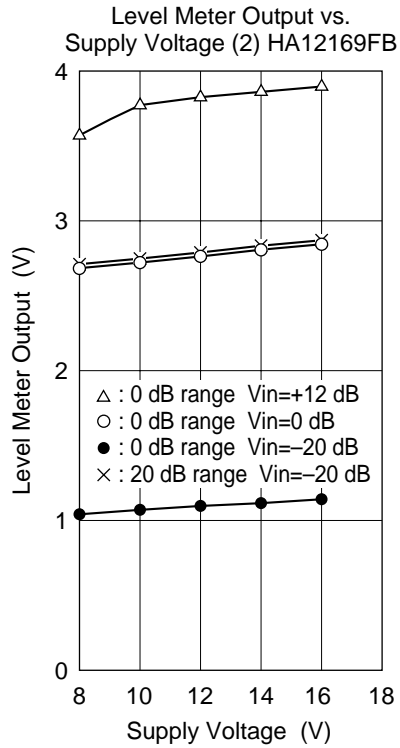
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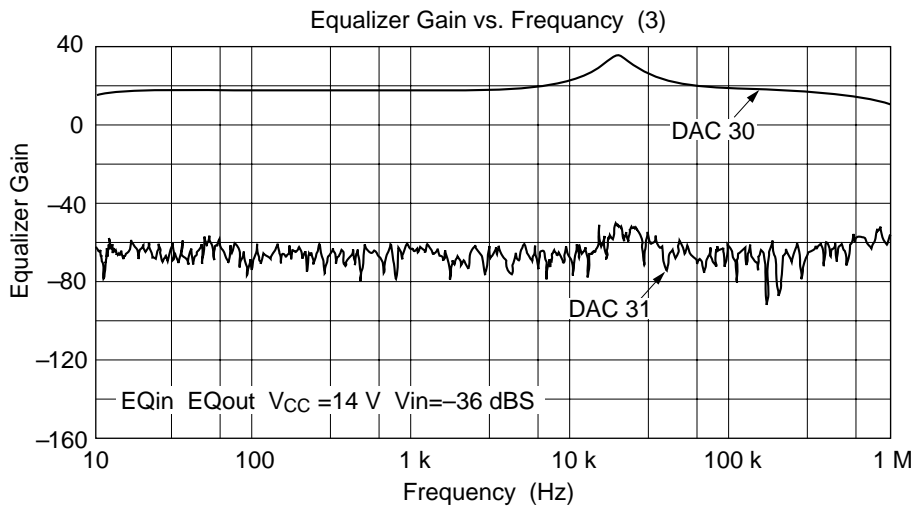
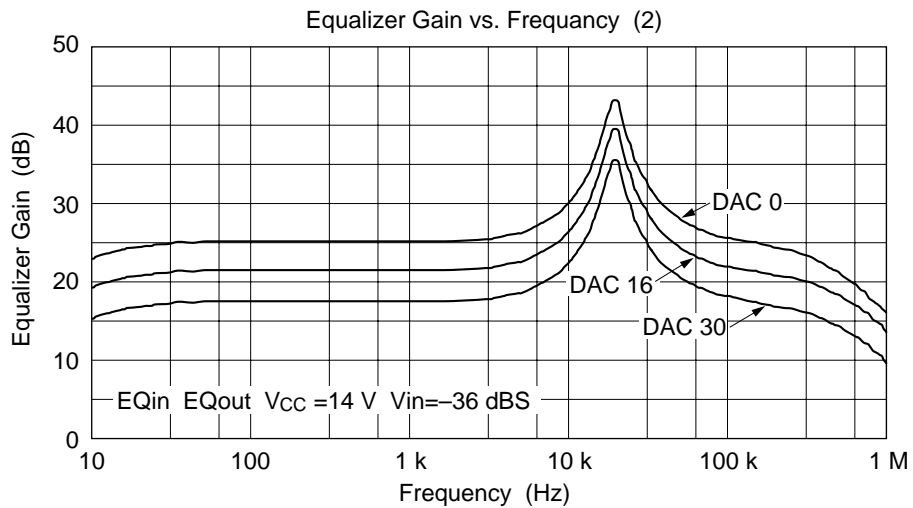
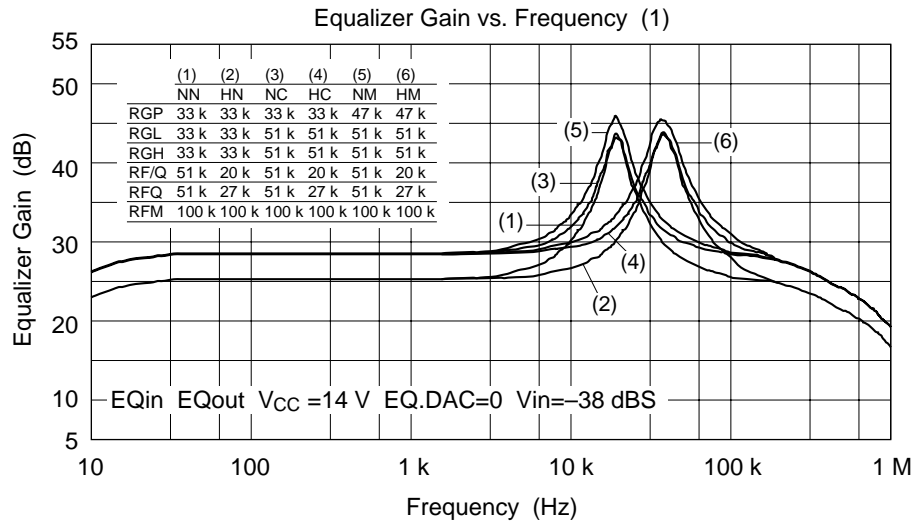


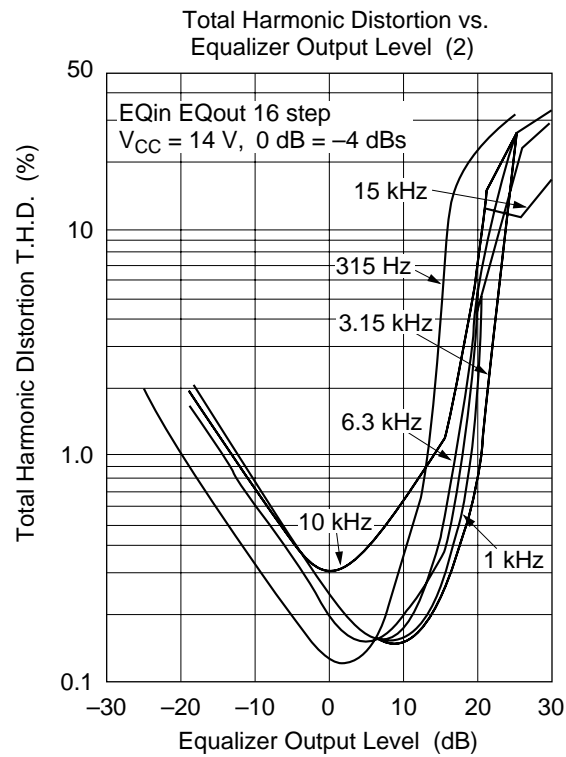
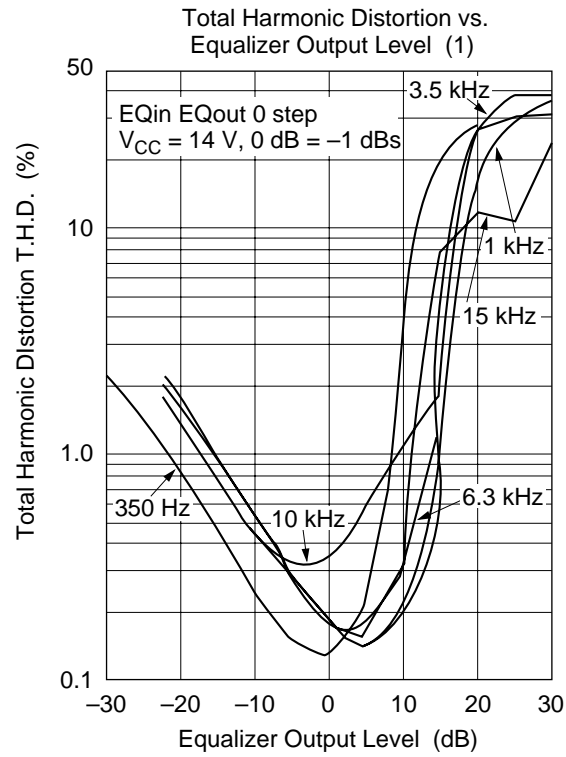
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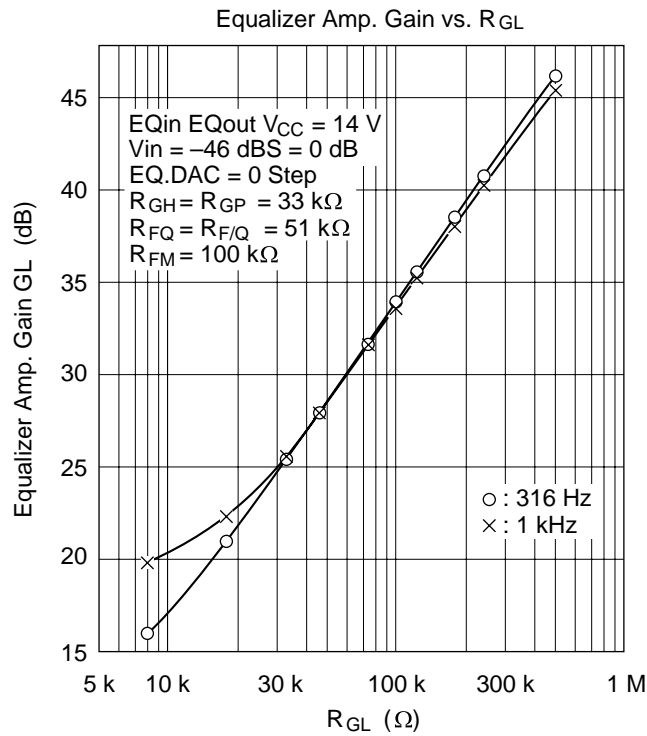
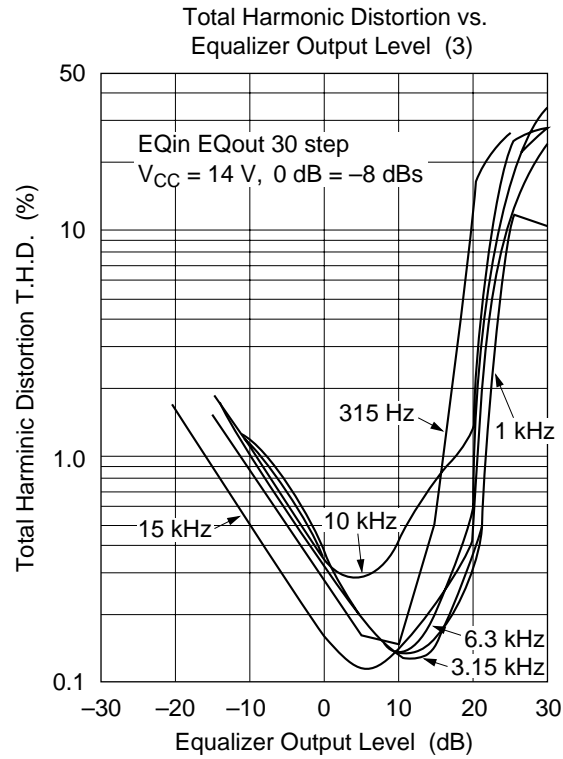


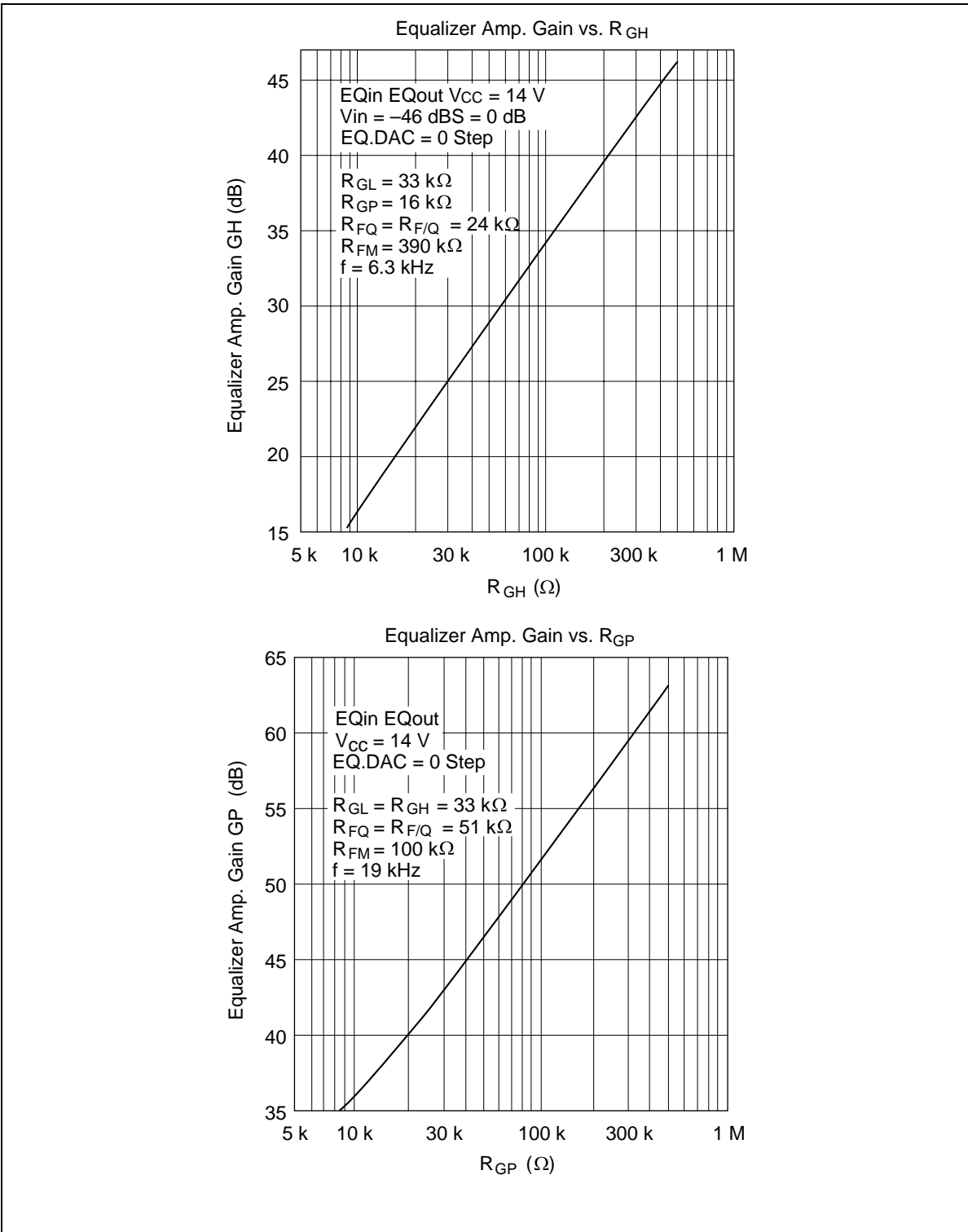
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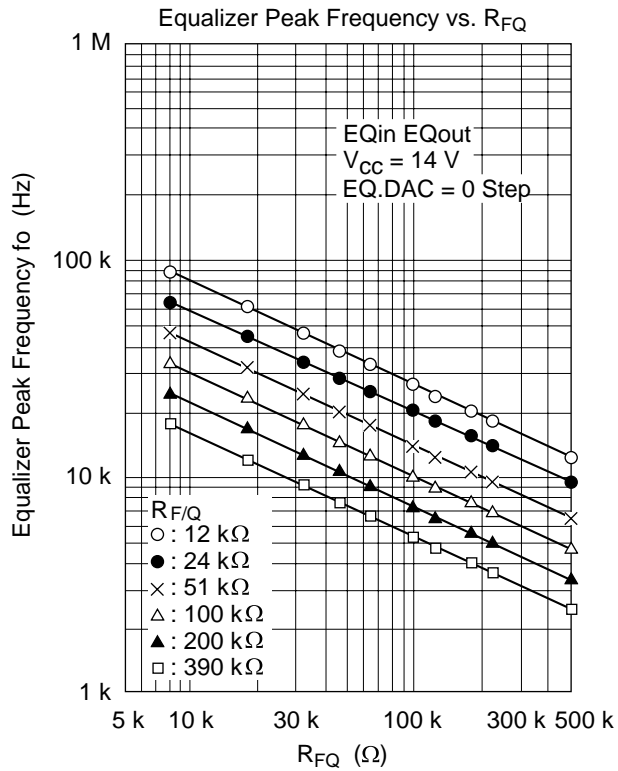
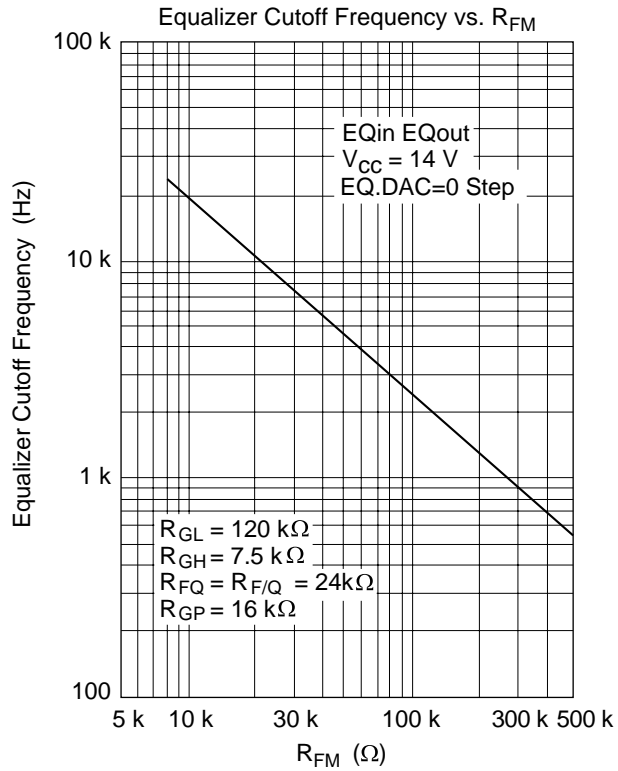


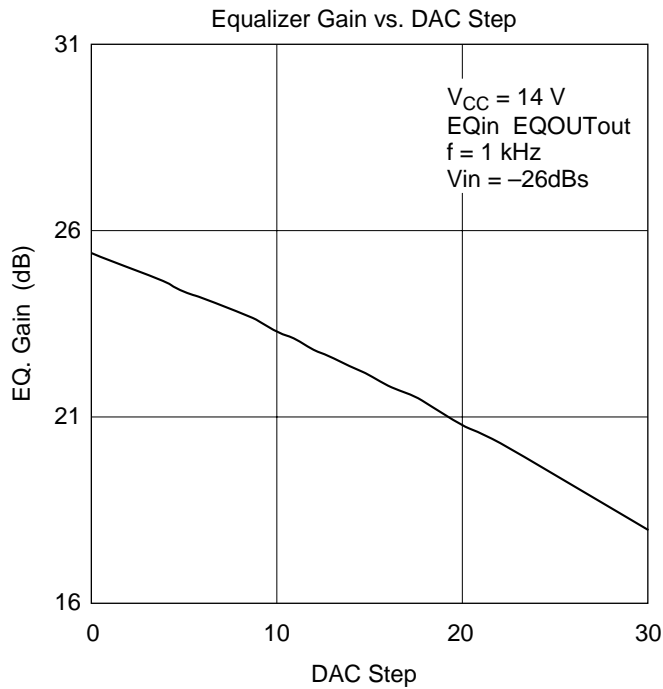
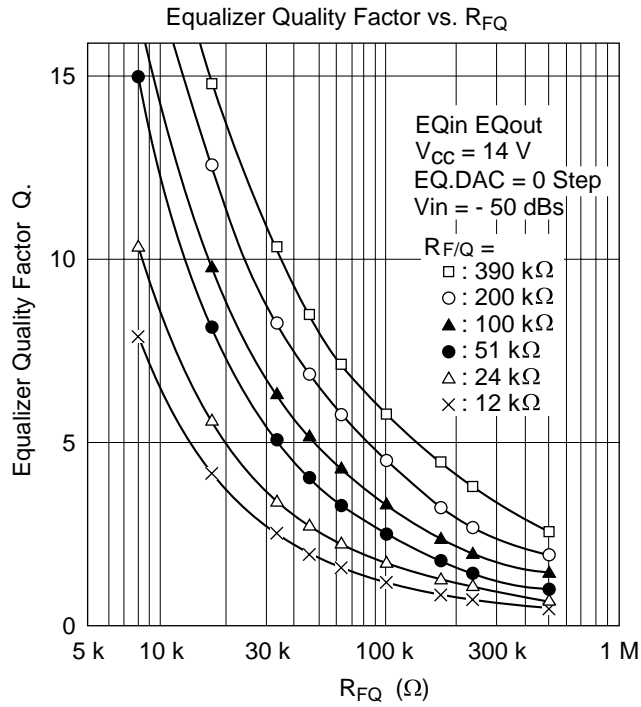
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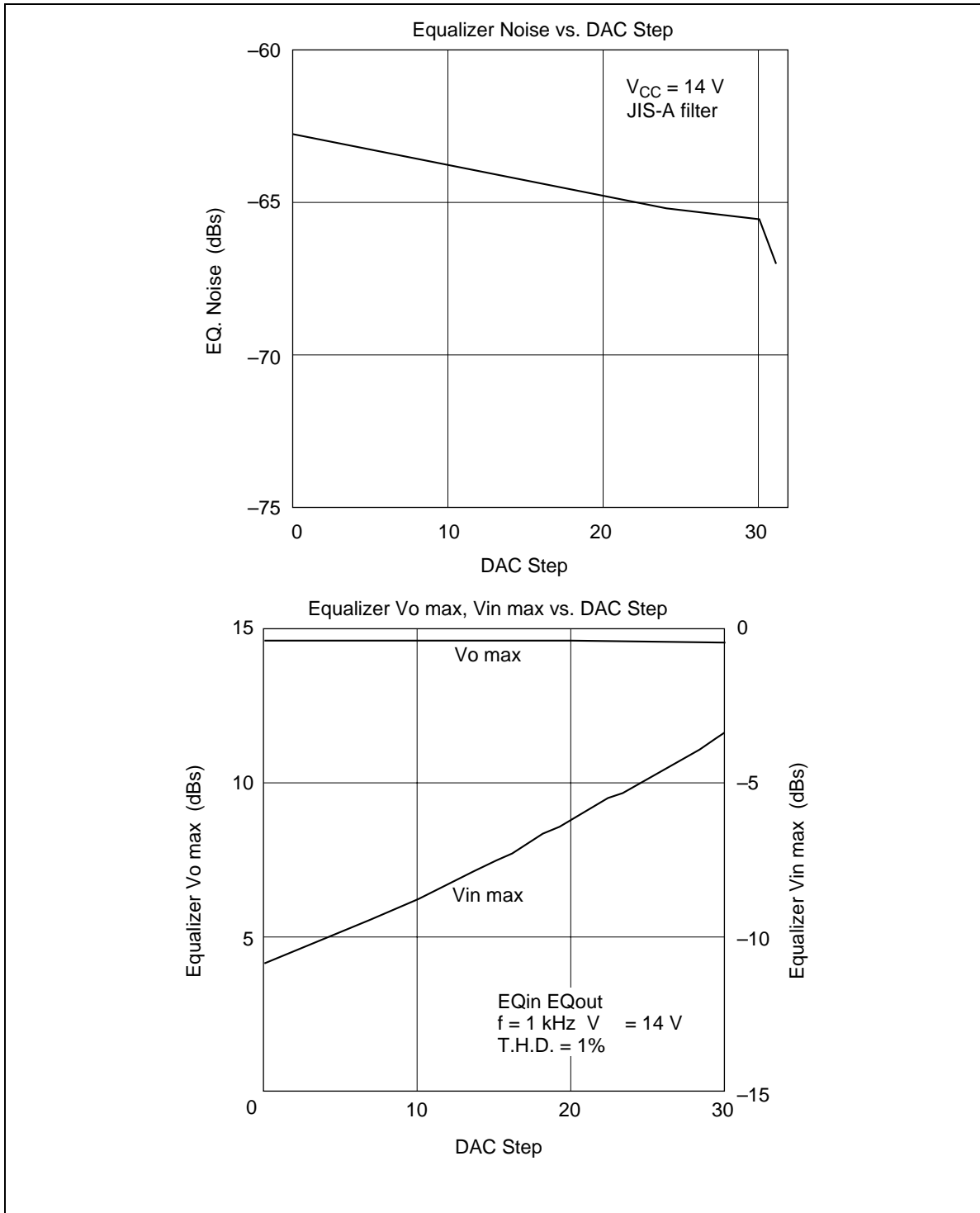


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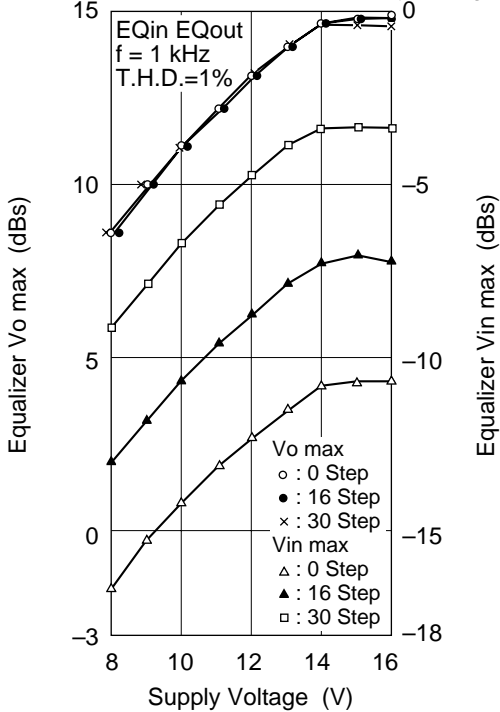




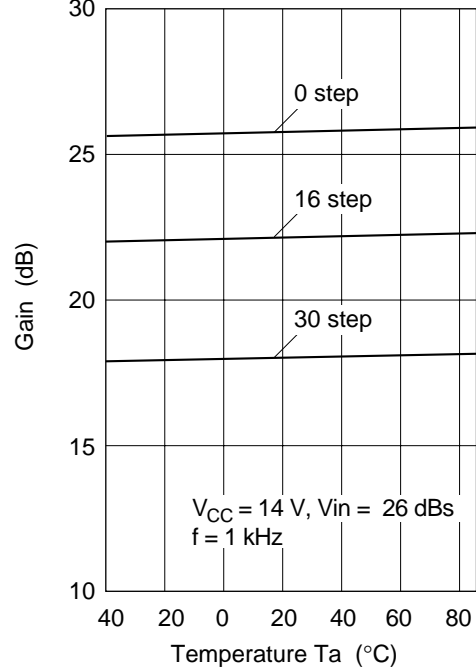
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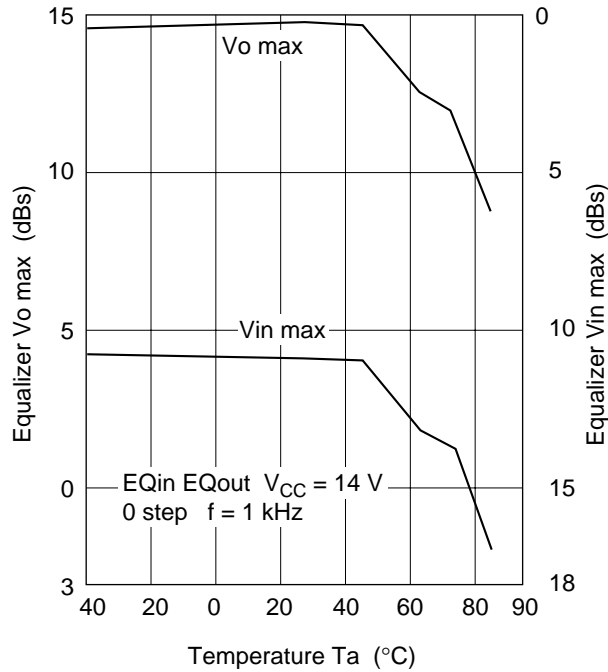
Equalizer Vo max, Vin max vs. Supply Voltage



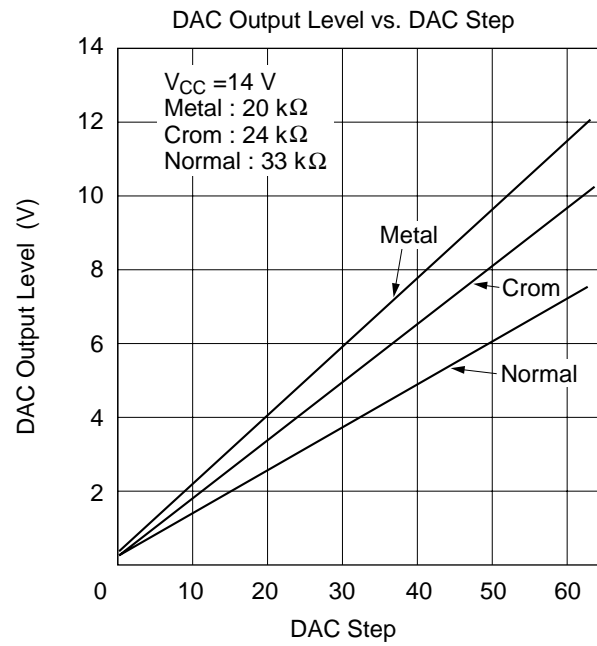
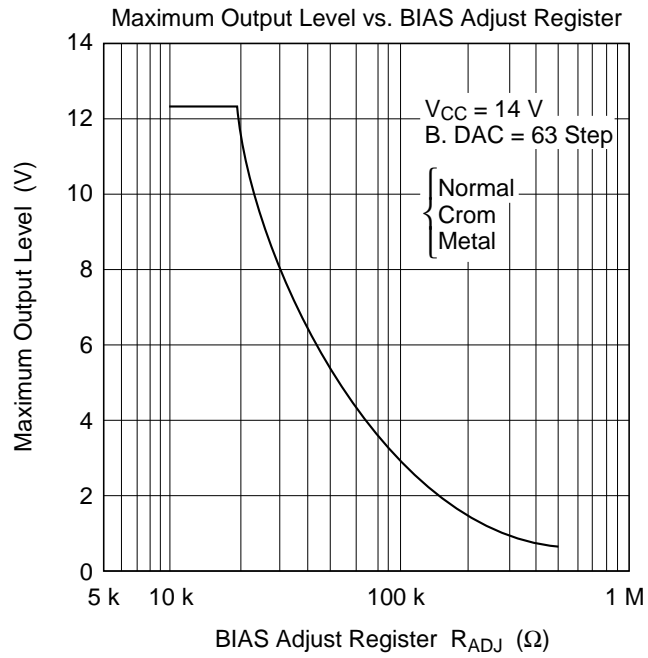
Equalizer Gain vs. Temperature

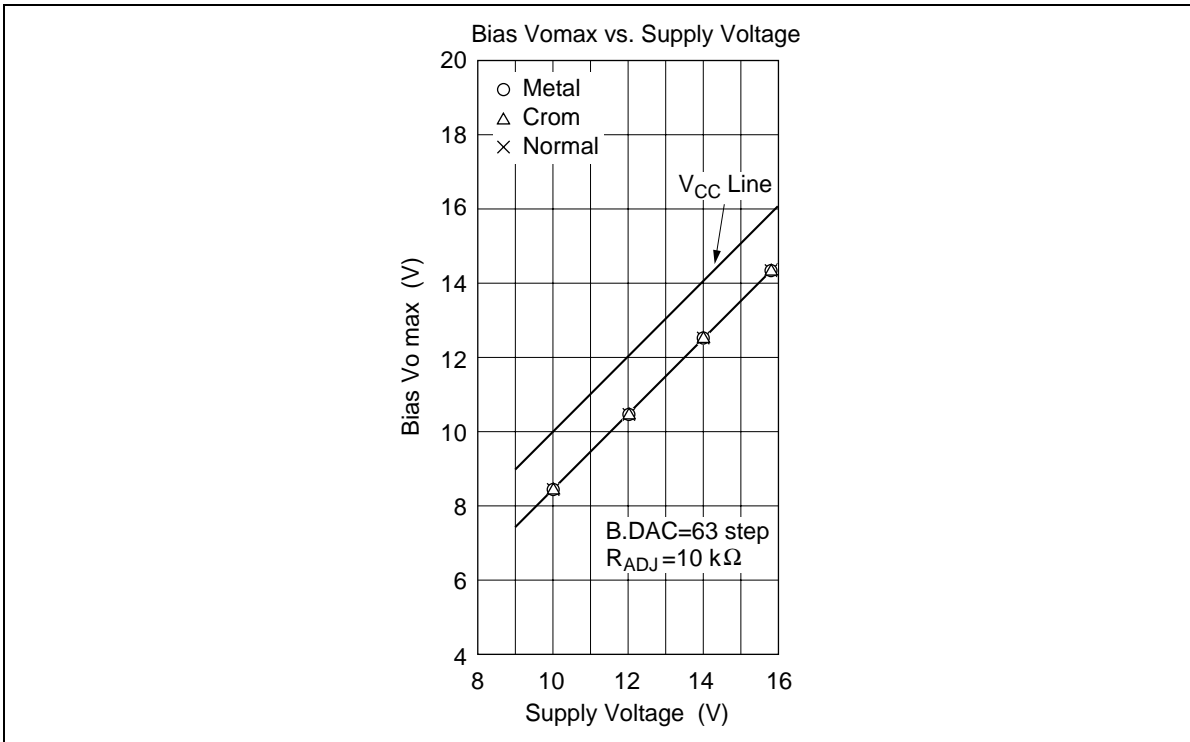


Equalizer Vo max, Vin max vs. Temperature



HA12167FB/HA12169FB

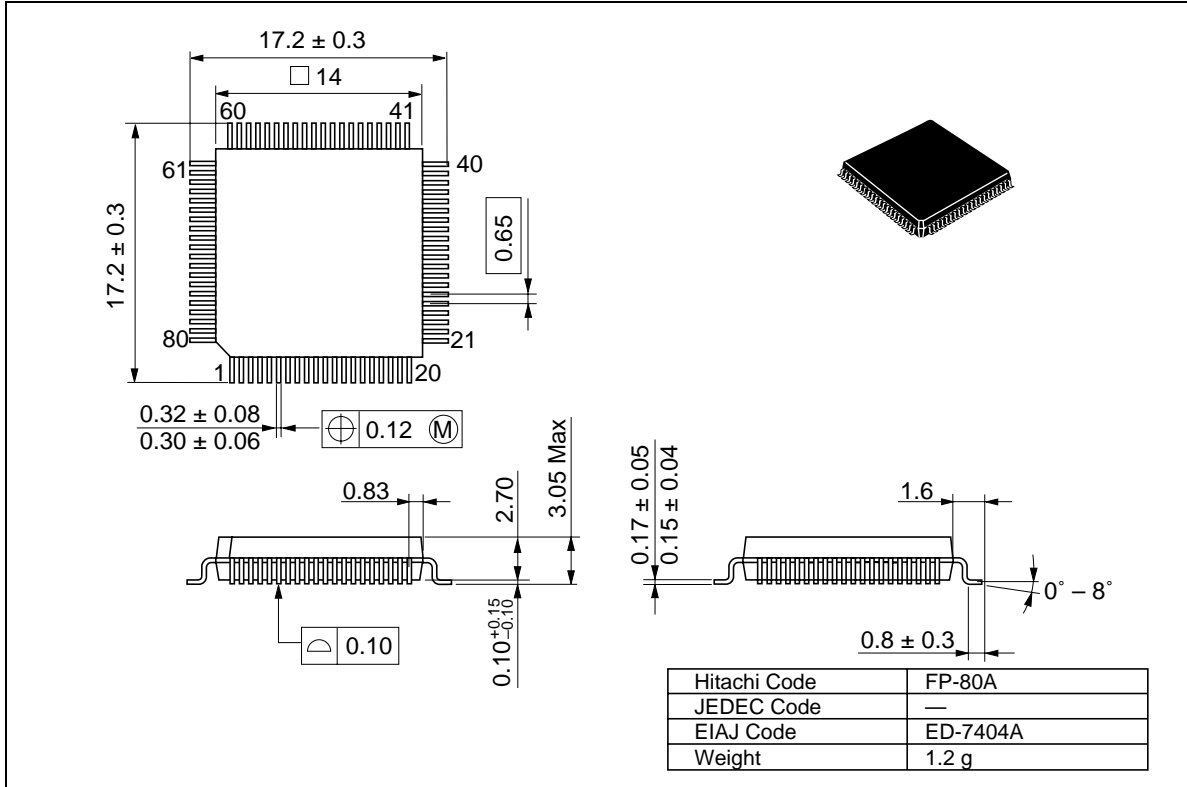




HA12167FB/HA12169FB

Package Dimensions

Unit: mm



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