PM5316/PM5310

SPECTRA-4X155 WITH TBS

REFERENCE DESIGN

PRELIMINARY

ISSUE 1: JUNE 2000

PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	June 2000	Document created.

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1 DEFINITIONS

LOS	Loss of signal - When a SONET receiver detects and all-zeros pattern for 10 microseconds or longer, this constitutes a LOS failure. It indicates that the upstream transmitter has failed. This condition is cleared when two consecutive valid frames are received.
LOF	Loss of frame - The absense of valid framing pattern for 3 microseconds leads to a LOF failure condition. This is cleared when two consecutive valid A1/A2 framing patterns are received.
ODL	Optical Data Link
ESD	ElectroStatic Discharge
AIS	Alarm indication signal - This condition can occur in response to one of the conditions above. The SONET signal format provides AISs for the line (AIS-L), STS Path (AIS-P), and VT Path (AIS-V) layers.
BER	Bit Error Rate
CRU	Clock Recovery Unit - Recovers timing information from receive data streams.
CSU	Clock Synthesis Unit - Generates timing signal for transmit data streams.

2 FEATURES

- 33 MHz CompactPCI (cPCI) interface.
- 4 HP MT-RJ OC-3 rate line side transceivers operating at 3.3V provide 622 Mbit/s aggregate operation.
- 3.3 V CMOS ADD/DROP Telecom bus interface to the TBS ADD/DROP Telecom bus interface.
- Telecom bus is configured to operate in single STS-12 (STM-4) mode at 77.76 MHz.
- CPLD performs address decoding, timing source selection and signal interfacing functions.
- Line interface speeds up to 155.52 Mbit/s.
- Enables 4XOC-3 channelization.

3 APPLICATIONS

- SONET/SDH Multiservice ADMs
- SONET/SDH Cross Connects
- SONET/SDH Terminal Multiplexers

4 REFERENCES

1. PMC-Sierra, Inc. PMC-990822, “SPECTRA-4X155 Data Sheet ”, March 2000, Issue 1.

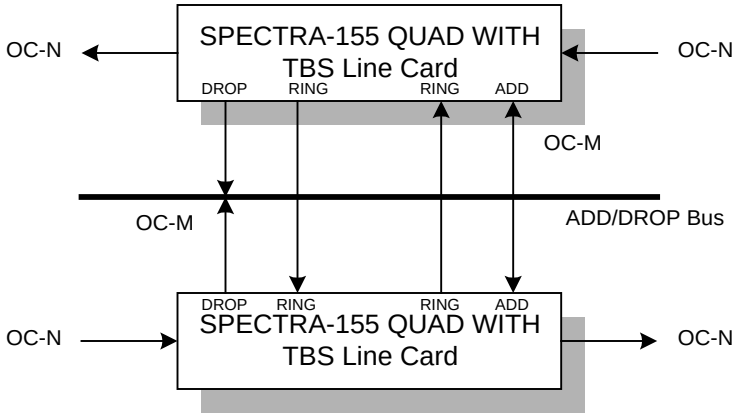
2. PMC-Sierra, Inc. PMC-990522, “TBS Telecombus Serializer”, May 1999, Issue 1.

3. PLX Technology, Inc. , “PCI 9054 Data Book v2.0”, August 1999.

5 APPLICATION EXAMPLES

The SPECTRA-4X155 WITH TBS Reference Card can be implemented as a multi-service ADM in a SONET network. Four line side OC-3 channels provide considerable flexibility for implementing SONET ring architectures. Figure 1 below outlines a typical ADM application.

Figure 1 - Add/Drop MUX.

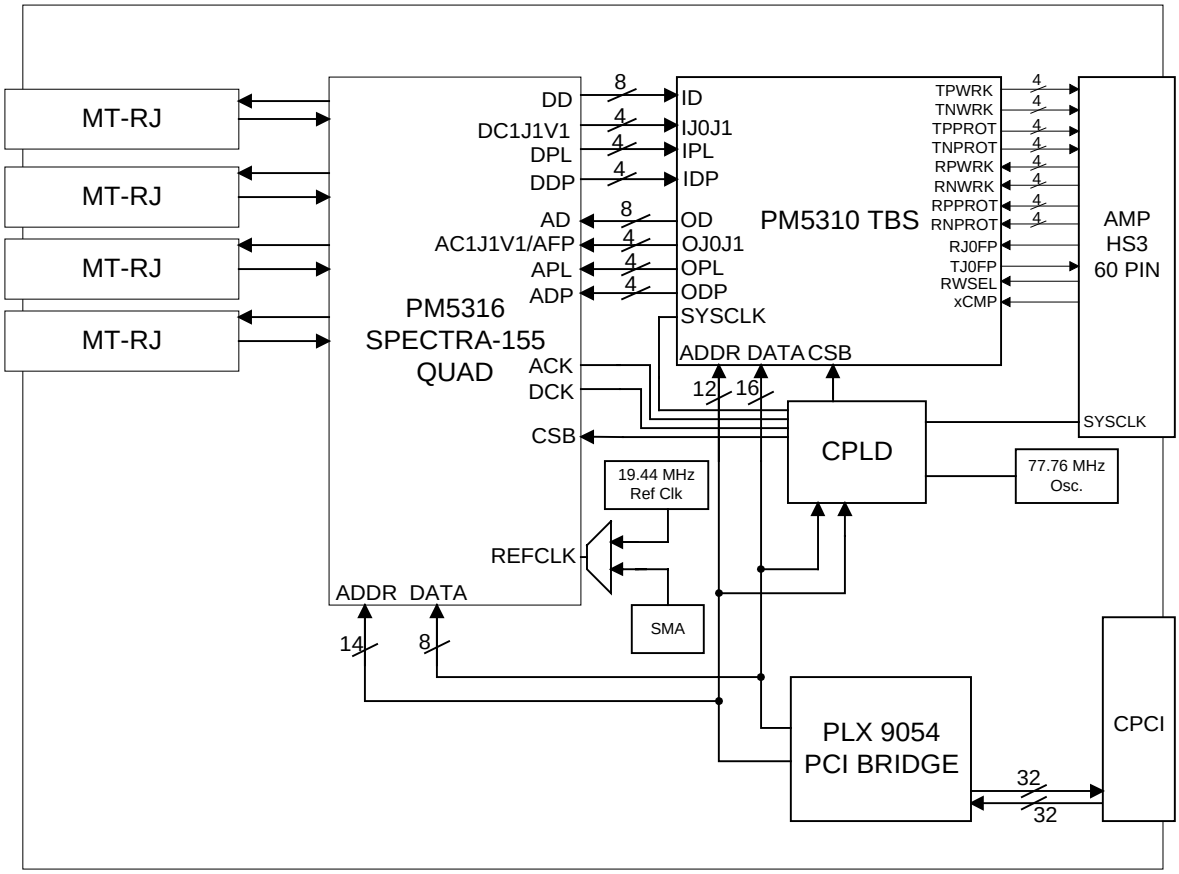


The SPECTRA-4X155 WITH TBS Line Card can also be implemented as a SONET/SDH digital cross connect. Two TBS devices on two line cards can be interfaced to create a simple switch architecture. Note that the TBS can switch at STS-1 granularity only in the parallel to serial or serial to parallel directions. A more complete digital cross-connect can be implemented utilizing the TSE as the core cross-connect element.

Additionally, the Line Card can be implemented as a Terminal Multiplexer, which is similar to the ADM, except that all incoming traffic to the card is dropped. This application would allow all four OC-3 streams to be terminated in a point-to-point network.

6 BLOCK DIAGRAM

Figure 2 - SPECTRA-4x155 Reference Design Board



7 FUNCTIONAL DESCRIPTION

The PM5316 SPECTRA-4X155 receives 4 OC-3 SONET/SDH serial bit streams from 4 Hewlett Packard MT-RJ optical transceivers and recovers clock and data. The chip processes SONET section, line, and path overhead. The 77.76 Mbit/s Telecom ADD/DROP bus on the SPECTRA-4X155 connects directly to the Telecom ADD/DROP bus on the TBS. The extracted payload from the incoming data bit stream is placed on the DROP Telecom bus and routed to the TBS in byte-serial format. The TBS receives and serializes the incoming byte-serial data stream into a bit-serial stream. The bit-serial stream is routed to the backplane via a pair of working, a pair of auxiliary, and a pair of protect 777.6 MHz LVDS serial links with 8B/10B-based encoding.

The system side of the SPECTRA-4X155 device is configured to operate in single DROP/ADD Telecombus mode at 77.76 MHz. In this mode, a single STS-12 byte-serial stream connects to the Telecom bus interface of the TBS device and only the lower 8 bits of the TBS's 32 bit parallel Telecombus are required to pass traffic.

The reference board routes signals to and from a backplane which permits further processing by other members of the CHESS chipset. For example, the S/UNI MACH48 is used to terminate ATM or bit/byte HDLC.

The system clock source is selectable between two modes. The board can provide it's own system clock via an onboard 77.76 MHz oscillator, or it can receive the clock signal through the backplane from a timing card. The SPECTRA-4X155 19.44 MHz reference clock is provided by an on board oscillator.

7.1 PM5316 SPECTRA-4X155

The PM5316 SPECTRA-4X155 SONET/SDH PAYLOAD EXTRACTOR/ALIGNER terminates the transport and path overhead of four STS-3 155 Mbit/s streams.

The SPECTRA-4X155 receives SONET/SDH frames via bit serial interfaces, recovers clock and data, and terminates the SONET/SDH section, line, and path. The SPECTRA-4X155 performs framing (A1,A2), descrambling, detects alarm conditions, and monitors section and line bit interleaved parity (BIP) (B1, B2), accumulating error counts at each level for performance monitoring purposes. The SPECTRA-4X155 interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope (virtual container).

The SPECTRA-4X155 transmits SONET/SDH frames, via bit serial interfaces. The chip performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section and line BIPs (B1, B2) as required to allow performance monitoring at the far end. In addition to its basic processing of the transmit SONET/SDH overhead, the SPECTRA-4X155 provides convenient access to all overhead bytes, which are inserted serially on lower rate interfaces, allowing additional external sourcing of overhead, if desired.

The SPECTRA-4X155 is implemented in 3.3V, CMOS process technology. It has TTL and positive ECL (PECL) compatible inputs and outputs. The SPECTRA-4X155 is configured, controlled and monitored via a generic 8-bit microprocessor bus interface and has a standard 5 signal JTAG test port for boundary scan board test purposes. The SPECTRA-4X155 is available in a 520 pin SBGA package.

7.2 PM5310 TBS

The PM5310 TBS Telecom bus serializer is a monolithic integrated circuit that implements conversions between parallel Telecom bus and the serial Telecom bus. The TBS can be used to connect SONET/SDH framer devices to ATM/POS processor devices or to cross-connect devices. The TBS can also be used to connect cross-connect devices (like the PM5372 TSE) to SONET/SDH tributary unit processors and PDH mapper devices.

The TBS connects the Parallel-Telecom Bus to three sets of four serial LVDS links called Working, Protect and Auxiliary. Transport and payload frame boundaries, pointer justification events and alarm conditions are marked with 8B/10B control characters. The read Working channel selection signal (RWSEL) determines which receive S-TCB port is forwarded to the outgoing P-TCB. Software control allows for mixing the data on the outgoing P-TCB from any of the three S-TCB ports.

The TBS is configured, controlled and monitored via a generic 16-bit microprocessor bus interface and has a standard 5 signal JTAG test port for boundary scan board test purposes. The TBS is available in a 352 pin UBGA package.

7.3 PLX Technology 9054 PCI Interface

The PLX Technology PCI9054 provides the interface between the system PCI signals and the local bus on the SPECTRA-4X155 Reference Design board. The system PCI signals are found on connector J1_1. The PCI9054 bridge provides data and address information on the local bus side, and interrupt signalling to the host processor card. The PCI9054 device is configured via a 1K-bit serial EEPROM device.

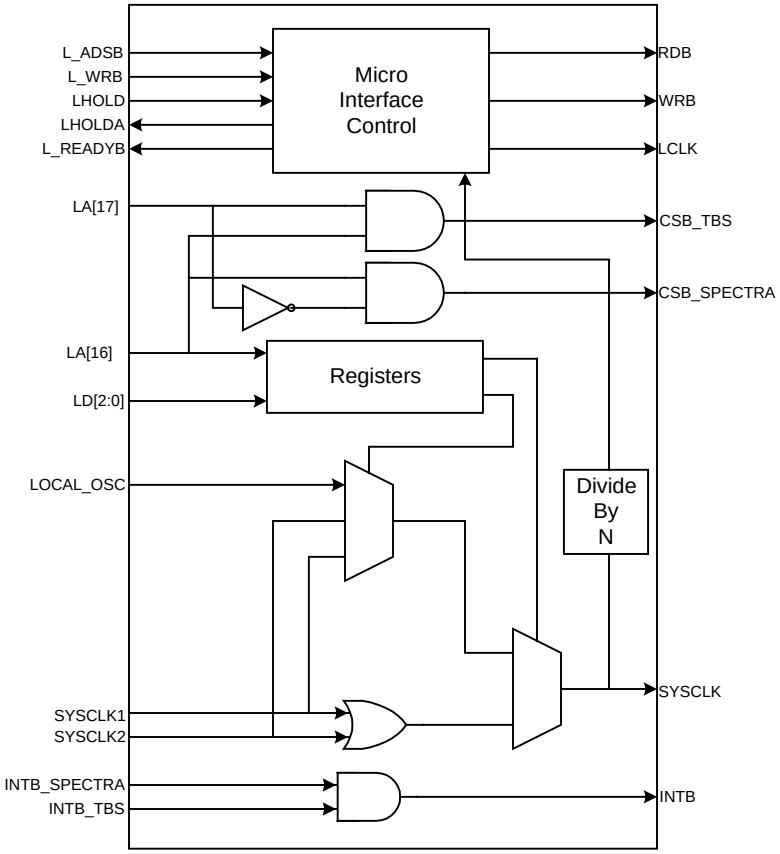
7.4 CPLD

The CPLD is used for chip select decoding for SPECTRA and TBS devices that share the LA[31..2] and LD[31..0] buses. The LA[16] and LA[17] bits are used to select the appropriate device to access. When LA[17] =1, the CPLD will have it's internal register accessed with the data on LD[0] and LD[1]. When LA[17] is 0, the RDB and WRB signals are passed and LA[16] bit is used to decode between the chip selects of the SPECTRA-4X155 and the TBS. LA[16] =0 will assert the CSB_SPECTRA signal, while LA[16] =1 asserts the CSB_TBS signal.

The internal register is used to select the clock source for SYSCLK, DCK and ACK. LD[0] selects between the backplane supplied SYSCLK signal and the onboard oscillator.

The CPLD is used to change the local read/write signal from the PCI controller (L_WRB) into two separate signals for the microprocessor interface signals RDB and WRB. The CPLD acts as a buffer for the non-LVDS signals that come in from the backplane and can show debugging information with 8 LEDs. Some of the overhead signals from the SPECTRA_4X155 are routed to the CPLD for debugging/overhead monitoring. Figure 3 details the functions of the CPLD.

Figure 3 - CPLD Functional Block Diagram



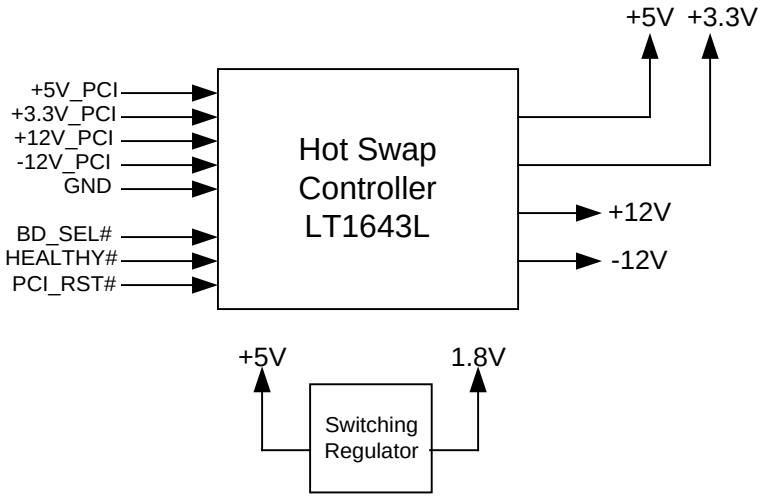
7.5 Clocks

The 77.76 MHz system clock signal for the TBS and ACK and DCK Telecom bus clocks for the SPECTRA-4X155 can be configured in two ways: from an on-board 77.76 MHz oscillator or from the backplane.

The SPECTRA-4X155 19.44 MHz reference with a balance of ± 20 ppm is supplied by either a 19.44 MHz oscillator or optionally the reference clock can be supplied externally through a SMB connector.

7.6 Power Supply

Figure 4 - Power Supply System Block.



The Power Block provides stable voltage supplies delivered over the CompactPCI backplane from a centralized power supply. Voltage levels of +5V, +3.3V, +12V, -12V and regulated 1.8V are available from this block.

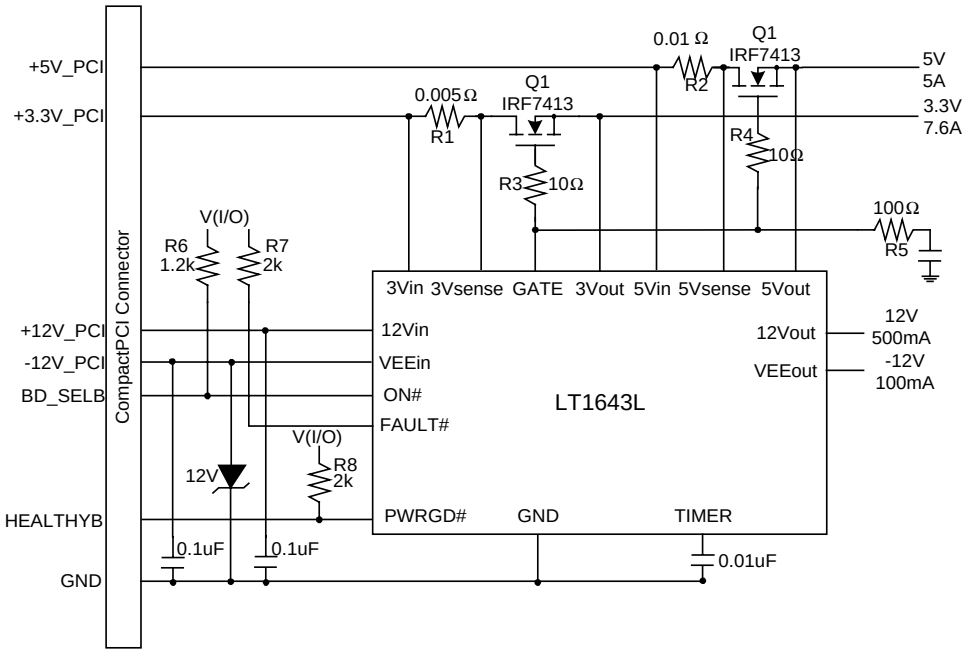
7.6.1 Voltage Regulators

Linear regulators supply the 3.3V analog and 1.8V analog pins of the SPECTRA-4X155 and TBS devices respectively. These regulators are located on the power sheets of the SPECTRA-4X155 and the TBS. The 5V to 1.8V switching regulator module is used to generate the supply labelled 1.8V. Only the TBS uses this supply.

7.6.2 Hot Swap Controller

The Hot Swap Controller is used to allow the board to be safely inserted or removed from a live cPCI slot. External N-channel MOSFETS control the 3.3V and 5V supplies, while the +12V and –12V supplies are controlled with on-chip switches. The supply voltages are ramped up at a programmable rate. The hot swap controller is implemented using the Linear Technology LTC1643L. A typical cPCI Hot Swap circuit is shown below in Figure 2. Note that only the hot swap controller is implemented in the power block. Additional Hot Swap circuitry including the precharge circuitry for the cPCI bus is included in the CompactPCI block.

Figure 5 - cPCI Hot Swap Circuit



The 3.3V, 5V, +12V, and –12V power supplies are generated from the medium length power pins on the PCI connector (+5V_PCI, +3.3V_PCI, etc). The long power pins which make the first connections are used to generate a 1V precharge voltage on the cPCI bus pins.

In the circuit above, the 3.3V and 5V power supplies are controlled by the N-channel pass transistors Q1 and Q2. Internal circuitry controls the +/-12V rails. R1 and R2 control overcurrent conditions. R5 and C1 provide current control loop compensation. R3 and R4 prevent high frequency oscillations in the pass transistors. Finally, the 12V Zener diode protects against power surges on the –12V rail.

During an insertion and power-up sequence, the BD_SEL# pin is the final pin to connect to the board. This pin is connected to the ON# pin of the Hot Swap Controller. When the ON# pin is pulled low, the pass transistors are turned on by pulling the GATE pin high, and the current in each pass transistor rises at a rate of dv/dt = 50μA/C1, until reaching the preset limit. If there is a high load capacitance, the rate of increase will be controlled by this value. Once the supply voltages stabilize the PWRGD# signal is pulled low.

The sense resistors R1 and R2 in Figure 5 above set the current limit for the 5V and 3.3V supplies. The current limit is governed by the following equation:

$$I_{\lim} = 53mV / R_{sense}$$

In the circuit of Figure 4 above, the 3.3V current limit will be 10.6A, and the 5V limit will be 5.3A.

Upon removal, the /ON pin will be pulled high, and the GATE pin on the pass transistors is pulled low to prevent load currents on the 3.3V and 5V rails from instantaneously going to zero and glitching the power supply. The /PWRGD pin is pulled high if any of the supply voltages moves below its threshold.

7.7 System Interface

This board is based on the cPCI 6U (233.35mm by 160mm) board size. The J1_1 connections are standard cPCI pinouts and the connector carries 32 standard cPCI signals. The other connectors implemented in this reference design are the AMP HS3 60 pin connectors. These connectors are used to connect the 777.6 Mbit/s LVDS signals and control signals to the backplane. Note that the columns of the connector are separated by ground planes. Column 10 of the HS3 connector does not have ground shielding on the outer side, therefore low speed signals are placed in this column. The pin assignments are made in the low-noise configuration as specified by AMP. The table on the following page outlines the HS3 pinout.

Table 1 - Working and Protect HS3 Connector Pinout

Column	A	B	C	D	E	F
1	GND	SYSCLK1P	SYSCLK1N	SYSCLK2 P	SYSCLK2N	GND
2	GND	RPPROT4	RNPROT4	TPPROT4	TNPROT4	GND
3	GND	RPPROT3	RNPROT3	TPPROT 3	TNPROT3	GND
4	GND	RPPROT2	RNPROT2	TPPROT2	TNPROT2	GND
5	GND	RPPROT1	RNPROT1	TPPROT1	TNPROT1	GND
6	GND	RPWRK4	RNWRK4	TPWRK4	TNWRK4	GND
7	GND	RPWRK3	RNWRK3	TPWRK3	TNWRK3	GND

Column	A	B	C	D	E	F
8	GND	RPWRK2	RNWRK2	TPWRK2	TNWRK2	GND
9	GND	RPWRK1	RNWRK1	TPWRK1	TNWRK1	GND
10-	GND	TJ0FP_OUT	RJ0FP_IN	RWSEL_IN	XCMP_IN	GND

Table 2 - Auxiliary HS3 Connector Pinout

Column	A	B	C	D	E	F
1	GND	GND	GND	GND	GND	GND
2	GND	GND	GND	TNAUX4	TPAUX4	GND
3	GND	GND	GND	TNAUX3	TPAUX3	GND
4	GND	GND	GND	TNAUX2	TPAUX2	GND
5	GND	GND	GND	TNAUX1	TPAUX1	GND
6	GND	GND	GND	GND	GND	GND
7	GND	GND	GND	RNAUX4	RPAUX4	GND
8	GND	GND	GND	RNAUX3	RPAUX3	GND
9	GND	GND	GND	RNAUX2	RPAUX2	GND
10	GND	GND	GND	RNAUX1	RPAUX1	GND

8 IMPLEMENTATION DESCRIPTION

This section describes the hardware implementation of the SPECTRA-4X155 WITH TBS reference design. Each section references the schematics contained in Section 9.

8.1 Root Drawing, Page 1

This page shows the interconnection between the functional blocks of the design.

8.2 Optics Block, Page 2

Page 2 shows the optical interface of the reference design. Four HP HFCT-5905E MT-RJ Duplex single mode transceivers are used to transmit and receiver four OC-3 optical streams. The HFCT-5905E is a 3.3 V PECL device in a 10-pin package. The PECL signals are connected to the SPECTRA-4X155 receive and transmit pins through 50 ohm controlled impedance lines. The receive and transmit lines are properly terminated at the SPECTRA-4X155 and transceiver devices. The 150 ohm resistors provide source terminations for the PECL outputs from the ODL and should be placed as close as possible to the ODL. The resistor and capacitor networks between the TXDP and TXDN lines provide biasing for the SPECTRA-4X155 PECL TX outputs and should also be placed close to the ODL.

8.3 Spectra-4x155 Block, Pages 3,4,5,6 & 7

The SPECTRA_4x155_BLOCK shows the SPECTRA-4X155 signals and power circuitry.

Page 3 contains Block 1 of the SPECTRA-4X155 device. Block 1 contains the line side signals of the SPECTRA-4X155. The PECL receive lines have parallel termination resistors of 100 ohms. The transmit differential TTL outputs have series capacitors of 0.1 uF to remove any DC component of the output signal and the 158 ohm resistors are used to bring the signals to PECL signaling levels. 0.22 uF capacitors are used for the loop filter pins, CP and CN. The PECLV pin is pulled to ground to select 3.3 V optics.

The REFCLK source must be a 19.44 MHz ±20ppm clock signal. By means of header J4, the clock source can be selected between an on-board oscillator or from an external source via a SMB connector.

Page 4 contains Blocks 2 and 3 of the SPECTRA-4X155 device. Blocks 2 and 3 of the SPECTRA-4X155 contain the ADD/DROP Telecom bus signals. The DROP bus data signals DROP_DATA[7:0] contain the STS-3/3c received SONET/SDH payload data of all four channels. The DROP bus data signals DROP_DATA[31:8] are left floating because no data will be delivered via these bits. Similarly, for single ADD bus interface, the ADD bus data signals ADD_DATA[7:0] contain the STS-3/3c SONET/SDH payload data to transmit on the four channels. The ADD bus data signals ADD_DATA[31:8] are pulled low to prevent noise triggering these signals as these inputs will not receive any data. Header J9 provides access to the TPAIS, TPAISCK, TPAISFP, DPAIS, DPAISCK, and DPAISFP signals.

Page 5 contains Block 4 of the SPECTRA-4X155 device. Block 4 contains the microprocessor and JTAG signals. JTAG is not implemented in this design therefore the pins are pulled-up to maintain appropriate signal state.

Page 6 contains Block 5 of the SPECTRA-4X155 device. Block 5 of the SPECTRA-4X155 device contains the transmit and receive overhead signals. All of the signals are routed to a 32X2 pin header for access. The four SALM signals are routed off-page to the CPLD for alarm indication. The transmit inputs are pulled-low to prevent noise triggering of the signals. The Ring Control signals are routed to a matched impedance connector for debugging.

Page 7 contains Block 6 of the SPECTRA-4X155 device. Block 6 contains the power pins for the SPECTRA-4X155. 20 of the 48 digital power pins have 0.1 uF decoupling capacitors placed as close as possible to the pins as well as 10uF bulk capacitors. The receive and transmit analog power pins are filtered via RC filters to provide a clean 3.3 voltage to the pins. VBIAS pins (VBIAS<1..0>) are tied to the 3.3V supply via a 1KΩ resistor since there are no 5V devices on the board.

The 3.3V regulator shown on this page is also used to supply the optics.

8.4 TBS Block, Pages 8, 9,10, & 11

The TBS_BLOCK shows the TBS signals and power circuitry.

Page 8 contains Block 1 of the TBS device. Block 1 shows the system side LVDS signals of the TBS. These signals are received from and transmitted to the backplane. The LVDS are differential signals and the transmission traces must be 50 ohm controlled impedance lines. The TCMP and OCMP (connection memory page) signals are buffered by the CPLD and sourced from the backplane. The SYSCLK is sourced from either an on-board 77.77 MHz oscillator or an external 77.76 MHz clock signal.

Page 9 contains Blocks 2 and 3 of the TBS device. Blocks 2 and 3 contain the ADD/DROP Telecom bus signals which interface the TBS to the SPECTRA-4X155. Because the SPECTRA-4X155 Telecom bus is configured to operate in single-drop mode, only OD1[7:0] and ID1[7:0] data bits are used. Outgoing (ADD) Telecom bus channels OD2 to OD4 are left unconnected as well as their respective ODP, OPL, OJ0J1, OPAIS, OTV5, OTPL, OTAIS, and OCOUT signals. The OPAIS, OTV5, OTPL, OTAIS, and OCOUT for channel one are routed to a header for access. Incoming (DROP) Telecom bus channels ID2 to ID4 are pulled low to prevent noise triggering the signals as well as their respective IDP, IPL, IJ0J1, IPAIS, ITV5, ITPL, and ITAIS signals. Signals IPAIS, ITV5, ITPL, and ITAIS for channel one are routed to a header for access.

Page 10 contains Block 4 of the TBS device. Block 4 contains the microprocessor and JTAG signals. JTAG is not implemented in this design therefore the pins are pulled-up to maintain appropriate signal state.

Page 11 contains Block 5 of the TBS device and a regulated 1.8V supply. Block 5 contains the power pins for the TBS. Both the 3.3 Volt and the 1.8 Volt supply rails are decoupled via 0.1 uF capacitors as well as 10uF bulk capacitors. The supply to the CSU_AVDH pin is passed through an RC filter to provide a clean voltage to the pin. The RES and RESK pins are externally attached via a 3.16K resistor. The 1.8V regulator shown on this page is used to supply the 1.8V analog pins on the TBS device.

8.5 System Interface Block, Page 12

The SYS_INTERFACE_BLOCK contains the AMP HS3 connectors for transfer of the LVDS signals between the backplane and the reference board. The transmit and receive differential pairs are grouped together on the connector. The top HS3 connector contains the LVDS working and protect differential signals. The differential SYSCLK signals generated on the TSE reference board are also sent through the top connector. The bottom connector is used strictly for the LVDS auxiliary channels. This connector is optional and can be populated depending on the application requirements. All of the LVDS signal traces and the differential SYSCLK traces are 50 ohm controlled impedance lines.

8.6 CPLD Block, Page 13

The CPLD_BLOCK shows the signal connections to and from the Xilinx XC9572XL CPLD. The CPLD is used for address decoding, microprocessor access control, signal conversion, signal buffering, and clock distribution.

The PECL differential clock signals, SYSCLK1(P,N) and SYSCLK2(P,N), are translated into single-ended TTL signals using the Motorola MC100EPT23 device. A 77.76 MHz local oscillator signal is also input to the CPLD. Through

software control, the CPLD can select which of the clock sources is to be used and sends the selected signal to the Pericom 49FCT3807 clock driver device. The 49FCT3807 clock distributes the 77.76 MHz signal to the SYSCLK input on the TBS as well as to the DCK and ACK Telecom bus clocks on the SPECTRA-4X155.

The Maxim 811 power supply monitor device with reset provides manual reset capability with a push-button switch attached to the master reset input. The Motorola MC74HC244 driver/buffer chip is used to drive the Lumex LXH5147 LED arrays. The LED's can be programmed to display the status of alarms from the SPECTRA-4X155 device or to display information for debugging. The microprocessor interrupt lines are also routed to the LED's for device interrupt status.

Header J1 provides an interface to the CPLD JTAG pins for programming the device.

8.7 cPCI Block, Pages 14 & 15

The CPCI_BLOCK shows the PLX 9054 signal and power circuitry connections.

The PCI9054 is a 3.3V/5V compliant PCI v2.2 32-bit, 33MHz Bus Master Interface Controller, that provides flexible local bus configurations and Hot Swap capability.

The 32 bit multiplexed address/data bus and associated control lines connect directly from the CPCI J1_1 connector to the PLC PCI9054 interface device. The bus and control lines are terminated with 10 ohm stub resistors that should be placed close to the J1_1 connector pins.

The PCI 9054 operates with a 32-bit non-multiplexed bus (C-mode) on the local bus side. The lower two bits of the address lines are used for 16 or 8 bit byte access but are unused in this application.

A serial EEPROM is required for device configuration after reset or at power-up. The Fairchild Semiconductor NM93CS46 serial EEPROM is used to program the 9054.

8.8 Power Block, Page 16

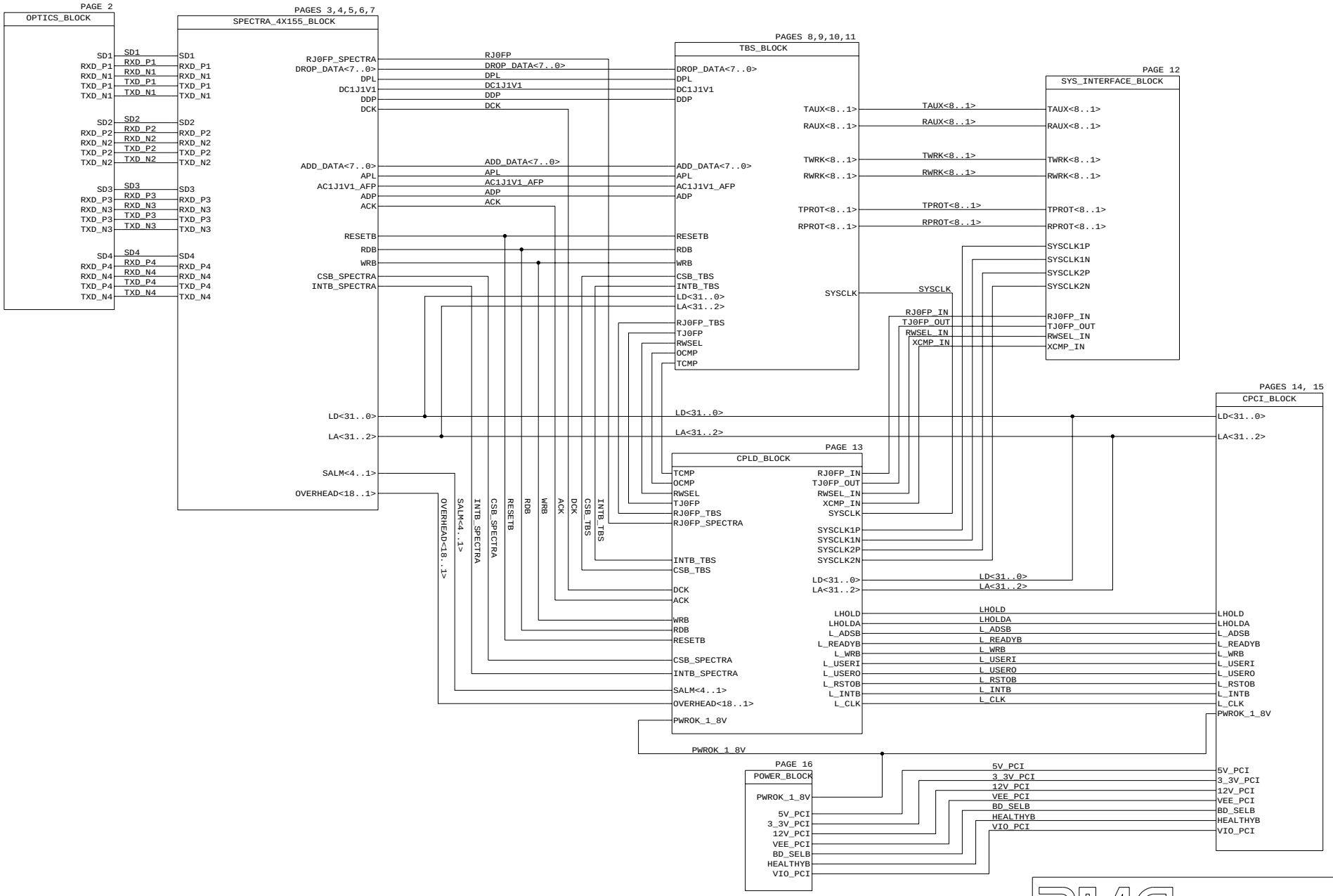
The POWER_BLOCK shows the power signal connections, the Hot-Swap Controller, and voltage regulator connections.

The Power Supply System Block provides stable voltage supplies delivered over the CompactPCI backplane from a centralized power supply. Voltage levels of +5V, +3.3V, +12V, -12V and a regulated 1.8V are provided.

A voltage regulator is provided in the Power Supply System Block. The 1.8V switching regulator generates the core digital power supply required for the TBS device. The 3.3V SPECTRA devices are powered directly from the digital sections of the hot swap controller.

9 SCHEMATICS AND LAYOUT

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

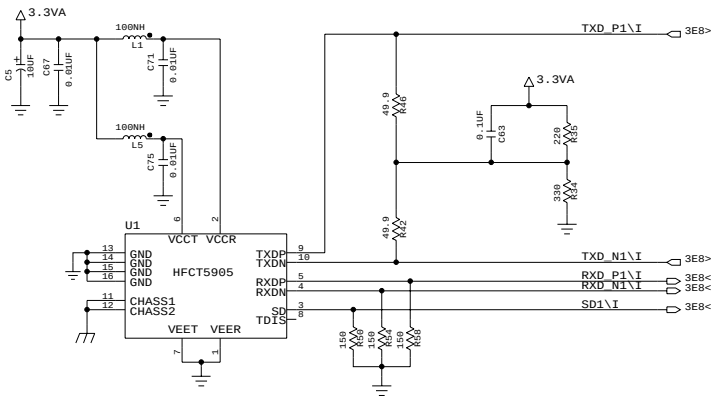


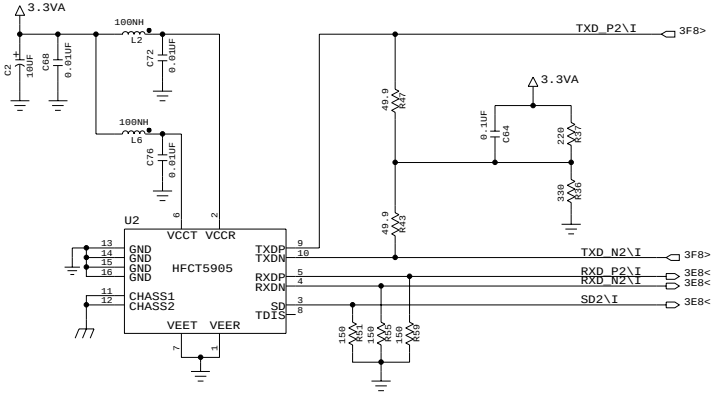
DRAWING:
TITLE=SPECTRA_4X155_ROOT
LAST_MODIFIED=Thu Jun 15 09:37:04 2000

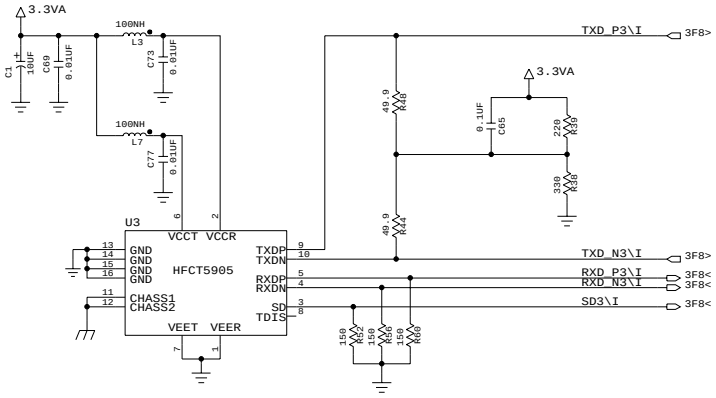
PMC-Sierra, Inc.

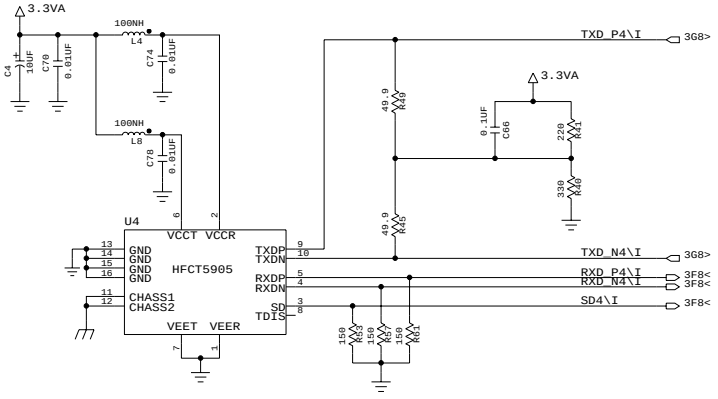
DOCUMENT NUMBER: PMC-991245 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 00/06/09
TITLE: SPECTRA 4X155 REFERENCE DESIGN ROOT_DIAGRAM	REVISION NUMBER: 1
ENGINEER: MB	PAGE:1 OF 16

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR







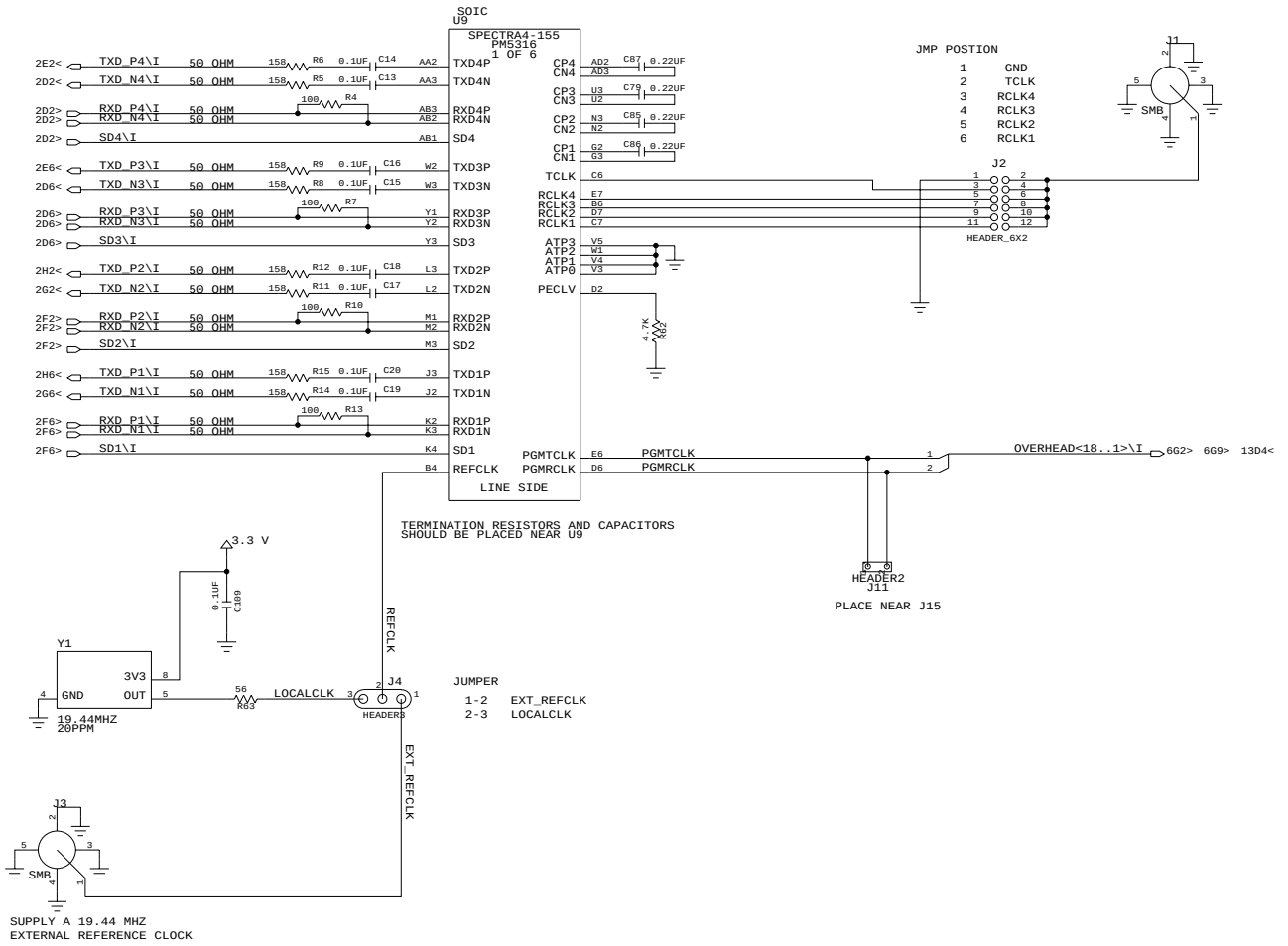


DRAWING:
TITLE=OPTICS_BLOCK
LAST_MODIFIED=Thu Jun 15 10:02:29 2000

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991245 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 00/06/09
TITLE: SPECTRA 4X155 REFERENCE DESIGN OPTICS_BLOCK	REVISION NUMBER: 1
ENGINEER: MB	PAGE:2 OF 16

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

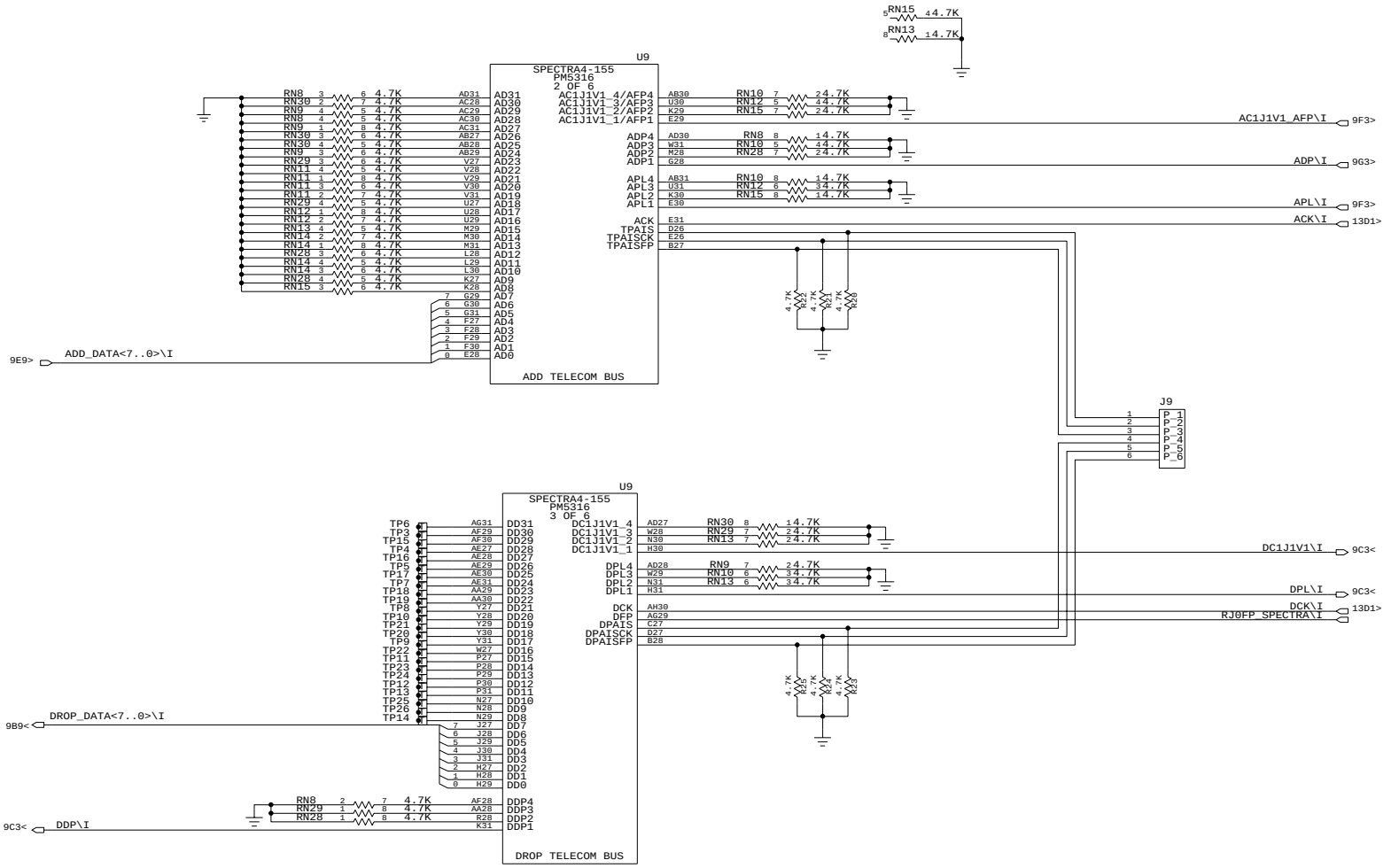


DRAWING:
TITLE=SPECTRA_4X155_BLOCK
LAST_MODIFIED=Thu Jun 15 10:02:32 2000

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991245 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 00/06/09
TITLE: SPECTRA 4X155 REFERENCE DESIGN SPECTRA_4X155_BLOCK	REVISION NUMBER: 1
ENGINEER: MB	PAGE:3 OF 16

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

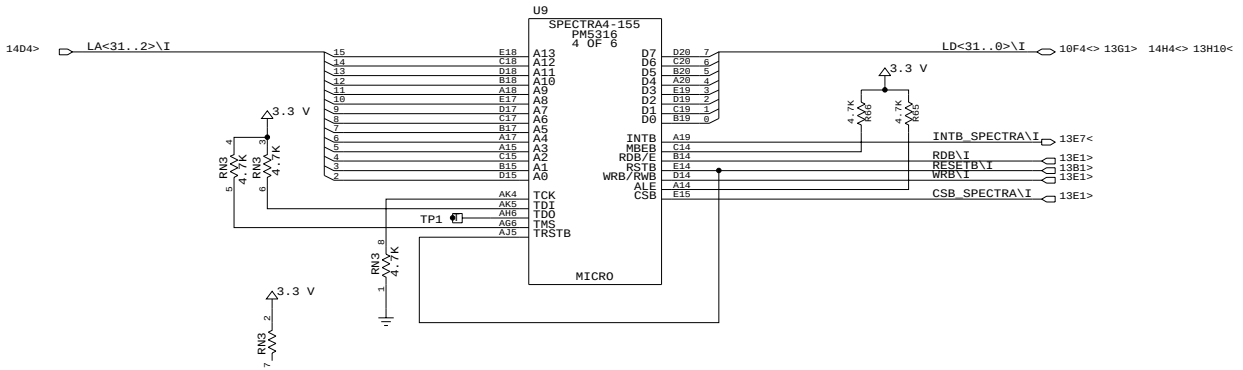


DRAWING:
TITLE=SPECTRA_4X155_BLOCK
LAST_MODIFIED=Thu Jun 15 10:02:36 2000

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991245 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 00/06/09
TITLE: SPECTRA 4X155 REFERENCE DESIGN SPECTRA_4X155_BLOCK	REVISION NUMBER: 1
ENGINEER: MB	PAGE:4 OF 16

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

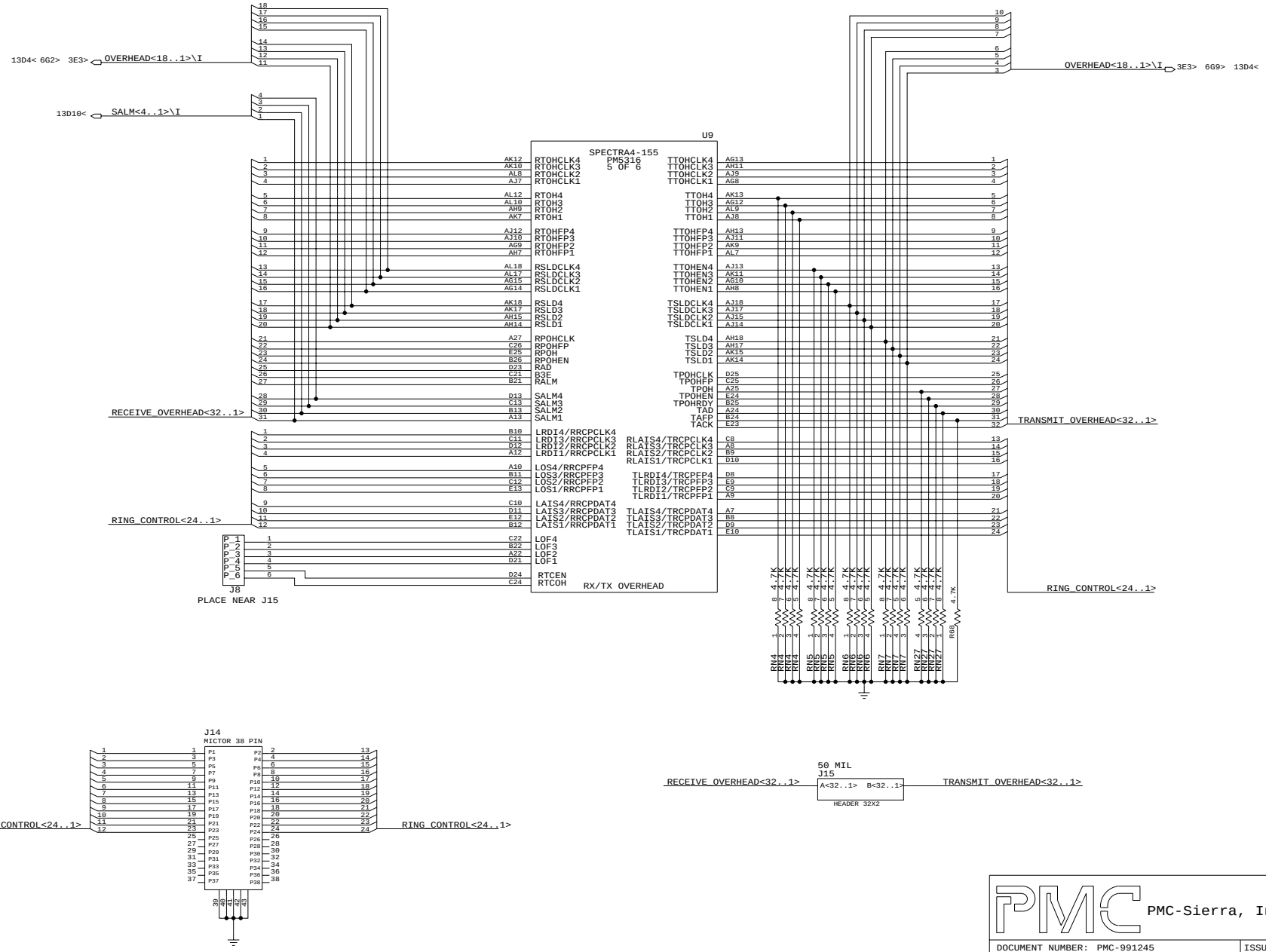


DRAWING:
TITLE=SPECTRA_4X155_BLOCK
LAST_MODIFIED=Thu Jun 15 10:02:38 2000

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991245 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 00/06/09
TITLE: SPECTRA 4X155 REFERENCE DESIGN SPECTRA_4X155_BLOCK	REVISION NUMBER: 1
ENGINEER: MB	PAGE:5 OF 16

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

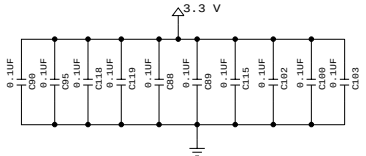


PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991245 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 00/06/09
TITLE: SPECTRA 4X155 REFERENCE DESIGN SPECTRA_4X155_BLOCK	REVISION NUMBER: 1
ENGINEER: MB	PAGE:6 OF 16

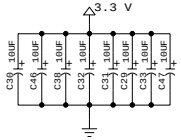
DRAWING:
TITLE=SPECTRA_4X155_BLOCK
LAST_MODIFIED=Thu Jun 15 10:02:11 2000

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

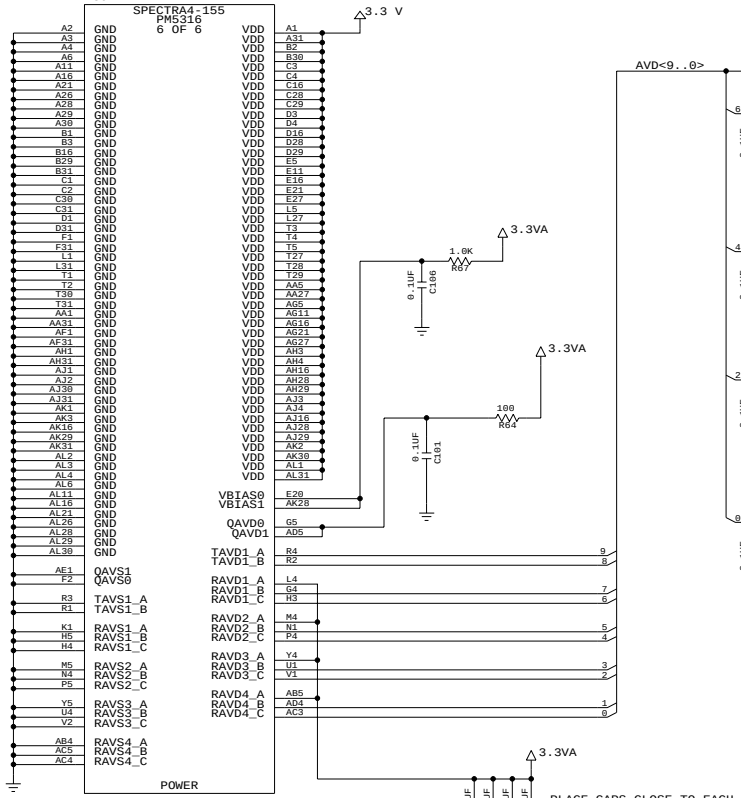


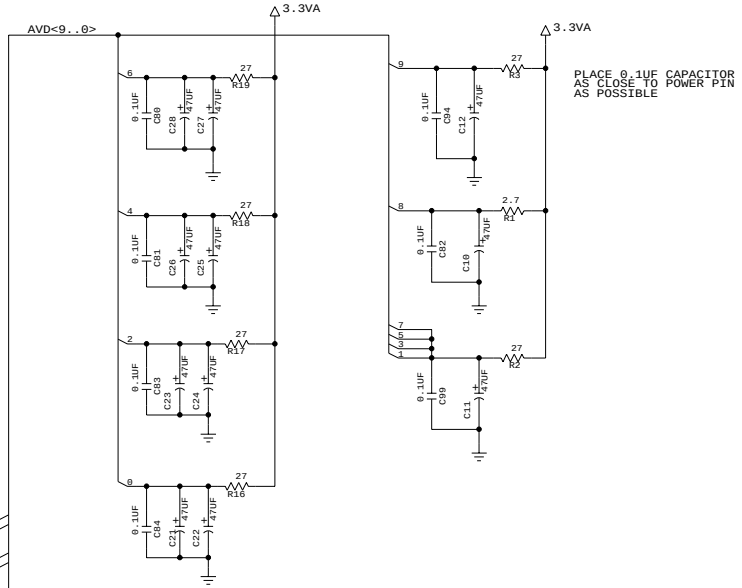
PLACE DECOUPLING CAPS
CLOSE TO THE FOLLOWING PINS:

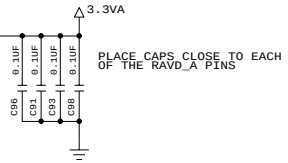
B30	T4
B2	AA27
D28	AA5
D16	AG21
D4	AG11
E21	AH28
E11	AH16
L27	AH4
L5	AK30
T28	AK2

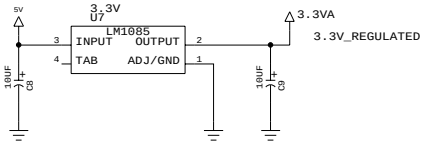


PLACE 2 PER EDGE
AROUND SPECTRA 4X155







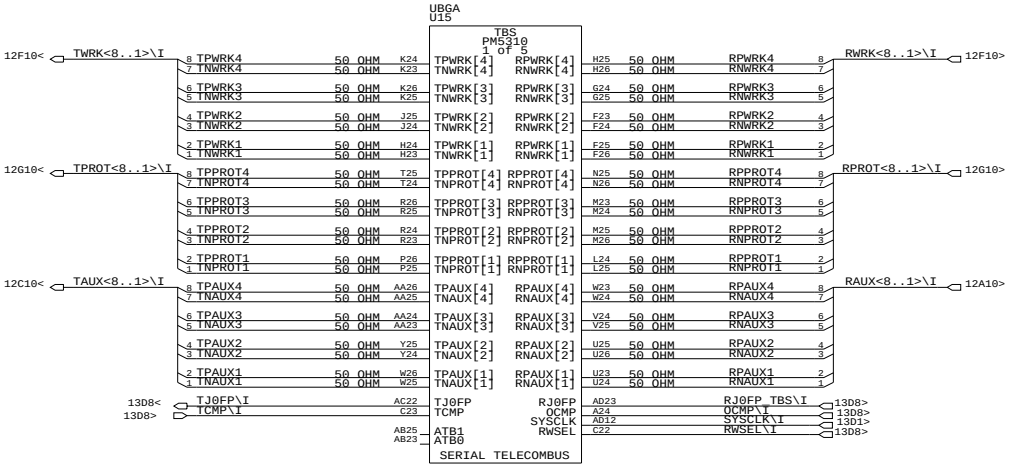


DRAWING:
TITLE=SPECTRA_4X155_BLOCK
LAST_MODIFIED=Thu Jun 15 10:02:46 2000

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991245 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 00/06/09
TITLE: SPECTRA 4X155 REFERENCE DESIGN SPECTRA_4X155_BLOCK	REVISION NUMBER: 1
ENGINEER: MB	PAGE:7 OF 16

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

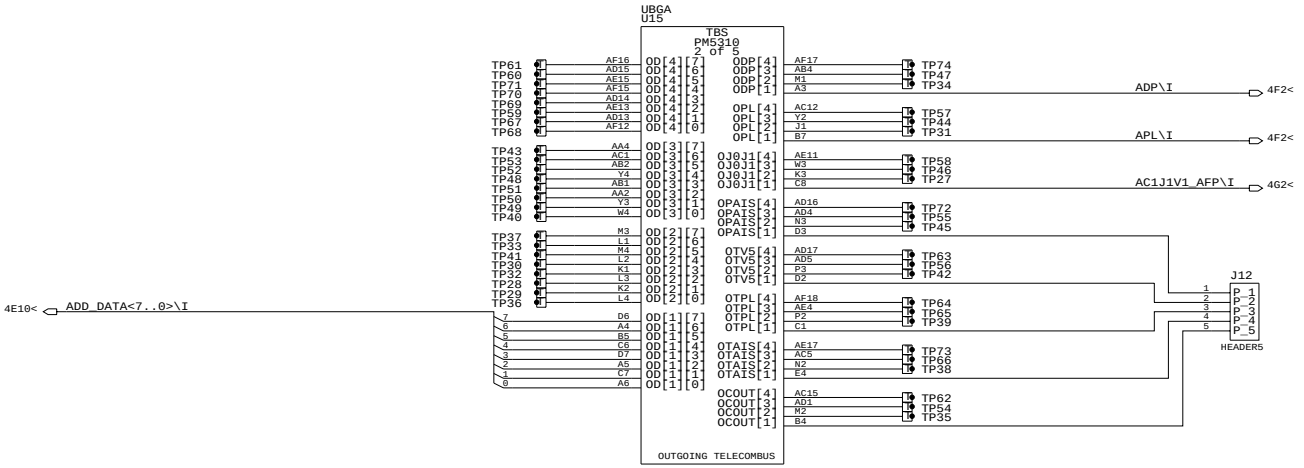


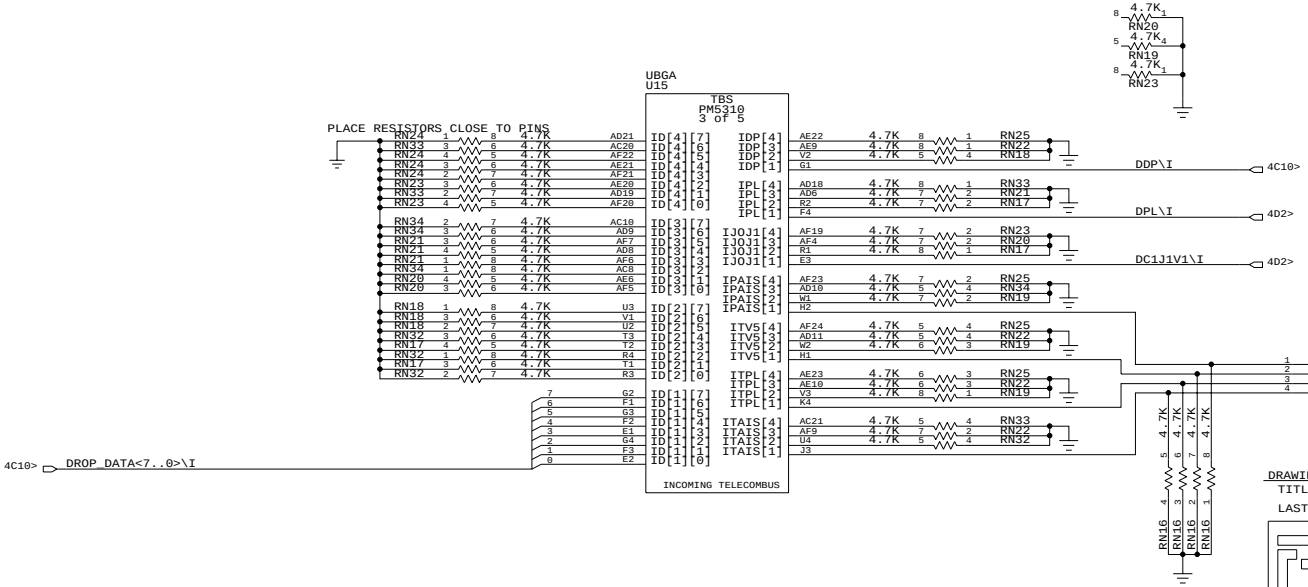
DRAWING:
TITLE=TBS_BLOCK
LAST_MODIFIED=Thu Jun 15 10:02:48 2000

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991245 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 00/06/09
TITLE: SPECTRA 4X155 REFERENCE DESIGN TBS_BLOCK	REVISION NUMBER: 1
ENGINEER: MB	PAGE:8 OF 16

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



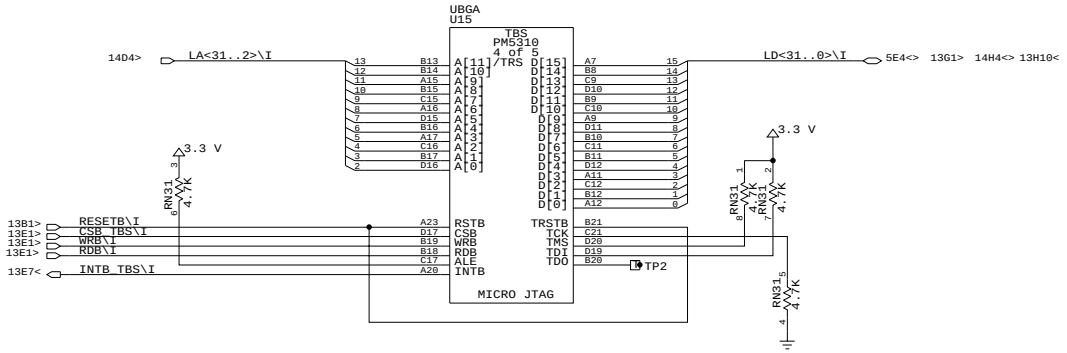


DRAWING:
TITLE=TBS_BLOCK
LAST_MODIFIED=Thu Jun 15 10:02:52 2000

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991245 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 00/06/09
TITLE: SPECTRA 4X155 REFERENCE DESIGN TBS_BLOCK	REVISION NUMBER: 1
ENGINEER: MB	PAGE:9 OF 16

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

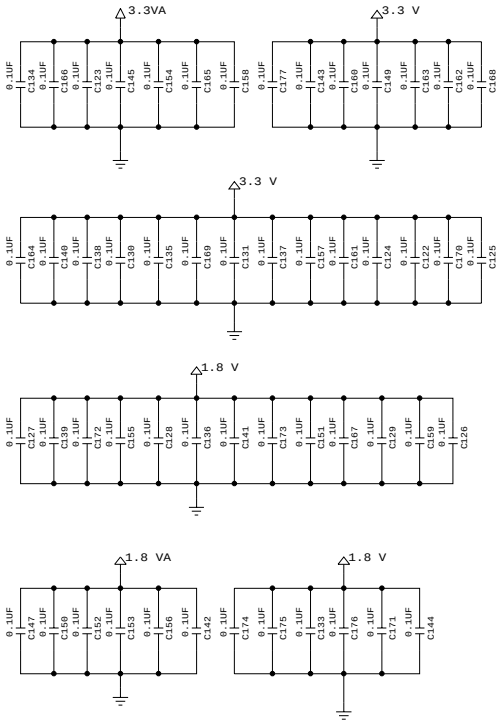


DRAWING:
TITLE=TBS_BLOCK
LAST_MODIFIED=Thu Jun 15 10:02:55 2000

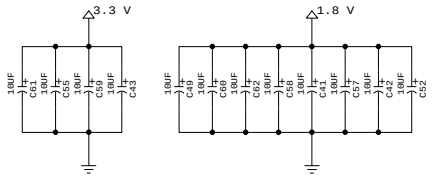
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991245 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 00/06/09
TITLE: SPECTRA 4X155 REFERENCE DESIGN TBS_BLOCK	REVISION NUMBER: 1
ENGINEER: MB	PAGE:10 OF 16

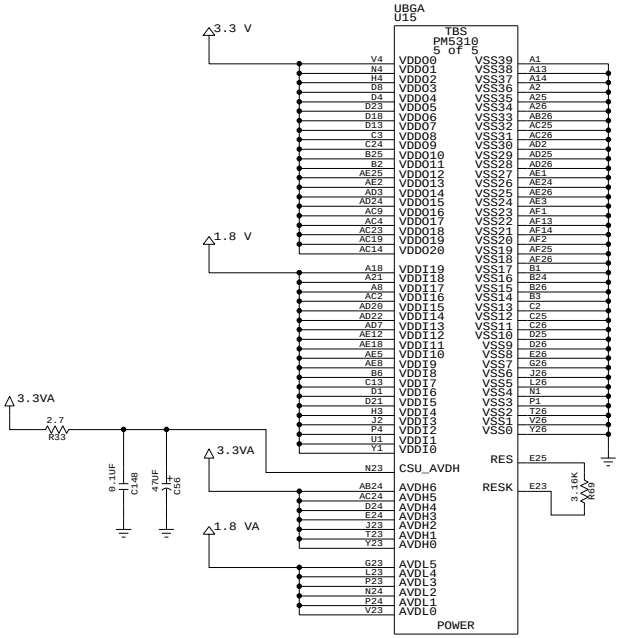
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

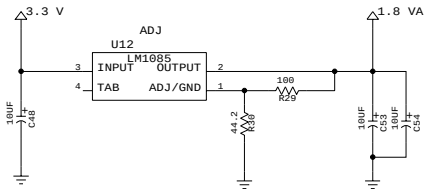


PLACE DECOUPLING CAPS
CLOSE TO EACH POWER PIN



PLACE 3 PER EDGE
AROUND TBS





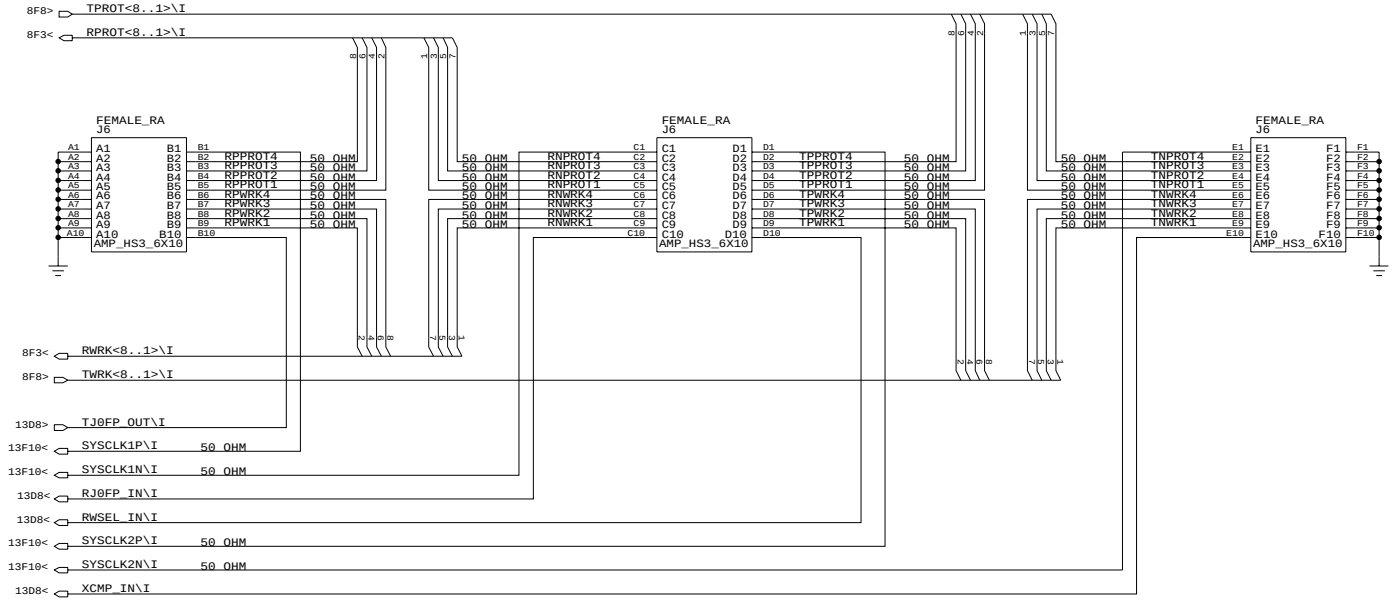
DRAWING:
TITLE=TBS_BLOCK
LAST_MODIFIED=Thu Jun 15 10:02:58 2000

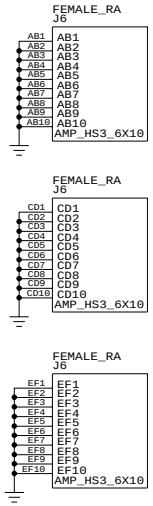
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991245 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 00/06/09
TITLE: SPECTRA 4X155 REFERENCE DESIGN TBS_BLOCK	REVISION NUMBER: 1
ENGINEER: MB	PAGE:11 OF 16

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

WORKING AND PROTECT LVDS LINKS

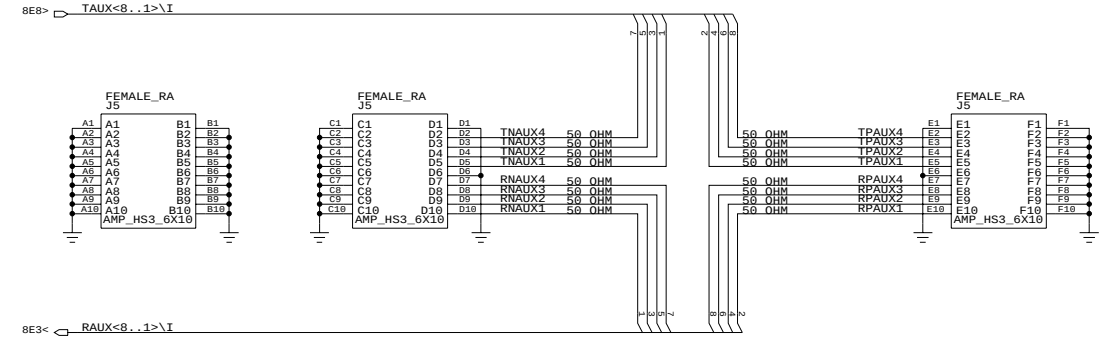


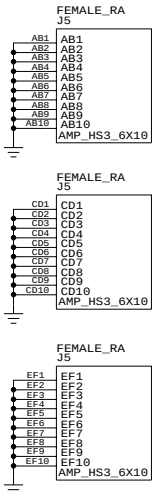


TPROT<8..1>, TWRK<8..1>, RWRK<8..1>, RPROT<8..1>, TAUX<8..1> AND RAUX<8..1> CONSIST OF DIFFERENTIAL LVDS PAIRS. EACH PAIR SHOULD BE ROUTED TOGETHER ON THE SAME LAYER AND HAVE THE SAME LENGTH. ALL LVDS TRACES SHOULD BE 50 OHM.

AUXILLARY LVDS LINKS

DO NOT POPULATE CONNECTOR IF AUXILLARY LVDS LINKS NOT REQUIRED



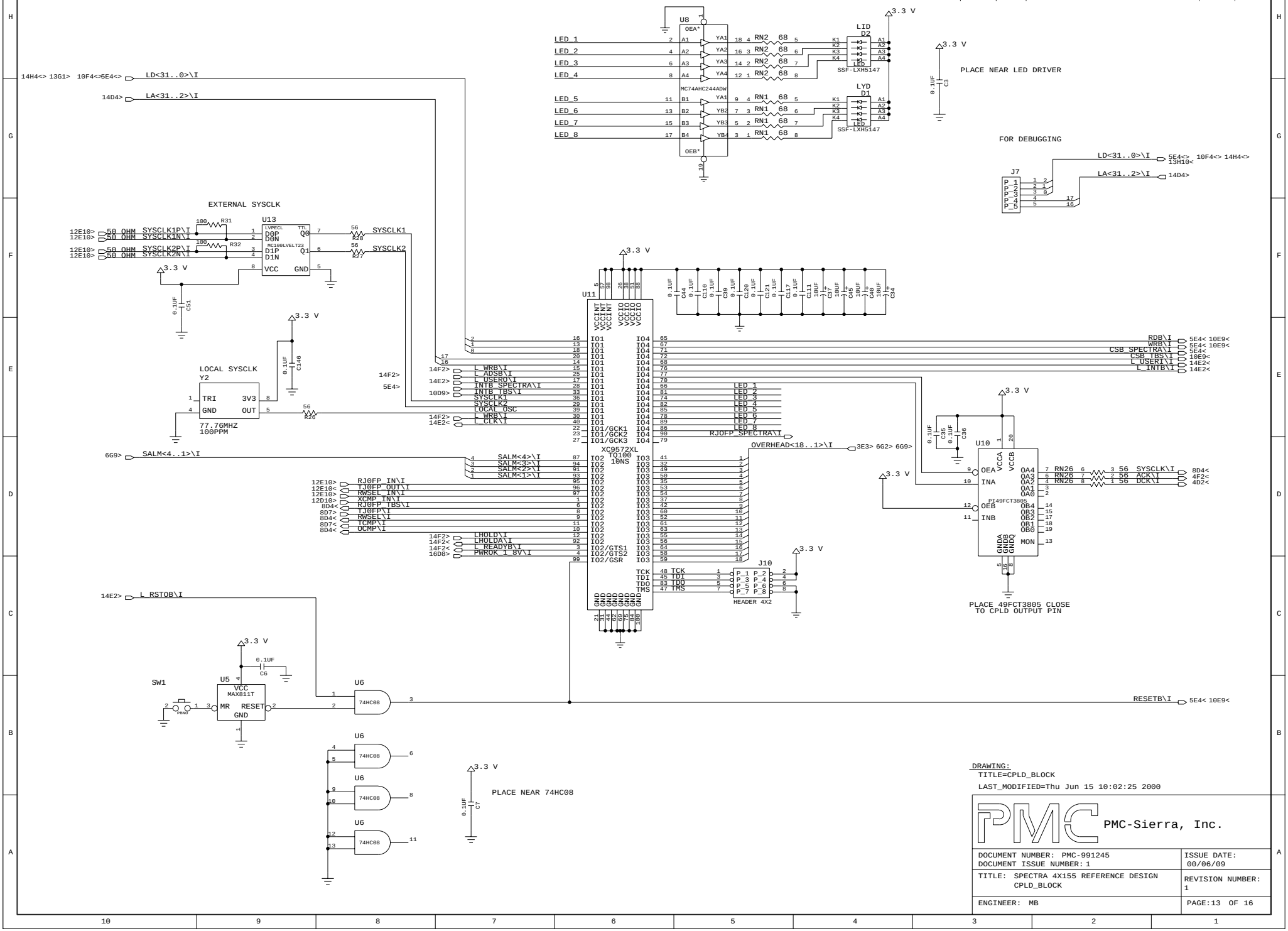


DRAWING:
TITLE=SYS_INTERFACE_BLOCK
LAST_MODIFIED=Thu Jun 15 10:02:22 2000

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991245 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 00/06/09
TITLE: SPECTRA 4X155 REFERENCE DESIGN SYSTEM_INTERFACE_BLOCK	REVISION NUMBER: 1
ENGINEER: MB	PAGE:12 OF 16

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



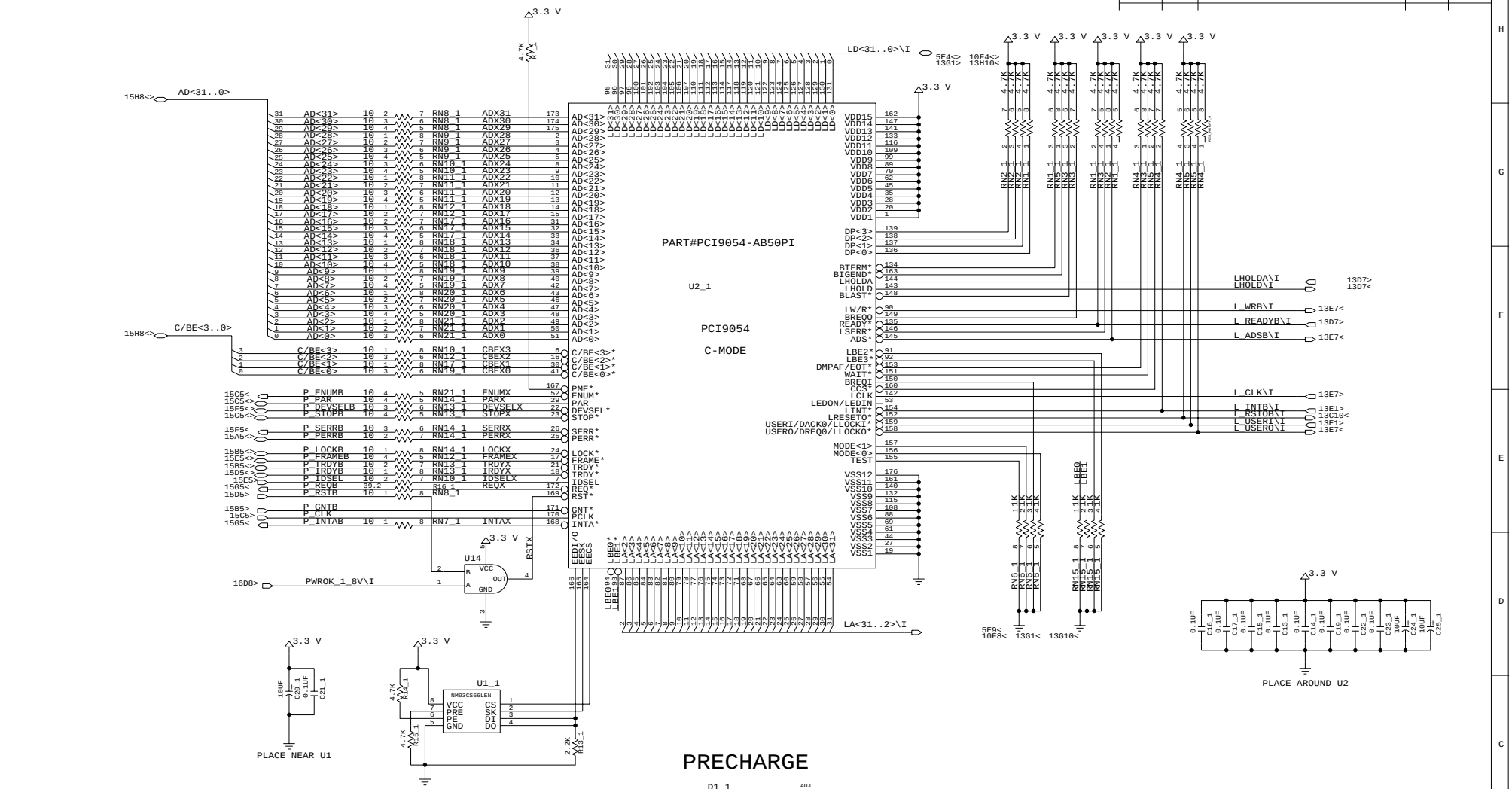
DRAWING:
TITLE=CPLD_BLOCK
LAST_MODIFIED=Thu Jun 15 10:02:25 2000

PMC-Sierra, Inc.

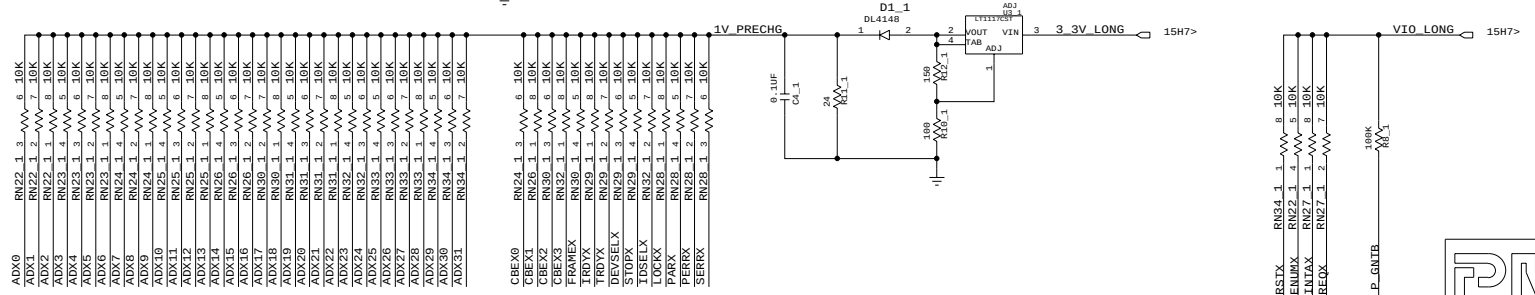
DOCUMENT NUMBER: PMC-991245 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: 00/06/09
TITLE: SPECTRA 4X155 REFERENCE DESIGN CPLD_BLOCK	REVISION NUMBER: 1
ENGINEER: MB	PAGE:13 OF 16

CPCI BRIDGE

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



PRECHARGE



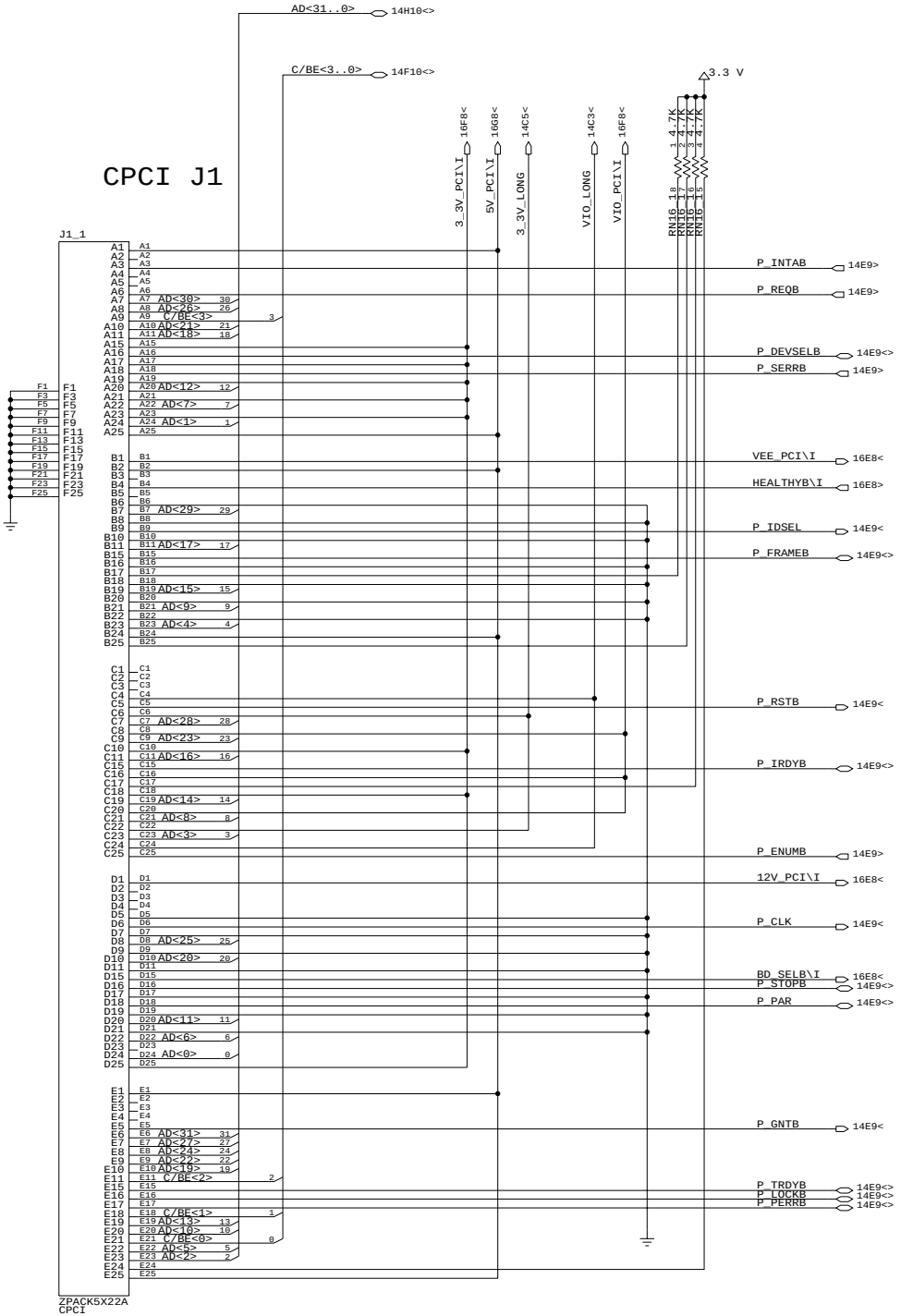
DRAWING:
TITLE=CPCI_BLOCK
ABBREV=CPCI_BLOCK
LAST_MODIFIED=Thu Jun 15 10:02:12 2000

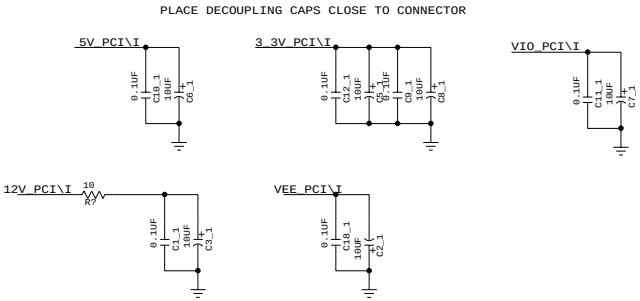
NOTES:
1. ALL 10 OHM STUBS WITHIN 0.6" OF J1
2. ALL PCI SIGNAL TRACES < 1.5" EXCEPT P_CLK
3. P_CLK TRACE MUST BE 2.5" +/- 0.1"
4. CPCI BUS TRACES ARE 65 OHM.
5. 39 OHM STUB RESISTOR ON REQB PLACED NEAR BRIDGE PIN

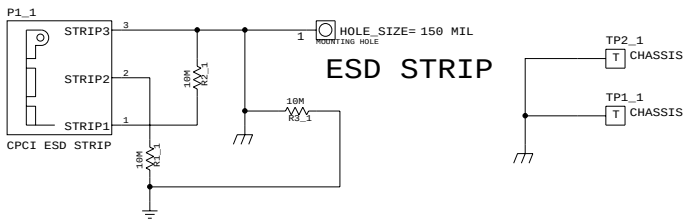
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991413 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: YY/MM/DD
TITLE: CPCI_BLOCK CPCI_BLOCK	REVISION NUMBER: 2
ENGINEER: PMC	PAGE:N OF M

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR







DRAWING:
TITLE=CPCI_BLOCK
ABBREV=CPCI_BLOCK
LAST_MODIFIED=Thu Jun 15 10:02:16 2000

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991245 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: YY/MM/DD
TITLE: SPECTRA 4X155 REFERENCE DESIGN CPCI_BLOCK	REVISION NUMBER: 2
ENGINEER: MB	PAGE:15 OF 16

10 BILL OF MATERIAL

Table 3 - Bill of Material

Item	Ref. No	Description	Manufactures Part #
1	U6	IC QUAD 2 IN AND GATE SOIC14 NARROW BODY	MM74HC08M
2	J5, J6	Z-PACK 6 ROW HS3 BACKPLANE CONNECTOR, RIGHT ANGLE RECEPTACLE	120673-1
3	C67-C78, C7_2	CAP CERAMIC X7R 0603 50V 0.01UF	ECU-V1H103KBV
4	C8_2	CAP CERAMIC X7R 1206 50V 0.047UF	ECU-V1H473KBW
5	C10_1, C3, C6, C7, C13-C20, C35, C36, C39, C44, C51, C63-C66, C80-C84, C88-C119, C11_1, C120-C129, C12_1, C130, C131, C133-C139, C13_1, C140-C149, C14_1, C150-C159, C15_1, C160-C169, C16_1, C170-C177, C17_1, C18_1, C19_1, C1_1, C21_1, C22_1, C23_1, C4_1, C5_2, C6_2, C9_1	CAP CERAMIC X7R 0603 16V 0.1UF	ECJ-1VB1C104K
6	C79, C85-C87	CAP SERAMIC X7R 0805 16V 0.22UF	ECJ-1VB1C224K
7	C1, C2, C20_1, C24_1, C25_1, C29, C2_1, C4, C5, C8, C9, C30-C34, C37, C38, C3_1, C40-C43,	CAP TANCAPC 16V 20% 10UF	ECS-H1CC106R

Item	Ref. No	Description	Manufactures Part #
	C45-C49, C52-C55, C57-C59, C5_1, C60-C62, C6_1, C7_1, C8_1		
8	C2_2, C3_2	CAP TANCAPC 35V 20% 2.2UF	ECS-H1VC225R
9	C1_2, C4_2, C9_2	CAP ELECTRO VA SMD 10V 20% 220UF	ECE-V1AA221P
10	C10-C12, C21-C28, C56	CAP TANCAPD 10V 20% 47UF	ECS-H1AD476R
11	J14	38 PIN SIGNAL CONNECTOR, MATCHED IMPEDANCE, 0.025, SMD	2-767004-2
12	P1_1	COMPACT PCI ESD STRIP, CREATE ON PCB LAYOUT	PART OF PCB
13	D1_1	DIODE RECT 150MA 75V SMT MINIMELF	DL4148MS
14	J11	CONN HEADER STRAIGHT 36POS MALE .1" SINGLE ROW	PZC36SAAN
15	J4	CONN HEADER STRAIGHT 36POS MALE .1" SINGLE ROW	PZC36SAAN
16	J13	CONN HEADER STRAIGHT 36POS MALE .1" SINGLE ROW	PZC36SAAN
17	J7, J12	CONN HEADER STRAIGHT 36POS MALE .1" SINGLE ROW	PZC36SAAN
18	J8, J9	CONN HEADER STRAIGHT 36POS MALE .1" SINGLE ROW	PZC36SAAN
19	J15	50 MIL SPACING HEADER (150 POS PER PART)	SAMTEC HTMS-150-25-G-S-1 25
20	J10	HEADER 2X4 SMT 2MM MALE	87267-0850
21	J2	CONNECTOR HEADER 6X2 .1"	PZC36DAAN
22	U1-U4	MT-RJ DUPLEX SINGLE MODE TRANSCEIVER HFCT-5905E	HFCT-5905E
23	L1-L8	1.81	DIGI-KEY -- PCD1172CT-ND
24	Q1_2, Q2_2	IC MOSFET POWER	IRF7413
25	U7	REGULATOR VARIABLE MICROPOWER LOW DROPOUT 3.3V	LM1085
26	U12	REGULATOR VARIABLE MICROPOWER LOW DROPOUT ADJUSTABLE	LM1085IS-ADJ
27	U3_1	REGULATOR ADJUSTABLE SOT223 800MA OUTPUT	LT1117CST

Item	Ref. No	Description	Manufactures Part #
28	U2_2	IC CPCI HOT SWAP CONTROLLER	LTC1643LCGN
29	U5	4 PIN UP VOLTAGE MONITOR WITH MANUAL RESET INPUT 3.08V SOT143	MAX811TEUS-T
30	U3_2	IC VOLTAGE MONITOR WITH MANUAL RESET INPUT 2.63V SOT143	MAX812REUS-T
31	Y1	OSC HCMOS/TTL HALF SIZE 8 PIN 19.44MHZ 20PPM	MB3020H48-19.44MH Z
32	Y2	OSC HCMOS/TTL HALF SIZE 8 PIN 77.76MHZ 100PPM	MB3100H-77.76MHZ
33	U13	IC DUAL DIFFERENTIAL LVPECL TO TTL TRANSLATOR SOIC8	MC100LVELT23D
34	U8	IC OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER SO20WB	MC74HC244ADW
35	M1_1	MOUNTING HOLE .150" DIA	MOUNTING HOLE
36	U1_1	4096 BIT SERIAL EEPROM W/ DATA PROTECT AND SEQ READ DIP8	NM93CS66LEN
37	SW1	VERT PCB MOUNT SPST PUSH BUTTOM	DIGIKEY -- P8009S-ND
38	U2_1	IC PCI-TO-LOCAL BUS	PCI9054-AB50PI
39	U10	IC 3.3V 2X1:5 CMOS CLOCK DRIVER QSOP20	PI49FCT3805CQ
40	R14_2, R15_2, R5_2	RES 2512 1W 1% 0.01 OHM	WSL2512-R01-1
41	R67, R70	RES 0603 1/16W 5% 1.0K OHM	ERJ-3GSYJ102V
42	R2_2	RES 0603 1/16W 5% 1.2K OHM	ERJ-3GSYJ122V
43	R6_2, R8_2	RES 0603 1/16W 5% 10 OHM	ERJ-3GSYJ100V
44	R10, R10_1, R4, R7, R13, R29, R31, R32, R64, R9_2	RES 0603 1/16W 1% 100 OHM	ERJ-3EKF1000V
45	R16_2, R8_1	RES 0603 1/16W 5% 100K OHM	ERJ-3GSYJ104V
46	R1_1, R2_1, R3_1	RES 1206 1/8W 5% 10M OHM	ERJ-8GEYJ106V
47	R12_1	RES 0603 1/16W 1% 150 OHM	ERJ-3EKF1500V
48	R10_2, R50-R61	RES 0603 1/16W 5% 150 OHM	ERJ-3GSYJ151V
49	R1_2	RES 0603 1/16W 1% 182 OHM	ERJ-3EKF1820V
50	R3_2, R4_2	RES 0603 1/16W 5% 2.0K OHM	ERJ-3GSYJ202V
51	R13_1	RES 0603 1/16W 5% 2.2K OHM	ERJ-3GSYJ222V

Item	Ref. No	Description	Manufactures Part #
52	R1, R33	RES 0805 1/10W 1% 2.7 OHM	ERJ-6RQF2R7V
53	R35, R37, R39, R41	RES 0603 1/16W 5% 220 OHM	ERJ-3GSYJ221V
54	R11_1	RES 0805 1/10W 5% 24 OHM	ERJ-6GEYJ240V
55	R69	RES 0603 1/16W 1% 3.16K OHM	ERJ-3EKF3161V
56	R34, R36, R38, R40	RES 0603 1/16W 5% 330 OHM	ERJ-3GSYJ331V
57	R16_1	RES 0603 1/16W 1% 39.2 OHM	ERJ-3EKF39R2V
58	R14_1, R20-R25, R62, R65, R66, R68, R7_1, R7_2	RES 0603 1/16W 5% 4.7K OHM	ERJ-3GSYJ472V
59	R42-R49	RES 0603 1/16W 1% 49.9 OHM	ERJ-3EKF49R9V
60	R26-R28, R63	RES 0603 1/16W 5% 56 OHM	ERJ-3GSYJ560V
61	R12_2, R13_2	RES 0603 1/16W 5% 560 OHM	ERJ-3GSYJ561V
62	R11_2	RES 0603 1/16W 1% 63.4 OHM	ERJ-3EKF63R4V
63	RN10_1, RN11_1, RN12_1, RN13_1, RN14_1, RN17_1, RN18_1, RN19_1, RN20_1, RN21_1, RN7_1, RN8_1, RN9_1		PANASONIC -- EXB-V8V100JV
64	RN22_1, RN23_1, RN24_1, RN25_1, RN26_1, RN27_1, RN28_1, RN29_1, RN30_1, RN31_1, RN32_1, RN33_1, RN34_1		PANASONIC -- EXB-V8V103JV
65	RN15_1, RN6_1		PANASONIC -- EXB-V8V102JV
66	RN3-RN16, RN16_1, RN17-RN19, RN1_1, RN20-RN25, RN27-RN29, RN2_1, RN30-RN34, RN3_1, RN4_1, RN5_1		PANASONIC -- EXB-V8V472JV
67	RN26		PANASONIC -- EXB-V8V560JV
68	U1_2	IC REGULATOR 3.3V TO 1.8V 20 WATTS	SIE501.8R

Item	Ref. No	Description	Manufactures Part #
69	J1, J3	SMB VERTICAL GOLD	ARF1244-ND
70	U9	MONOLITHIC FOUR CHANNEL SONET/SDH PAYLOAD EXTRACTOR/ALIGNER	PM5316
71	D2_2	LED QUAD GREEN HORIZONTAL	SSF-LXH5147LGD
72	D2	LED QUAD RED HORIZONTAL	SSF-LXH5147LID
73	D1	LED QUAD YELLOW HORIZONTAL	SSF-LXH5147LYD
74	U15	TELECOMBUS SERIALIZER	PM5310
75	TP1_1, TP2_1	CONNECTOR HEADER STRAIGHT SINGLE .1"	N/A
76	U11	CPLD 3.3V 10NS	XC9572XL-10TQ100I
77	D1_2		DIGI-KEY ZM4742ACT-ND
78	J1_1	CONNECTOR ZPACK CPCI 2MM HM 110 POS. TYPE A WITH GND SHIELD	352068-1
79	U14	IC SINGLE 2-INPUT POSITIVE AND GATE	SN74AHC1G08DCKR

NOTES

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