

# Advance Information

## 512K x 32 Bit

### Fast Static RAM Module

The MCM32515 is a 16M bit static random access memory module organized as 524,288 words of 32 bits. The module is offered in a 72-lead single in-line memory module (SIMM). Four MCM6246 fast static RAMs, packaged in 36-lead SOJ packages are mounted on a printed circuit board along with eight decoupling capacitors.

The MCM6246 is a high-performance CMOS fast static RAM organized as 524,288 words of 8 bits. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM32515 is equipped with output enable ( $\overline{G}$ ) and four separate byte enable (E1 – E4) inputs, allowing for greater system flexibility. The  $\overline{G}$  input, when high, will force the outputs to high impedance. Ex high will do the same for byte x.

- Single 5 V  $\pm$  10% Power Supply
- Fast Access Times: 20/25 ns
- Three-State Outputs
- Fully TTL Compatible
- JEDEC Standard Pinout
- Power Requirement: 800/740 mA Maximum, Active AC
- High Board Density SIMM Package
- Byte Operation: Four Separate Chip Enables, One for Each Byte
- High Quality Six-Layer FR4 PWB with Separate Internal Power and Ground Planes
- Incorporates Motorola's State-of-the-Art Fast Static RAMs

PIN NAMES	
A0 – A18	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
E1 – E4	Byte Enables
DQ0 – DQ31	Data Input/Output
VCC	+ 5 V Power Supply
VSS	Ground
PD0 – PD3	Package Density
NC	No Connect

For proper operation of the device, VSS must be connected to ground.

## MCM32515

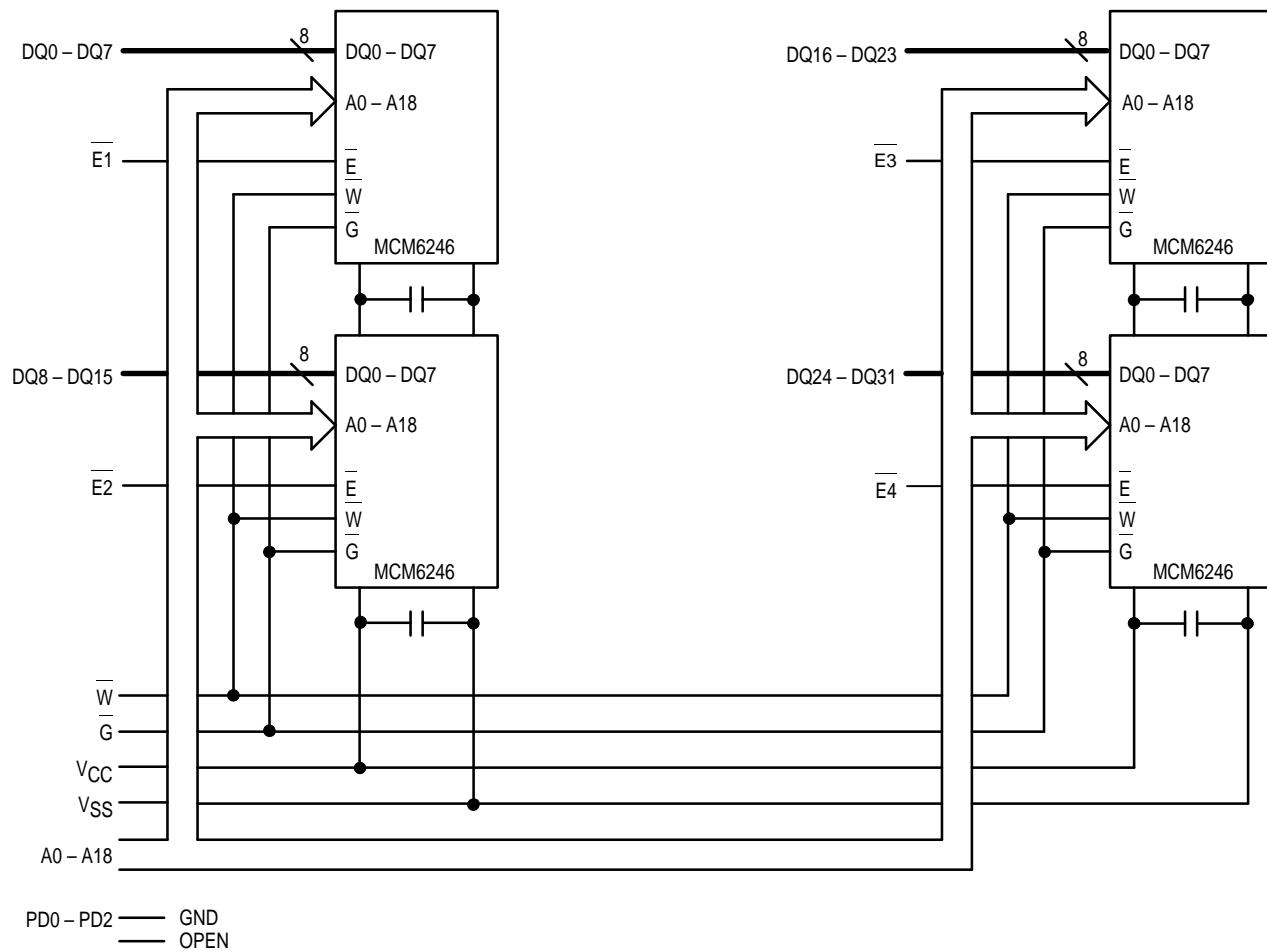
### PIN ASSIGNMENT TOP VIEW 72 LEAD SIMM — CASE TBD

NC	2	1	NC
PD3	4	3	PD2
PD0	6	5	VSS
DQ0	8	7	PD1
DQ1	10	9	DQ8
DQ2	12	11	DQ9
DQ3	14	13	DQ10
VCC	16	15	DQ11
A7	18	17	A0
A8	20	19	A1
A9	22	21	A2
DQ4	24	23	DQ12
DQ5	26	25	DQ13
DQ6	28	27	DQ14
DQ7	30	29	DQ15
$\overline{W}$	32	31	VSS
A14	34	33	A15
E1	36	35	$\overline{E2}$
$\overline{E3}$	38	37	$\overline{E4}$
A16	40	39	A17
VSS	42	41	$\overline{G}$
DQ16	44	43	DQ24
DQ17	46	45	DQ25
DQ18	48	47	DQ26
DQ19	50	49	DQ27
A10	52	51	A3
A11	54	53	A4
A12	56	55	A5
A13	58	57	VCC
DQ20	60	59	A6
DQ21	62	61	DQ28
DQ22	64	63	DQ29
DQ23	66	65	DQ30
VSS	68	67	DQ31
NC	70	69	A18
NC	72	71	NC

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FUNCTIONAL BLOCK DIAGRAM

512K x 32 MEMORY MODULE



## TRUTH TABLE

Ex	G	W	Mode	V <sub>CC</sub> Current	Output	Cycle
H	X	X	Not Selected	I <sub>SB1</sub> or I <sub>SB2</sub>	High-Z	—
L	H	H	Read	I <sub>CCA</sub>	High-Z	—
L	L	H	Read	I <sub>CCA</sub>	D <sub>out</sub>	Read Cycle
L	X	L	Write	I <sub>CCA</sub>	D <sub>in</sub>	Write Cycle

## ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V<sub>SS</sub> = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V <sub>CC</sub>	- 0.5 to 7.0	V
Voltage Relative to V <sub>SS</sub>	V <sub>in</sub> , V <sub>out</sub>	- 0.5 to V <sub>CC</sub> + 0.5	V
Output Current (per I/O)	I <sub>out</sub>	± 30	mA
Power Dissipation	P <sub>D</sub>	4.0	W
Temperature Under Bias	T <sub>bias</sub>	- 10 to + 85	°C
Operating Temperature	T <sub>A</sub>	0 to + 70	°C
Storage Temperature	T <sub>stg</sub>	- 25 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

The devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

These CMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

(V<sub>CC</sub> = 5.0 V ± 10%, T<sub>A</sub> = 0 to + 70°C, Unless Otherwise Noted)

### RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V<sub>SS</sub> = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V <sub>CC</sub>	4.5	5.0	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> +0.3*	V
Input Low Voltage	V <sub>IL</sub>	- 0.5**	—	0.8	V

\* V<sub>IH</sub> (max) = V<sub>CC</sub> + 0.3 V dc; V<sub>IH</sub> (max) = V<sub>CC</sub> + 2 V ac (pulse width ≤ 20 ns)

\*\* V<sub>IL</sub> (min) = - 3.0 V ac (pulse width ≤ 20 ns)

### DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V <sub>in</sub> = 0 to V <sub>CC</sub> )	I <sub>lkg(I)</sub>	—	—	± 4	μA
Output Leakage Current (G, Ex = V <sub>IH</sub> , V <sub>out</sub> = 0 to V <sub>CC</sub> )	I <sub>lkg(O)</sub>	—	—	± 4	μA
AC Active Supply Current (G, Ex = V <sub>IL</sub> , I <sub>out</sub> = 0 mA, MCM32515-20: t <sub>AVAV</sub> = 20 ns Cycle time ≥ t <sub>AVAV</sub> min)	I <sub>CCA</sub>	—	760 700	800 740	mA
AC Standby Current (Ex = V <sub>IH</sub> , Cycle time ≥ t <sub>AVAV</sub> min)	I <sub>SB1</sub>	—	220	240	mA
CMOS Standby Current (Ex ≥ V <sub>CC</sub> - 0.2 V, All Inputs ≥ V <sub>CC</sub> - 0.2 V or ≤ 0.2 V)	I <sub>SB2</sub>	—	40	60	mA
Output Low Voltage (I <sub>OL</sub> = + 8.0 mA)	V <sub>OL</sub>	—	—	0.4	V
Output High Voltage (I <sub>OH</sub> = - 4.0 mA)	V <sub>OH</sub>	2.4	—	—	V

NOTE: Good decoupling of the local power supply should always be used.

### CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T<sub>A</sub> = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All pins except DQ0 - DQ31, W, G, and E1 - E4) (E1 - E4) (W, G)	C <sub>in</sub>	16 10 20	24 14 32	pF
Input/Output Capacitance (DQ0 - DQ31)	C <sub>out</sub>	8	9	pF

## AC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $T_A = 0\text{ to } +70^\circ\text{C}$ , Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V  
 Output Timing Reference Level ..... 1.5 V  
 Input Pulse Levels ..... 0 to 3.0 V

Output Load ..... See Figure 1a Unless Otherwise Noted  
 Input Rise/Fall Time ..... 3 ns

### READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM32515-20		MCM32515-25		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	$t_{AVAV}$	20	—	25	—	ns	3
Address Access Time	$t_{AVQV}$	—	20	—	25	ns	
Enable Access Time	$t_{ELQV}$	—	20	—	25	ns	
Output Enable Access Time	$t_{GLQV}$	—	7	—	9	ns	
Output Hold from Address Change	$t_{AXQX}$	5	—	5	—	ns	
Enable Low to Output Active	$t_{ELQX}$	5	—	5	—	ns	4,5,6
Output Enable to Output Active	$t_{GLQX}$	0	—	0	—	ns	4,5,6
Enable High to Output High-Z	$t_{EHQZ}$	0	9	0	10	ns	4,5,6
Output Enable High to Output High-Z	$t_{GHQZ}$	0	9	0	10	ns	4,5,6
Power Up Time	$t_{ELICCH}$	0	—	0	—	ns	
Power Down Time	$t_{EHICCL}$	—	20	—	25	ns	

#### NOTES:

1.  $\underline{W}$  is high for read cycle.
2. E1 – E4 are represented by  $\bar{E}$  in these timing specifications, any combination of Exs may be asserted.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature,  $t_{EHQZ}$  max is less than  $t_{ELQX}$  min, and  $t_{GHQZ}$  max is less than  $t_{GHQX}$  min, both for a given device and from device to device.
5. Transition is measured  $\pm 500$  mV from steady-state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ( $E = V_{IL}$ ,  $G = V_{IL}$ ).

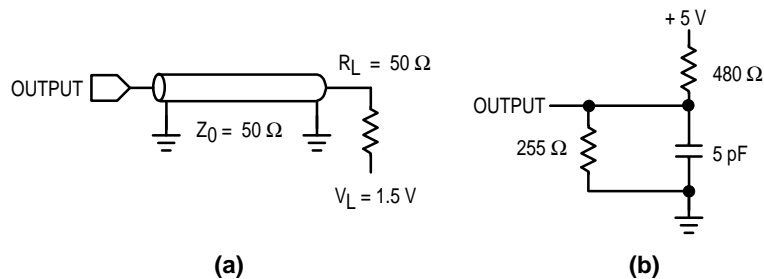
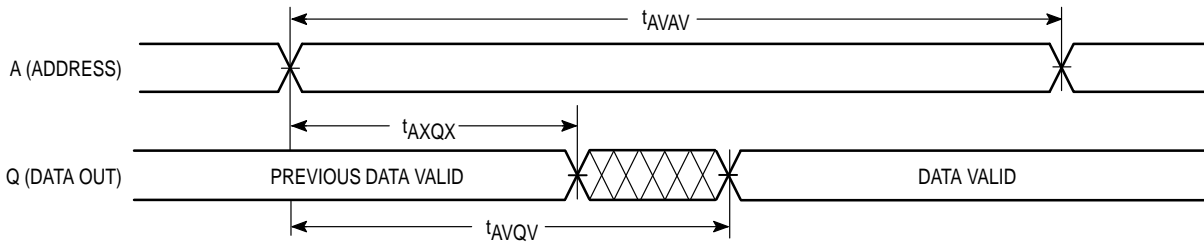


Figure 1. Test Loads

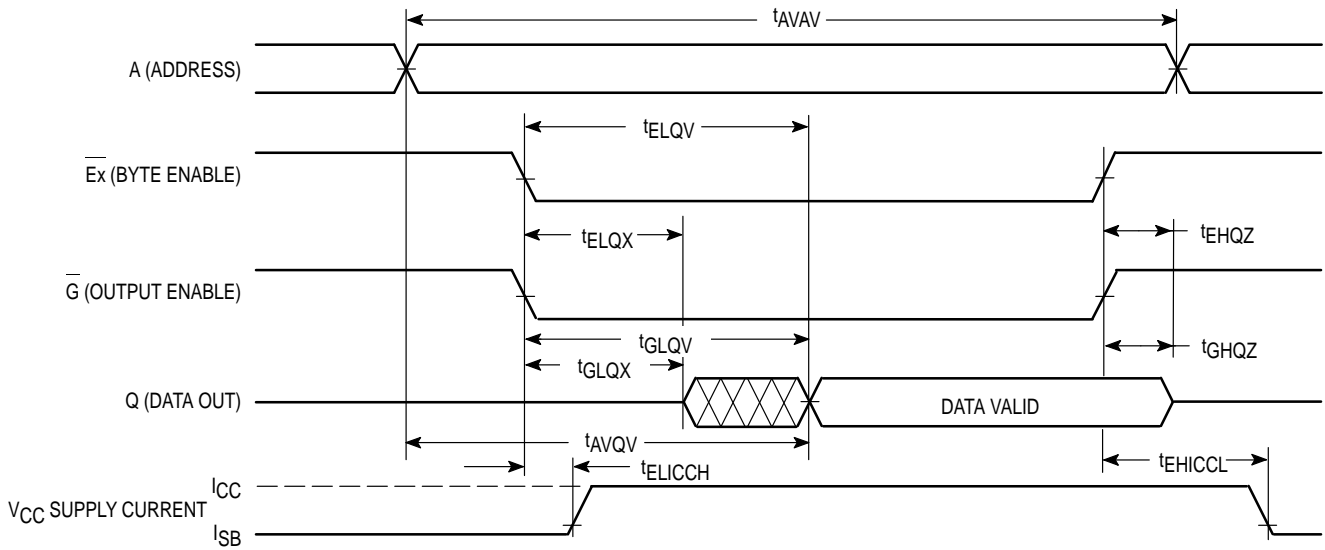
### TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

**READ CYCLE 1** (See Note 7 Above)



**READ CYCLE 2** (See Note)



NOTE: Addresses valid prior to or coincident with  $\bar{E}$  going low.

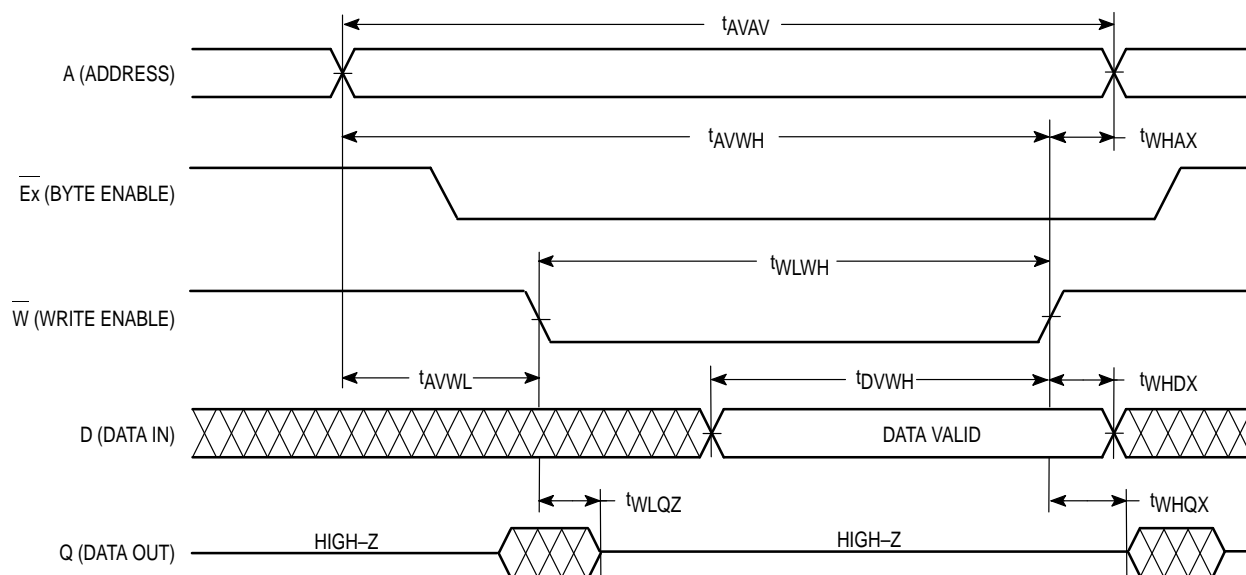
**WRITE CYCLE 1** ( $\overline{W}$  Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM32515-20		MCM32515-25		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	20	—	25	—	ns	3
Address Setup Time	$t_{AVWL}$	0	—	0	—	ns	
Address Valid to End of Write	$t_{AVWH}$	15	—	17	—	ns	
Write Pulse Width	$t_{WLWH}$ , $t_{WLEH}$	15	—	17	—	ns	
Data Valid to End of Write	$t_{DVWH}$	10	—	10	—	ns	
Data Hold Time	$t_{WHDX}$	0	—	0	—	ns	
Write Low to Data High-Z	$t_{WLQZ}$	0	9	0	10	ns	4,5,6
Write High to Output Active	$t_{WHQX}$	5	—	5	—	ns	4,5,6
Write Recovery Time	$t_{WHAX}$	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low.
2. E1 – E4 are represented by E in these timing specifications, any combination of Exs may be asserted.  $\overline{G}$  is a don't care when  $\overline{W}$  is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured  $\pm 500$  mV from steady-state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature,  $t_{WLQZ}$  max is less than  $t_{WHQX}$  min both for a given device and from device to device.

**WRITE CYCLE 1**



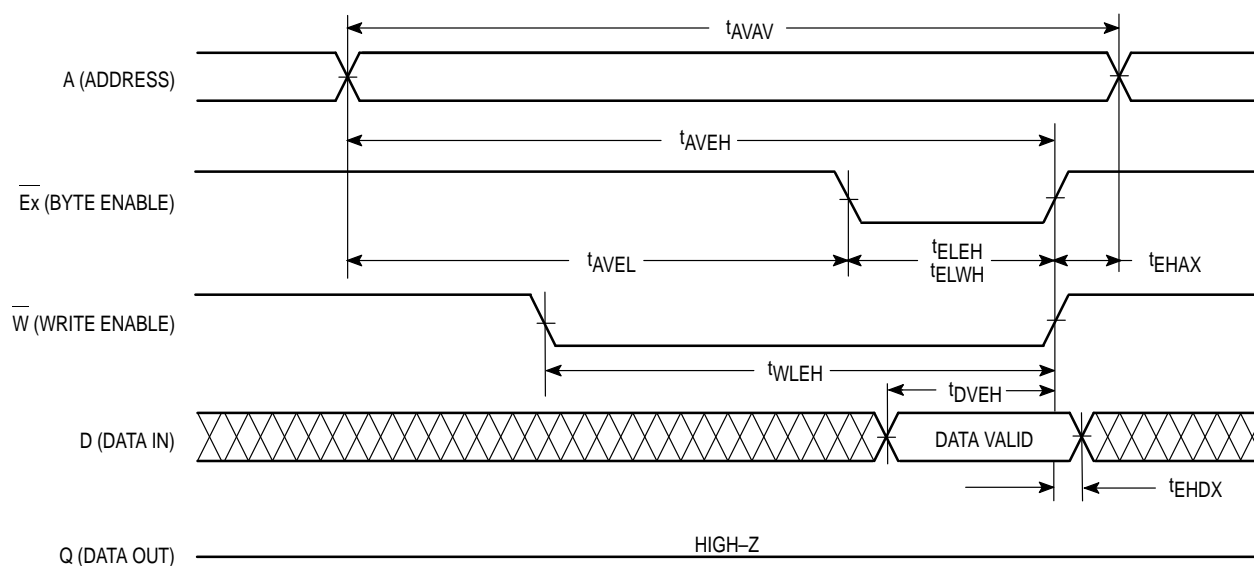
**WRITE CYCLE 2** ( $\bar{E}$  Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM32515-20		MCM32515-25		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	20	—	25	—	ns	3
Address Setup Time	$t_{AVEL}$	0	—	0	—	ns	
Address Valid to End of Write	$t_{AVEH}$	15	—	17	—	ns	
Enable to End of Write	$t_{ELEH}$	15	—	17	—	ns	4,5
Enable to End of Write	$t_{ELWH}$	15	—	17	—	ns	
Write Pulse Width	$t_{WLEH}$	15	—	17	—	ns	
Data Valid to End of Write	$t_{DVEH}$	10	—	10	—	ns	
Data Hold Time	$t_{EHDX}$	0	—	0	—	ns	
Write Recovery Time	$t_{EHAX}$	0	—	0	—	ns	

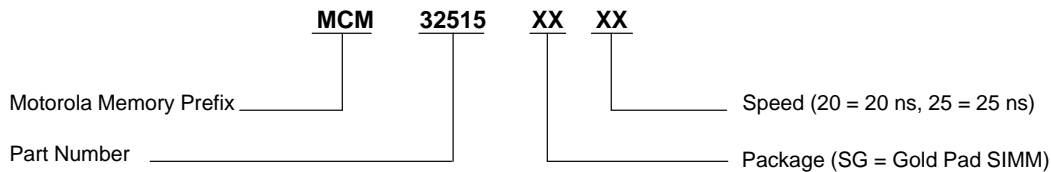
NOTES:

1. A write occurs during the overlap of  $\bar{E}$  low and  $\bar{W}$  low.
2. E1 – E4 are represented by E in these timing specifications, any combination of Exs may be asserted. G is a don't care when  $\bar{W}$  is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If  $\bar{E}$  goes low coincident with or after  $\bar{W}$  goes low, the output will remain in a high impedance condition.
5. If E goes high coincident with or before  $\bar{W}$  goes high, the output will remain in a high impedance condition.


**WRITE CYCLE 2**



**ORDERING INFORMATION**  
(Order by Full Part Number)



Full Part Numbers — MCM32515SG20 MCM32515SG25

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