

## N-Channel Enhancement-Mode Vertical DMOS FETs

## **Ordering Information**

BV <sub>DSS</sub> /	R <sub>DS(ON)</sub>	I <sub>D(ON)</sub>	V <sub>GS(th)</sub>	Order Number / Package		
BV <sub>DGS</sub>	(max)	(min)	(max)	TO-92		
20V	1.3Ω	0.5A	1.0V	TN0702N3		

### **Features**

- Low threshold 1.0 volt max
- On resistance guaranteed at V<sub>GS</sub> = 2, 3, and 5 volts
- High input impedance
- ☐ Low input capacitance —130pF typical
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage

### **Applications**

- Logic level interfaces
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

### **Absolute Maximum Ratings**

Drain-to-Source Voltage	$BV_{DSS}$
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

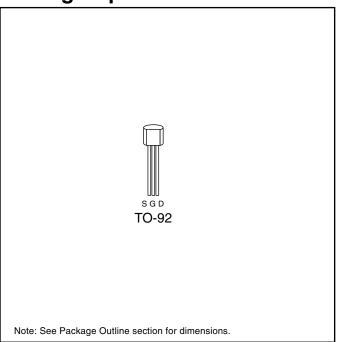
<sup>\*</sup>Distance of 1.6 mm from case for 10 seconds maximum.

### Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

## **Package Option**



03/11/02

## **Thermal Characteristics**

Package	I <sub>D</sub> (continuous)*	I <sub>D</sub> (pulsed)	Power Dissipation @ T <sub>C</sub> = 25°C	$ heta_{ extsf{jc}}$ $^{\circ}$ C/W	θ <sub>ja</sub> °C/W	I <sub>DR</sub> *	I <sub>DRM</sub>
TO-92	0.53A	1.0A	1W	125	170	0.53A	1.0A

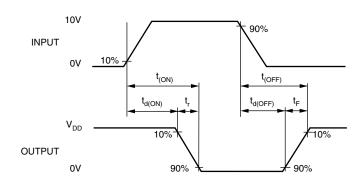
 $<sup>\</sup>overline{\phantom{a}}^* I_D$  (continuous) is limited by max rated  $T_j$ .

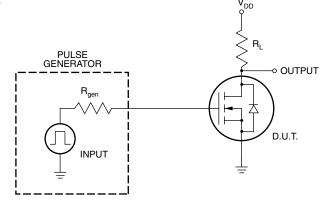
## Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Тур	Max	Unit	Conditions	
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	20			V	$V_{GS} = 0V$ , $I_D = 1mA$	
V <sub>GS(th)</sub>	Gate Threshold Voltage	0.5	0.8	1.0	V	$V_{GS} = V_{DS}, I_D = 1.0 \text{mA}$	
$\Delta V_{GS(th)}$	Change in V <sub>GS(th)</sub> with Temperature			-4.0	mV/°C	$V_{GS} = V_{DS}$ , $I_D = 1.0 \text{mA}$	
I <sub>GSS</sub>	Gate Body Leakage			100	nA	$V_{GS} = \pm 20V, \ V_{DS} = 0V$	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current			100	nA	$V_{DS} = 20V, \ V_{GS} = 0V$	
				100	μΑ	$V_{DS} = 0.8$ Max Rating, $V_{GS} = 0V$ , $T_A = 125$ °C	
I <sub>D(ON)</sub>	ON-State Drain Current	0.5	1.0		Α	$V_{GS} = V_{DS} = 5V$	
	Static Drain-to-Source ON-State Resistance		4.0	5.0	Ω	$V_{GS} = 2V$ , $I_D = 50mA$	
R <sub>DS(ON)</sub>			1.9	2.5		$V_{GS} = 3V, I_{D} = 200mA$	
			1.0	1.3		$V_{GS} = 5V$ , $I_D = 500$ mA	
$\Delta R_{DS(ON)}$	Change in R <sub>DS(ON)</sub> with Temperature			0.75	%/°C	$V_{GS} = 5V, I_{D} = 500mA$	
G <sub>FS</sub>	Forward Transconductance	100	500		mʊ	$V_{DS} = 5V, I_{D} = 500mA$	
C <sub>ISS</sub>	Input Capacitance		130	200			
C <sub>oss</sub>	Common Source Output Capacitance		70	125	pF	$V_{GS} = 0V, V_{DS} = 20V, f = 1MHz$	
C <sub>RSS</sub>	Reverse Transfer Capacitance		30	60			
t <sub>d(ON)</sub>	Turn-ON Delay Time			20			
t <sub>r</sub>	Rise Time			20	ns	$V_{DD} = 20V, I_{D} = 0.5A,$	
t <sub>d(OFF)</sub>	Turn-OFF Delay Time			30		$R_{GEN} = 25\Omega$	
t <sub>f</sub>	Fall Time			20			
V <sub>SD</sub>	Diode Forward Voltage Drop			1.0	V	$V_{GS} = 0V, I_{SD} = 0.5A$	

#### Notes:

# **Switching Waveforms and Test Circuit**

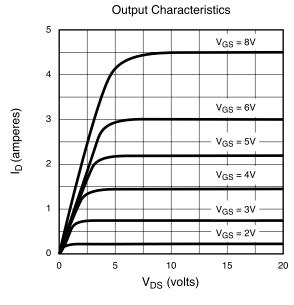


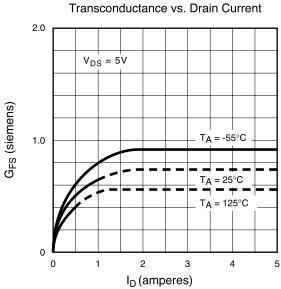


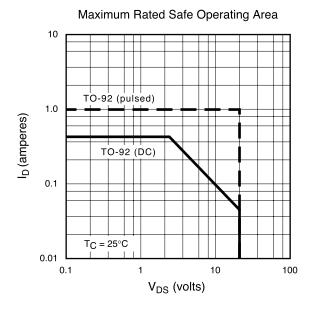
<sup>1.</sup> All D.C. parameters 100% tested at 25°C unless otherwide stated. (Pulse test: 300  $\mu s$  pulse, 2% duty cycle.)

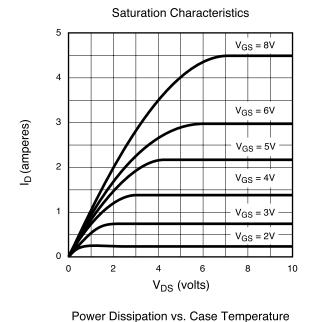
<sup>2.</sup> All A.C. parameters sample tested.

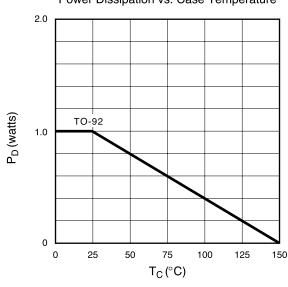
# **Typical Performance Curves**

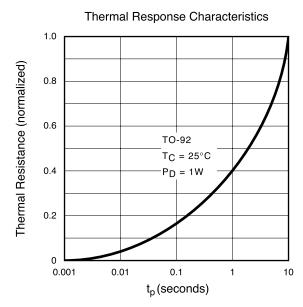


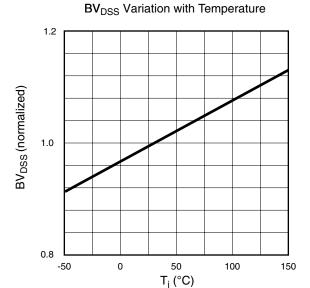




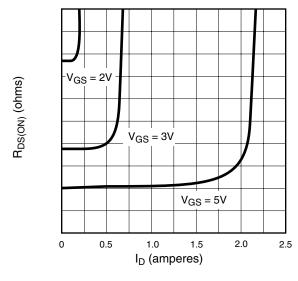




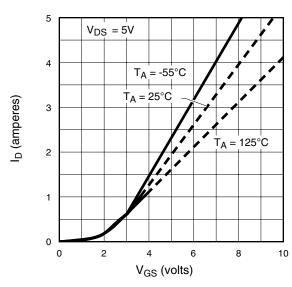




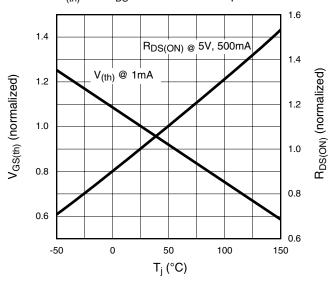
#### On-Resistance vs. Drain Current



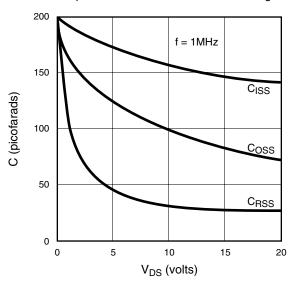




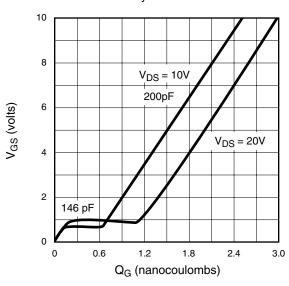
V<sub>(th)</sub> and R<sub>DS</sub> Variation with Temperature



#### Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



02/06//02