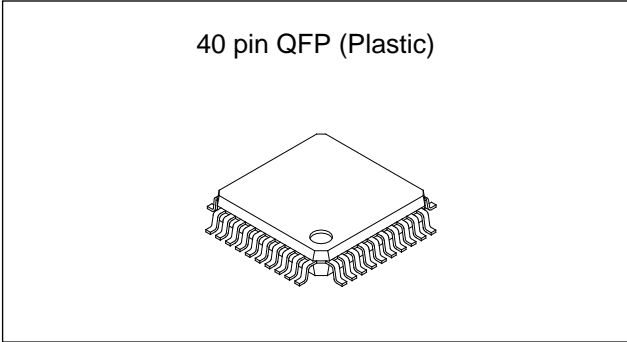


**Post-Amplifier for Optical Fiber Communication Receiver**

**Description**

The CXB1577Q achieves the 2R optical-fiber communication receiver functions (Reshaping and Regenerating) on a single chip. This IC is equipped with the signal detection function, which is used to enable TTL/ECL outputs. Also, the output disable function performs the output shutdown. 3.3V/5.0V can be used for the supply voltage.



**Features**

- Output disable function (TTL input)
- Signal detection function (TTL/ECL output)
- Supply voltage supports both 3.3V/5.0V

**Applications**

- SONET/SDH: 622.08Mbps
- Fibre Channel: 531.25Mbps  
: 1.062Gbps
- Gigabit-Ethernet: 1.25Gbps

**Absolute maximum Ratings**

• Supply voltage	$V_{CC} - V_{EE}$	-0.3 to +7	V
• Storage temperature	$T_{stg}$	-65 to +150	°C
• Input voltage difference $ V_D - V_{\bar{D}} $	$V_{dif}$	0 to +2	V
• SW input voltage	$V_i$	$V_{EE}$ to $V_{CC}$	V
• ECL output current	$I_{oQ/SD-ECL}$	-30 to 0	mA
• TTL output current (High level)	$I_{oH SD-TTL}$	-20 to 0	mA
• TTL output current (Low level)	$I_{oL SD-TTL}$	0 to 20	mA

**Recommended Operating Conditions**

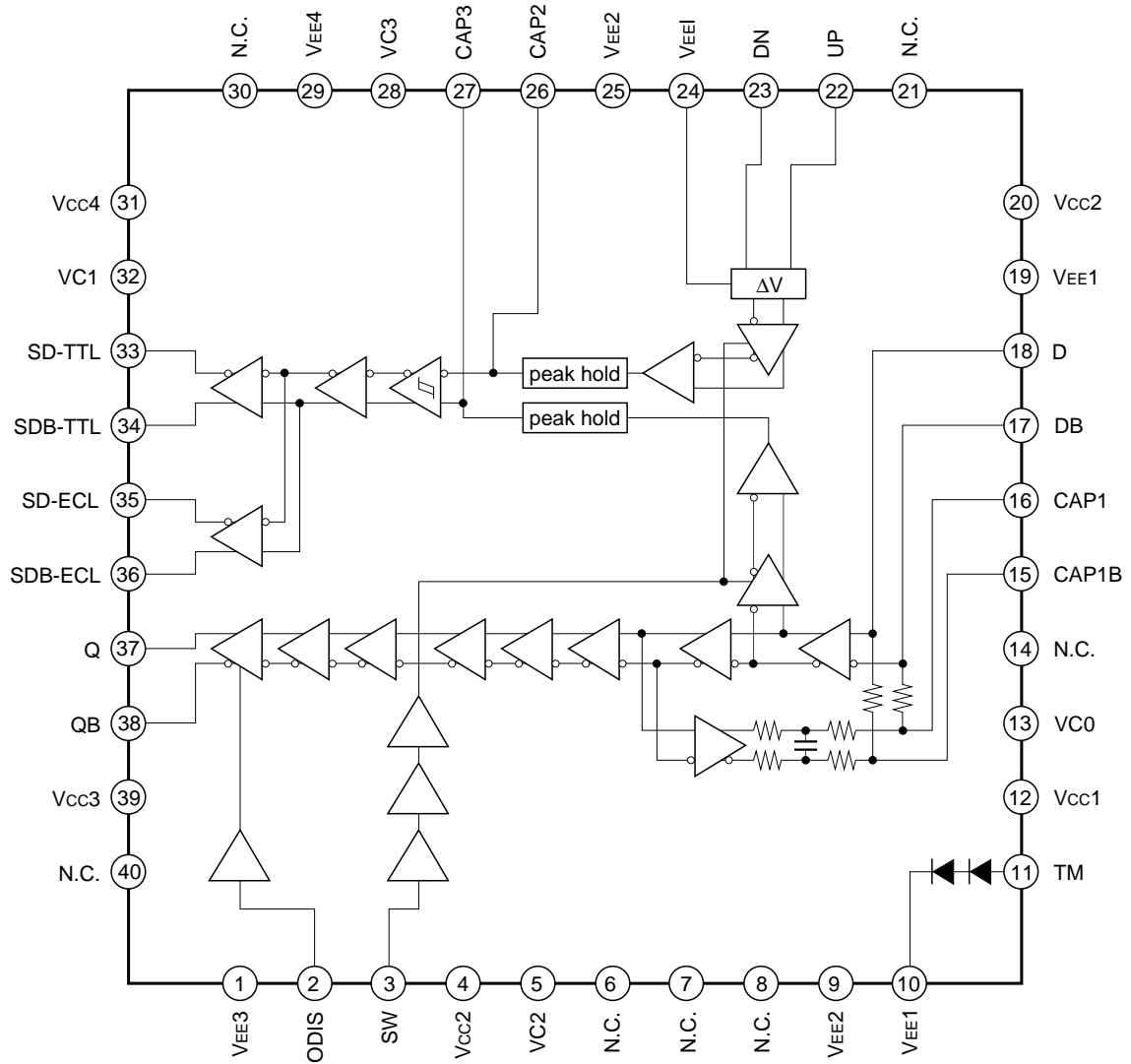
• Supply voltage	$V_{CC} - V_{EE}$	$3.3 \pm 0.2/5 \pm 0.25$	V
• Termination voltage (for data)	$V_{CC} - V_{TD}$	1.8 to 2.2	V
• Termination voltage (for alarm 1,alarm 2)	$V_{TA}$	$V_{EE}$	V
• Termination resistance (for data)	$R_{TD}$	46 to 56	$\Omega$
• Termination resistance (for alarm 1)	$R_{TA1}$	240 to 300	$\Omega$
• Termination resistance (for alarm 2)	$R_{TA2}$	460 to 560	$\Omega$
• Operating temperature	$T_a$	-40 to +85	°C

**Structure**

Bipolar silicon monolithic IC

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Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	Typical pin voltage		Equivalent circuit	Description
		DC	AC		
1	V <sub>EE3</sub>	-3.3V /-5V			Negative power supply for ECL output buffer.
2	ODIS	0V (Open) or -3.3V /-5V			Controls the output shutdown function. High voltage when open; the Q output is fixed to Low. Low voltage when connected to V <sub>EE</sub> ; the D input results in the Q output with ECL level. TTL level is also available.
3	SW	0V (Open) or -3.3V /-5V			Switches the identification maximum voltage amplitude. High voltage when open; the identification maximum voltage amplitude becomes 40mVp-p. Low voltage when connected to V <sub>EE</sub> ; the amplitude becomes 20mVp-p.
4	V <sub>CC2</sub>	0V			Positive power supply for digital block.
5	VC2	0V /-1.7V (Open)			Switches 3.3V/5V. Short this pin to V <sub>CC</sub> for 3.3V between V <sub>CC</sub> and V <sub>EE</sub> . Leave this pin open for 5V between V <sub>CC</sub> and V <sub>EE</sub> .
6	N.C.				No connected.
7					
8					
9	V <sub>EE2</sub>	-3.3V /-5V			Negative power supply for digital block.
10	V <sub>EE1</sub>	-3.3V /-5V			Negative power supply for analog block.
11	TM	-1.8V /-3.5V			Chip temperature monitor.

Pin No.	Symbol	Typical pin voltage		Equivalent circuit	Description
		DC	AC		
12	Vcc1	0V			Positive power supply for analog block.
13	VC0	0V /-1.7V (Open)			Switches 3.3V/5V. Short this pin to Vcc for 3.3V between Vcc and VEE. Leave this pin open for 5V between Vcc and VEE.
14	N.C.				No connected.
15	CAP1B				Pins 15 and 16 connect a capacitor which determines the cut-off frequency for DC feedback block. Pins 17 and 18 are input pins for limiting amplifier block. Input the signal with AC coupled.
16	CAP1				
17	DB	-1.3V	-0.9V to -1.7V		
18	D	-1.3V	-0.9V to -1.7V		
19	VEE1	-3.3V /-5V			Negative power supply for analog block.
20	Vcc2	0V			Positive power supply for digital block.
21	N.C.				No connected.
22	UP				Connects a resistor for alarm level setting. Default voltage can be generated without an external resistor by shorting the VEE1 pin to VEE.
23	DN				
24	VEE1	-3.3V /-5V			Generates the default voltage between UP and DOWN. The voltage (8.0mV for input conversion) can be generated between UP and DOWN (Pins 22 and 23) as alarm setting level by connecting this pin to VEE.
25	VEE2	-3.3V /-5V			Negative power supply for digital block.



Pin No.	Symbol	Typical pin voltage		Equivalent circuit	Description
		DC	AC		
33	SD-TTL		$V_{EE}$ or $V_{EE} + 3V$		Alarm signal TTL level output.
34	SDB-TTL		$V_{EE}$ or $V_{EE} + 3V$		Alarm signal TTL level output.
35	SD-ECL		$-0.9V$ or $-1.7V$		Alarm signal ECL level output. Terminate this pin in $510\Omega$ to $V_{EE}$ at $V_{EE} = 5V$ ; in $270\Omega$ to $V_{EE}$ at $V_{EE} = 3.3V$ .
36	SDB-ECL		$-0.9V$ or $-1.7V$		

Pin No.	Symbol	Typical pin voltage		Equivalent circuit	Description
		DC	AC		
37	Q		-0.9V or -1.7V		<p>Data signal output. Terminates this pin in <math>50\Omega</math> to <math>V_{TT} = V_{cc} - 2V</math>.</p>
38	QB		-0.9V or -1.7V		
39	Vcc3	0V			Positive power supply for ECL output buffer.
40	N.C.				No connected.

**Electrical Characteristics**

**DC Characteristics**

$V_{CC} = GND$ ,  $V_{EE} = -5V \pm 5\%$ ,  $T_a = -40$  to  $+85^\circ\text{C}$ ,  $VC0$  to  $VC3 = \text{open}$ ,  
 or  $V_{CC} = GND$ ,  $V_{EE} = -3.3V \pm 5\%$ ,  $T_a = -40$  to  $+85^\circ\text{C}$ ,  $VC0$  to  $VC3 = GND$

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current	$I_{EE}$		-74	-51	-34	mA
Q/QB High output voltage	$V_{OH}$	$50\Omega$ to $V_{TT}$	-1100		-860	mV
Q/QB Low output voltage	$V_{OL}$	$T_a = 0$ to $+85^\circ\text{C}$	-1860		-1620	
SD-ECL/SDB-ECL High output voltage	$V_{OH-E}$	When $V_{CC} - V_{EE} = 5.0V$ , $510\Omega$ to $V_{EE}$ ; when $V_{CC} - V_{EE} = 3.3V$ , $270\Omega$ to $V_{EE}$	-1100		-860	mV
SD-ECL/SDB-ECL Low output voltage	$V_{OL-E}$	$T_a = 0$ to $+85^\circ\text{C}$	-1890		-1650	
SD-TTL/SDB-TTL High output voltage 1	$V_{OH-T1}$	$I_{OH} = -0.4mA$ , $V_{CC} - V_{EE} = 3.3V$ , $T_a = 0$ to $+85^\circ\text{C}$	$V_{EE} + 2.2$			V
SD-TTL/SDB-TTL High output voltage 2	$V_{OH-T2}$	$I_{OH} = -0.4mA$ , $V_{CC} - V_{EE} = 5V$ , $T_a = 0$ to $+85^\circ\text{C}$	$V_{EE} + 2.4$			
SD-TTL/SDB-TTL Low output voltage	$V_{OL-T}$	$I_{OL} = 2mA$ $T_a = 0$ to $+85^\circ\text{C}$			$V_{EE} + 0.5$	
SW High input voltage	$V_{IHSW}$	at SW pin Open: High	$V_{CC} - 0.5$		$V_{CC}$	
SW Low input voltage	$V_{ILSW}$		$V_{EE}$		$V_{EE} + 0.5$	$\mu\text{A}$
SW High input current	$I_{IHSW}$				10	
SW Low input current	$I_{ILSW}$		-100			V
ODIS High input voltage	$V_{IHOD}$	at ODIS pin Open: High	$V_{EE} + 2.0$		$V_{CC} + 0.5$	
ODIS Low input voltage	$V_{ILOD}$		$V_{EE}$		$V_{EE} + 0.8$	$\mu\text{A}$
ODIS High input current	$I_{IHOD}$				20	
ODIS Low input current	$I_{ILOD}$		-400			$\Omega$
D/DB input resistance	$R_{in}$		765	1020	1275	



**AC Characteristics**

$V_{CC} = GND$ ,  $V_{EE} = -5V \pm 5\%$ ,  $T_a = -40$  to  $+85^\circ C$ ,  $VC0$  to  $VC3 = open$ ,  
or  $V_{CC} = GND$ ,  $V_{EE} = -3.3V \pm 5\%$ ,  $T_a = -40$  to  $+85^\circ C$ ,  $VC0$  to  $VC3 = GND$

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Maximum input voltage amplitude	Vmax	single-ended input	1600			mVp-p
Amplifier gain (excluding the output buffer)	GL		52			dB
Identification maximum voltage amplitude of alarm level	VmaxA1	SW pad: Low, single-ended input	20			mVp-p
	VmaxA2	SW pad: Open High, single-ended input	40			
SD/SDB hysteresis width	$\Delta P1$	SW pin: Low, at default alarm level	3	6	7	dB
	$\Delta P2$	SW pin: Open High, at default alarm level	3	6	7	
Alarm setting level for default	Vdef	UP/DOWN pin: open, $V_{EEL} = V_{EE}$ , Differential voltage input	7.0	8.4	9.7	mV
Q/QB rise time	TrQ	20% to 80%		230	350	ps
Q/QB fall time	TfQ	50 $\Omega$ to VTT		230	350	
SD-TTL/SDB-TTL rise time	TrSDT	$V_{EE} + 0.8V$ to $V_{EE} + 2.0V$ $C_L = 10pF$			10	ns
SD-TTL/SDB-TTL fall time	TfSDT				10	
SD-ECL/SDB-ECL rise time	TrSDE	20% to 80% When $V_{CC} - V_{EE} = 5.0V$ , 510 $\Omega$ to $V_{EE}$ , when $V_{CC} - V_{EE} = 3.3V$ , 270 $\Omega$ to $V_{EE}$			1.6	
SD-ECL/SDB-ECL fall time	TfSDE				1.6	
Propagation delay time	TPD		0.4		1.9	
SD response assert time	Tas	*1	0		100	$\mu s$
SD response deassert time	Tdas	*2	2.3		100	
SD response assert time for alarm level default	Tasd	*3	0		100	
SD response deassert time for alarm level default	Tdasd	*4	2.3		100	

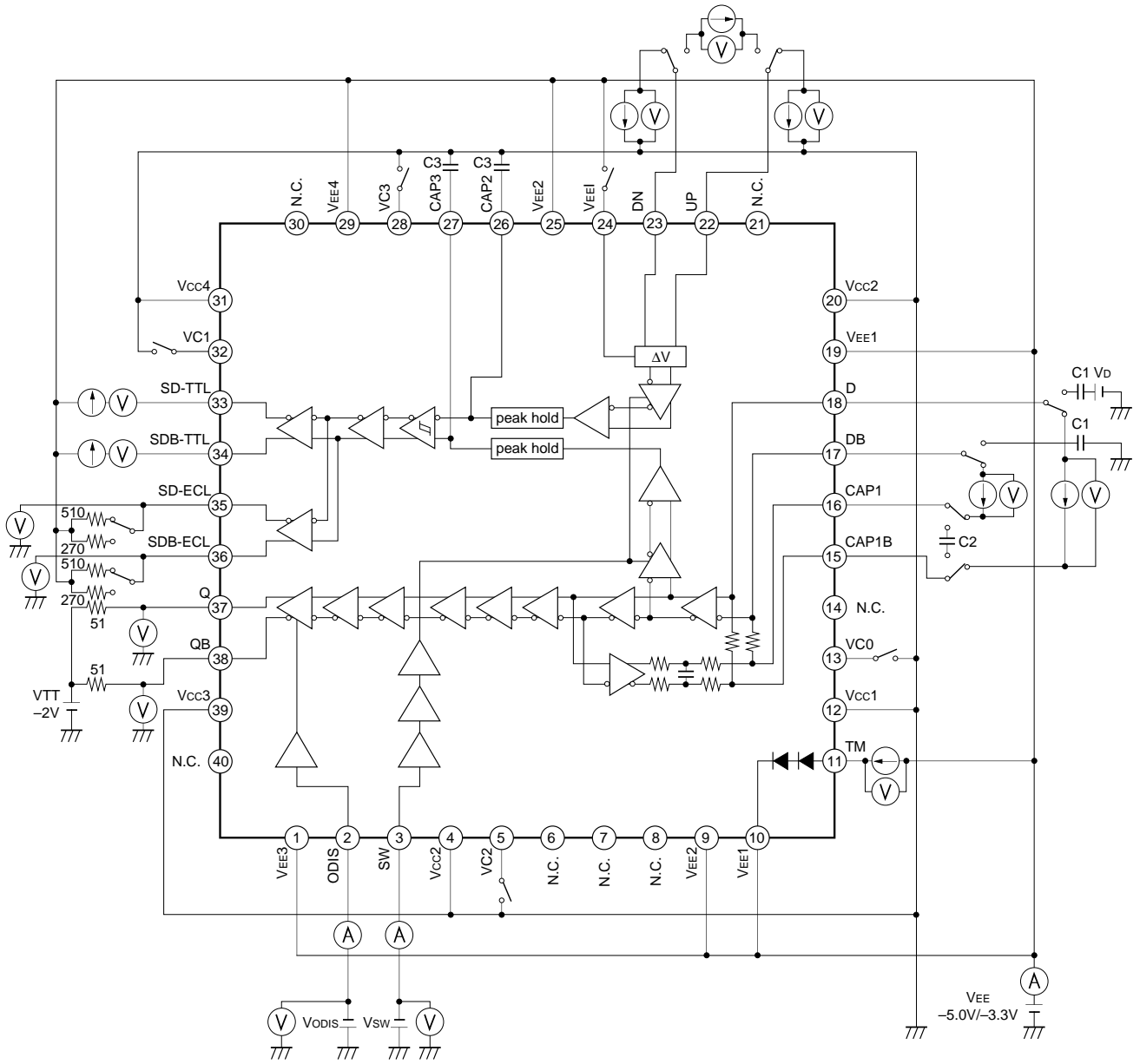
\*1  $V_{UP} - V_{DOWN} = 100mV$ ,  $V_{in} = 100mVp-p$  (single ended), SW pin: High, peak hold capacitance (CAP2, CAP3 pins) of 470pF, connect  $V_{EEL}$  to  $V_{EE}$ .

\*2  $V_{UP} - V_{DOWN} = 100mV$ ,  $V_{in} = 1Vp-p$  (single ended), SW pin: High, peak hold capacitance (CAP2, CAP3 pins) of 470pF, connect  $V_{EEL}$  to  $V_{EE}$ .

\*3  $V_{in} = 50mVp-p$  (single ended), SW pin: Low, peak hold capacitance of 470pF, connect  $V_{EEL}$  to  $V_{EE}$ .

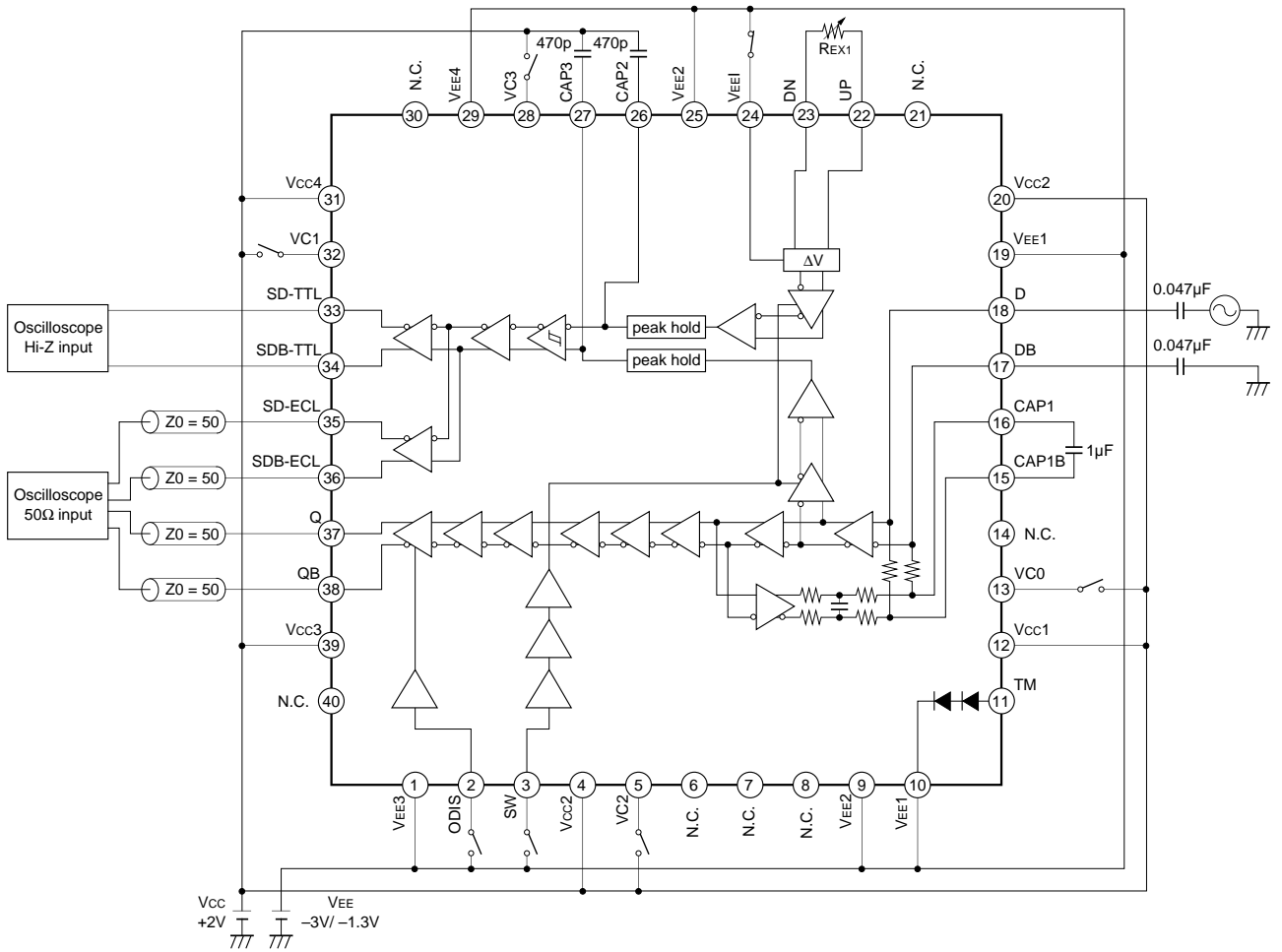
\*4  $V_{in} = 1Vp-p$  (single ended), SW pin: Low, peak hold capacitance of 470pF, connect  $V_{EEL}$  to  $V_{EE}$ .

DC Electrical Characteristics Measurement Circuit



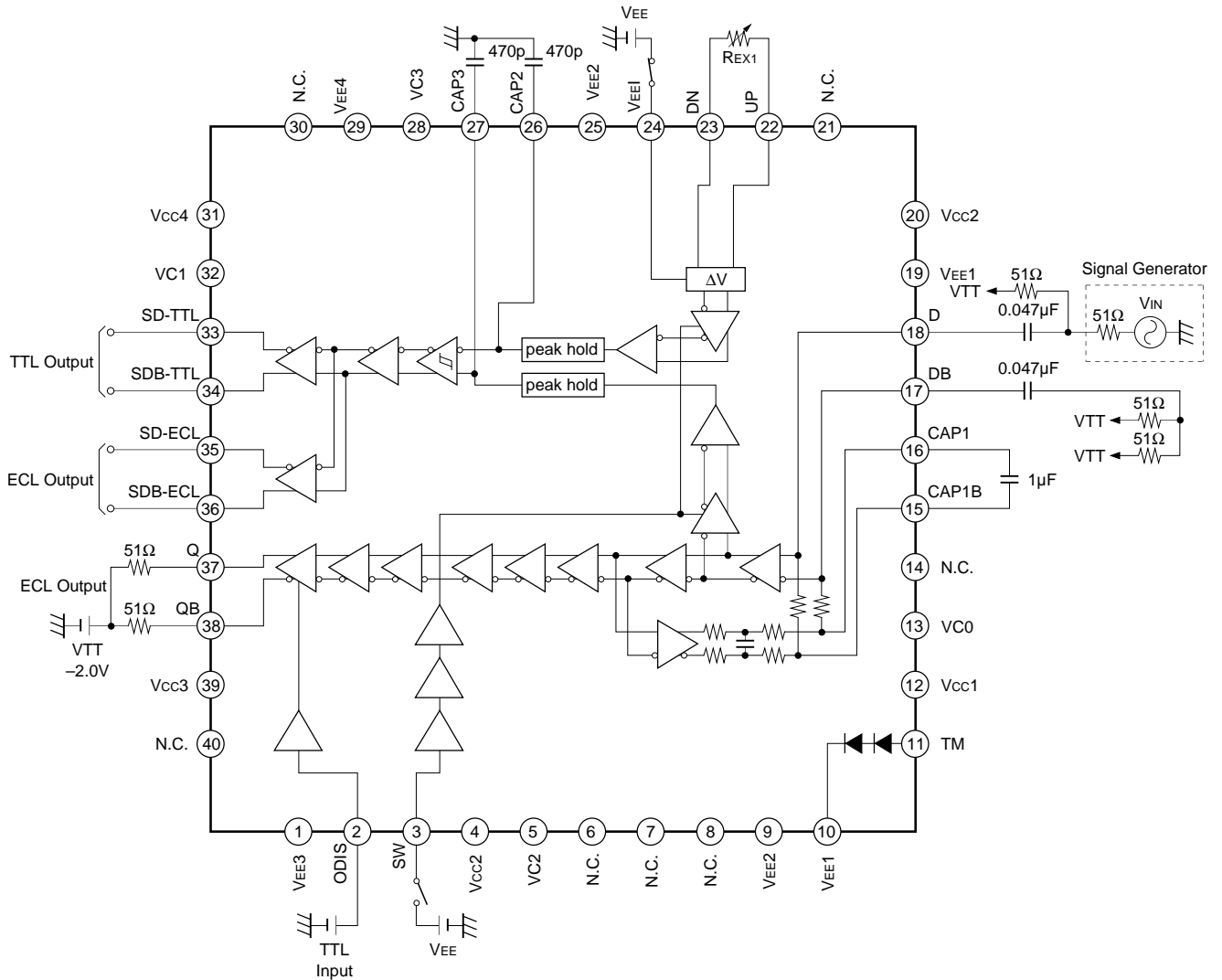
\* When VEE = -5.0V: VC0 to VC3 = open  
 When VEE = -3.3V: VC0 to VC3 = Vcc

AC Electrical Characteristics Measurement Circuit



\* When VEE = -3.0V: VC0 to VC3 = open  
 When VEE = -1.3V: VC0 to VC3 = Vcc

Application Circuit



\* When VEE = -3.3V: VC0 to VC3 = Vcc  
 When VEE = -5.0V: VC0 to VC3 = open

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

1. Limiting amplifier block

The limiting amplifier block is equipped with the auto-offset canceler circuit. When external capacitors C1 and C2 are connected as shown in Fig. 1, the DC bias is set automatically in this block. External capacitor C1 and IC internal resistor R1 determine the low input cut-off frequency f2 as shown in Fig. 2. Similarly, external capacitor C2 and IC internal resistor R2 determine the high cut-off frequency f1 for DC bias feedback. Since peaking characteristics may occur in the low frequency area of the amplifier gain characteristics depending on the f1/f2 combination, set the C1 and C2 values so as to avoid the occurrence of peaking characteristics. The target values of R1 and R2 and the typical values of C1 and C2 are as indicated below. When a single-ended input is used, provide AC grounding by connecting Pin 17 to a capacitor which has the same capacitance as capacitor C1.

R1 (internal): 1kΩ	} f2: 3.4kHz	R2 (internal): 7.5kΩ	} f1: 21Hz
C1 (external): 0.047μF		C2 (external): 1μF	

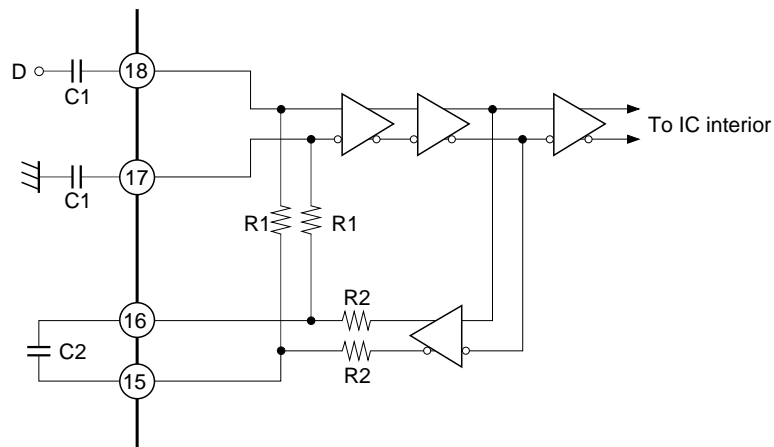


Fig. 1

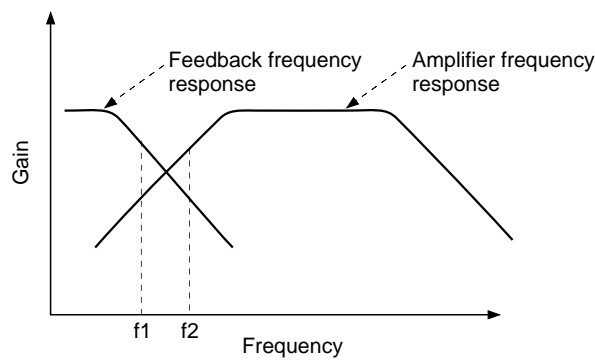


Fig. 2

2. Alarm block

In order to operate the alarm block, give the voltage difference between Pins 22 and 23 to set an alarm level and connect the peak hold capacitor C3 shown in Fig. 3.

This IC has two setting methods of alarm level; one is to connect Pin 24 to VEE and leave Pins 22 and 23 open to set an alarm level default value (8mV for input conversion). The other is to connect Pin 24 to VEE and set a desired alarm level using the external resistors REX1, REX2 and REX3 shown in Fig. 3. Connect REX1 between Pins 22 and 23 or connect REX3 between Pin 23 and Vcc when less alarm level is desired to be set than its default value; connect REX2 between Pin 22 and Vcc when more alarm level is desired to be set than its default value. However, the Pin 22 voltage must be higher than that of Pin 23.

This IC also features two-level setting of identification maximum voltage amplitude. The amplitude is set to 40mVp-p when Pin 3 is left open (High level) and it is set to 20mVp-p when Pin 3 is Low level. Therefore, the noise margin can be increased by setting Pin 3 to Low level when the small signal is input. The relation of input voltage and peak hold output voltage is shown in Fig. 5.

In the relation between the alarm setting level and hysteresis width, the hysteresis width is designed to maintain a constant gain (design target value: 6dB) as shown in Fig. 4.

This IC is designed to externally have the capacitor C3, and the C3 value should be set so as to obtain desired assert time and deassert time settings for the alarm signal.

The electrical characteristics for the SD response assert and deassert times are guaranteed only when the waveforms are input as shown in the timing chart of Fig. 6.

REX1: 100Ω (when the alarm level is set to 4mV for input conversion.)

REX2: 8kΩ (when the alarm level is set to 10mV for input conversion.)

REX3: 4kΩ (when the alarm level is set to 4mV for input conversion.)

C3: 470pF

The table below shows the alarm logic.

Optical signal input state	SD	$\overline{SD}$
Signal input	High level	Low level
Signal interruption	Low level	High level

The table below shows the output disable function logic.

Optical signal input state	Q	$\overline{Q}$
ODIS: Open High	Fixed Low	Fixed High
ODIS: Low	Data	$\overline{Data}$

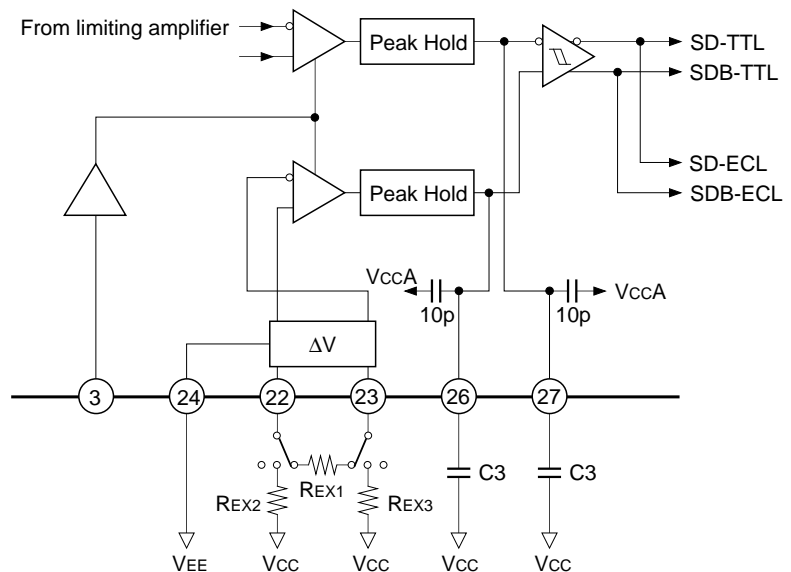
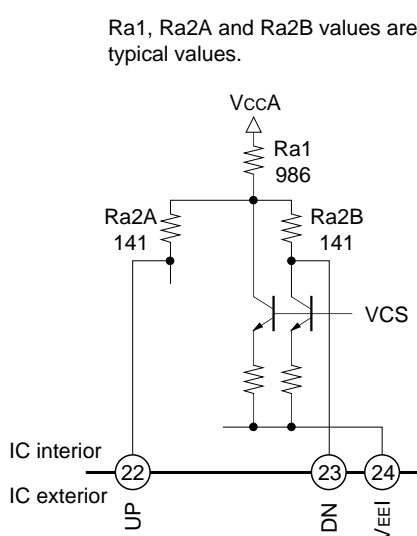


Fig. 3

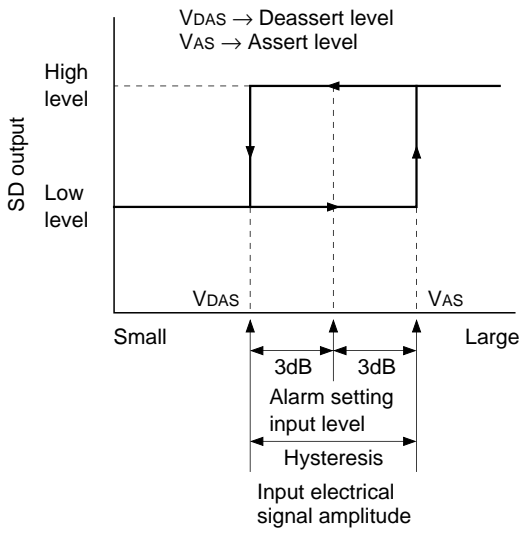


Fig. 4

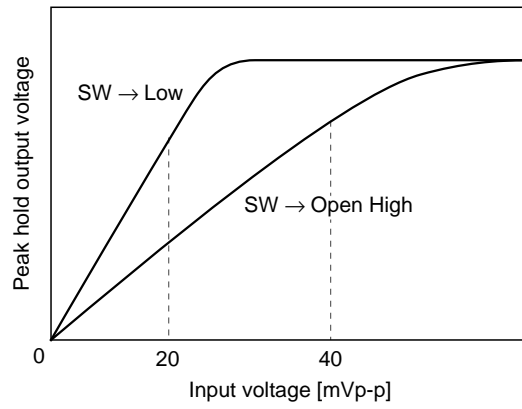


Fig. 5

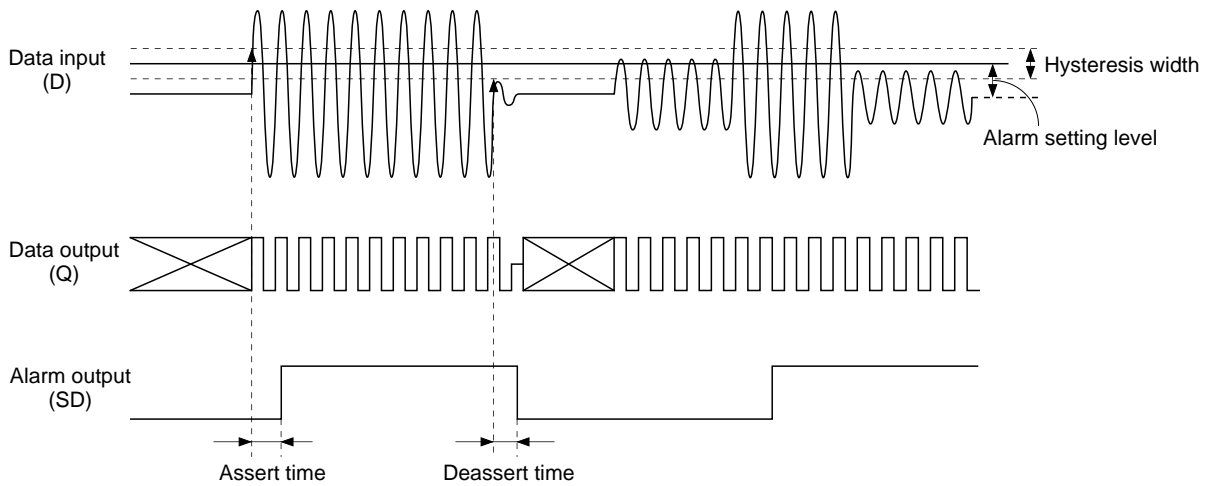
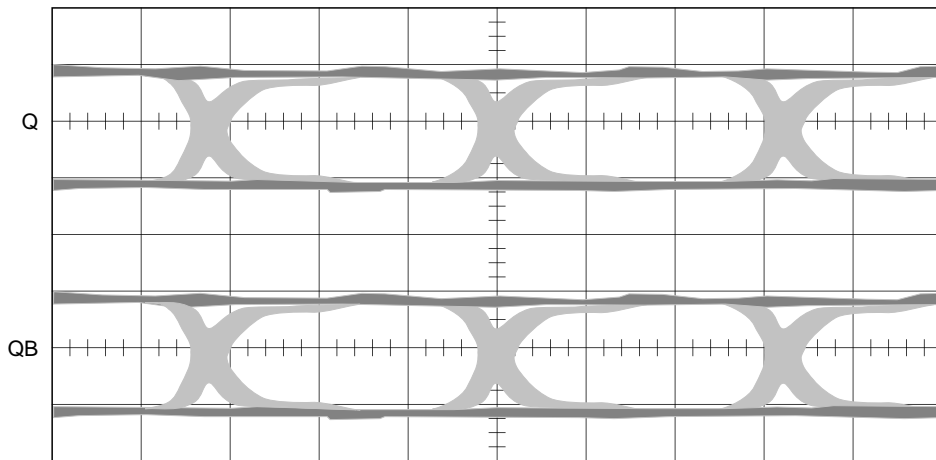


Fig. 6

Example of Representative Characteristics

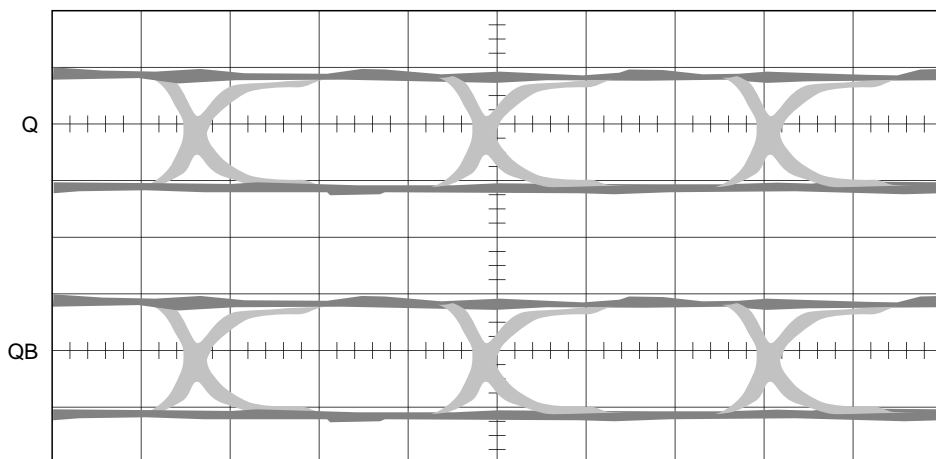
1. Q/QB output waveform



V<sub>CC</sub> = GND  
 V<sub>EE</sub> = -3.3V  
 V<sub>TT</sub> = -2V  
 T<sub>a</sub> = 27°C  
 D = 622Mbps  
 V<sub>in</sub> = 5mVp-p  
 Single input  
 pattern: PRBS2<sup>23</sup>-1  
 Q/QB = 50Ω to V<sub>TT</sub>

Ch. 1 = 400mV/div OFFSET = -1330mV, Ch. 2 = 400mV/div OFFSET = -1330mV, Timebase = 500ps/div

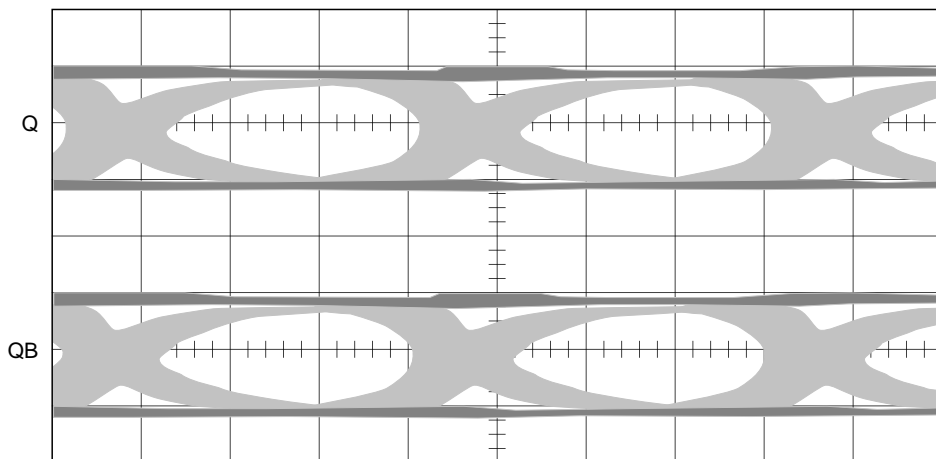
Fig. 7



V<sub>CC</sub> = GND  
 V<sub>EE</sub> = -3.3V  
 V<sub>TT</sub> = -2V  
 T<sub>a</sub> = 27°C  
 D = 622Mbps  
 V<sub>in</sub> = 10mVp-p  
 Single input  
 pattern: PRBS2<sup>23</sup>-1  
 Q/QB = 50Ω to V<sub>TT</sub>

Ch. 1 = 400mV/div OFFSET = -1330mV, Ch. 2 = 400mV/div OFFSET = -1330mV, Timebase = 500ps/div

Fig. 8

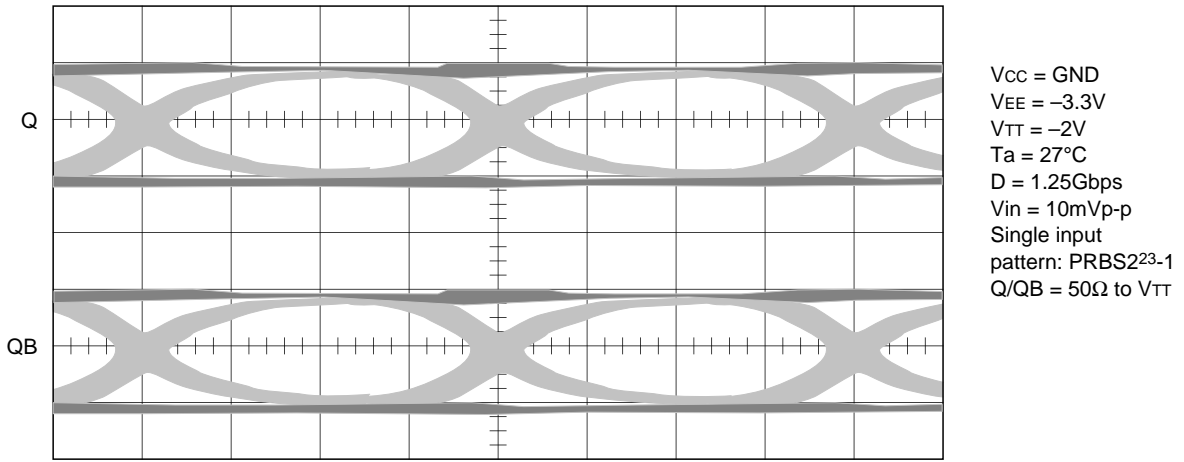


V<sub>CC</sub> = GND  
 V<sub>EE</sub> = -3.3V  
 V<sub>TT</sub> = -2V  
 T<sub>a</sub> = 27°C  
 D = 1.25Gbps  
 V<sub>in</sub> = 5mVp-p  
 Single input  
 pattern: PRBS2<sup>23</sup>-1  
 Q/QB = 50Ω to V<sub>TT</sub>

Ch. 1 = 400mV/div OFFSET = -1330mV, Ch. 2 = 400mV/div OFFSET = -1330mV, Timebase = 200ps/div

Fig. 9





Ch. 1 = 400mV/div OFFSET = -1330mV, Ch. 2 = 400mV/div OFFSET = -1330mV, Timebase = 200ps/div

Fig. 10

2. Bit error rate

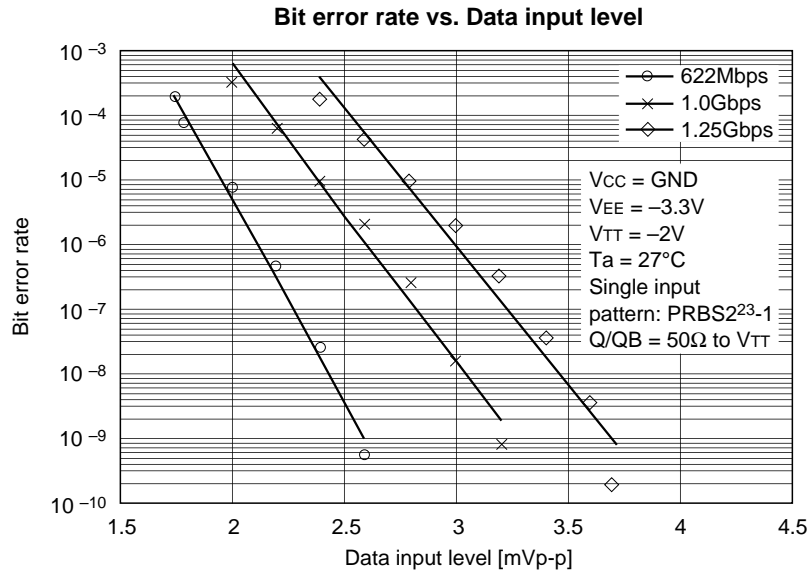


Fig. 11

3. Alarm level

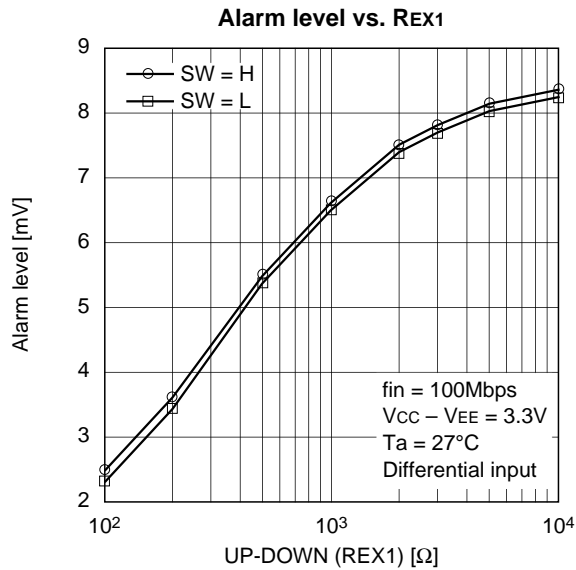


Fig. 12

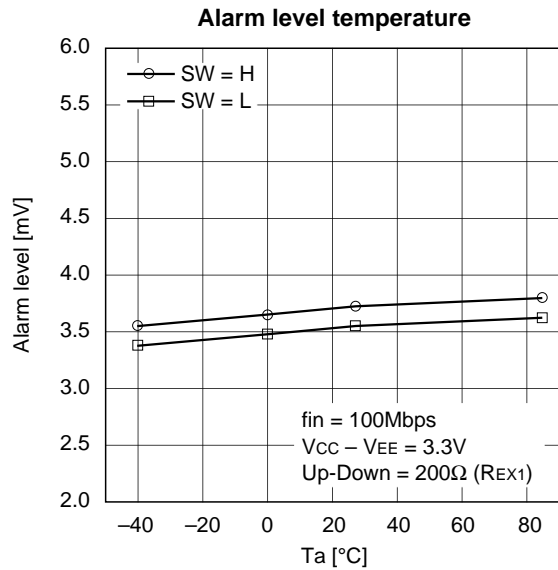


Fig. 13

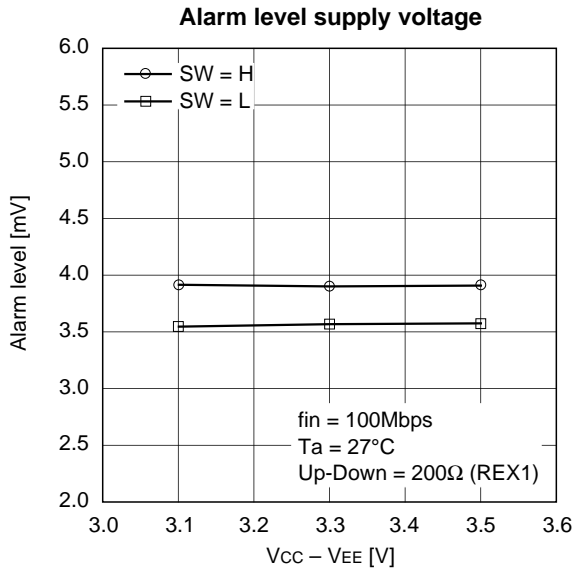


Fig. 14

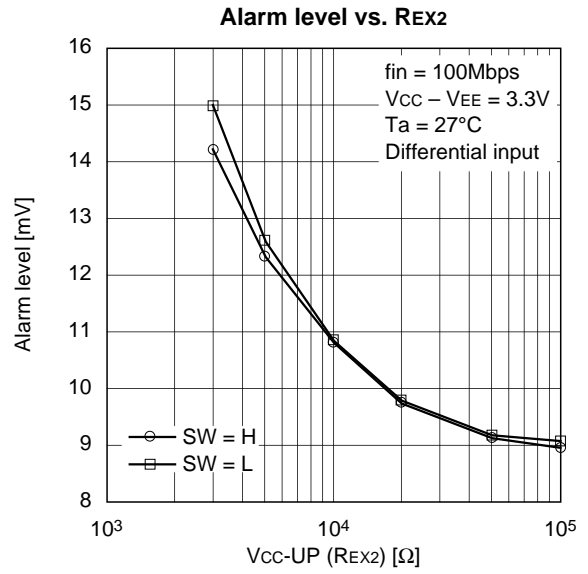


Fig. 15

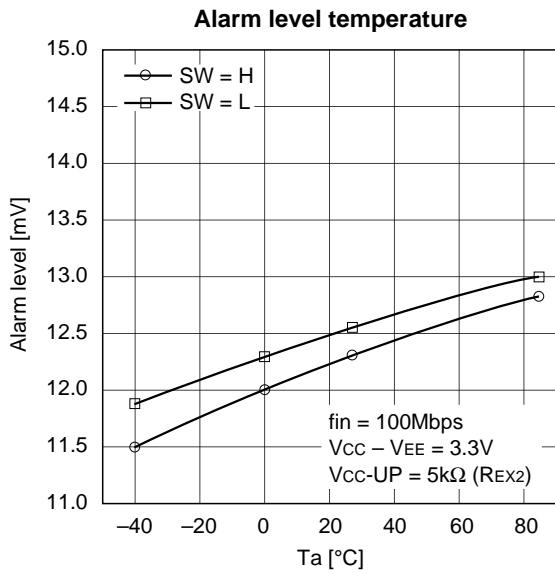


Fig. 16

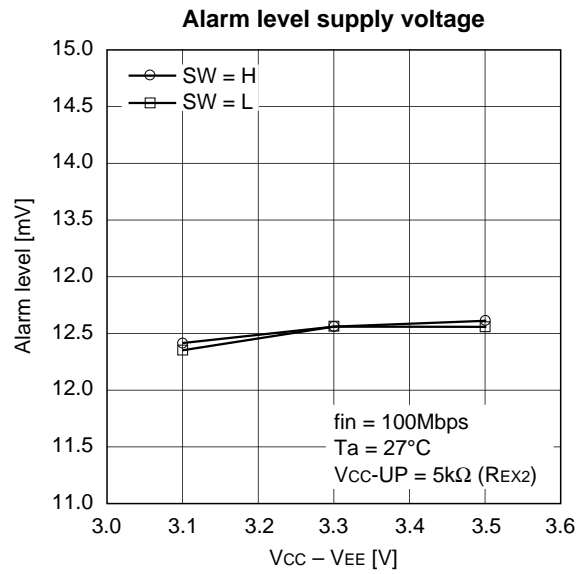


Fig. 17

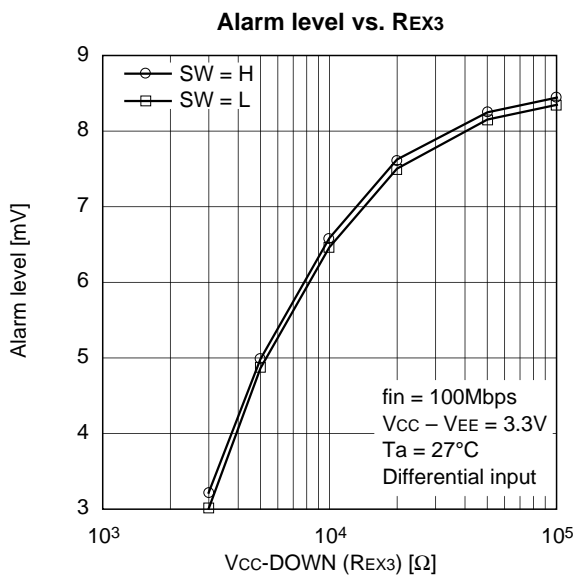


Fig. 18

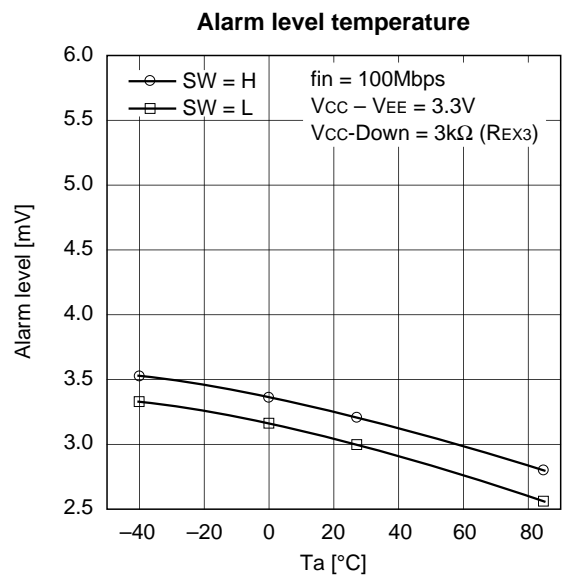


Fig. 19

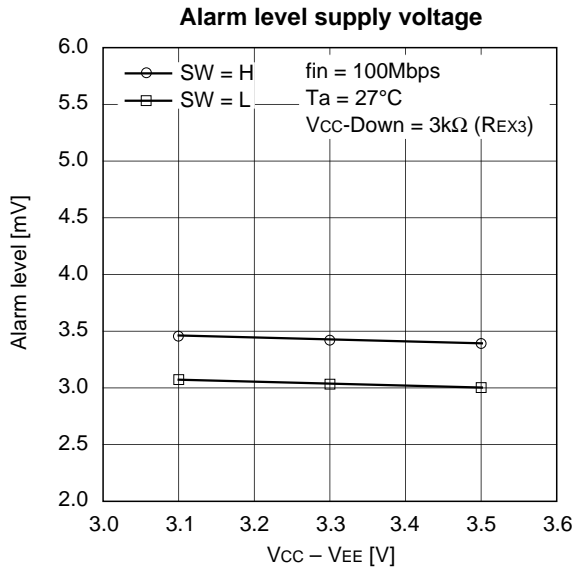


Fig. 20

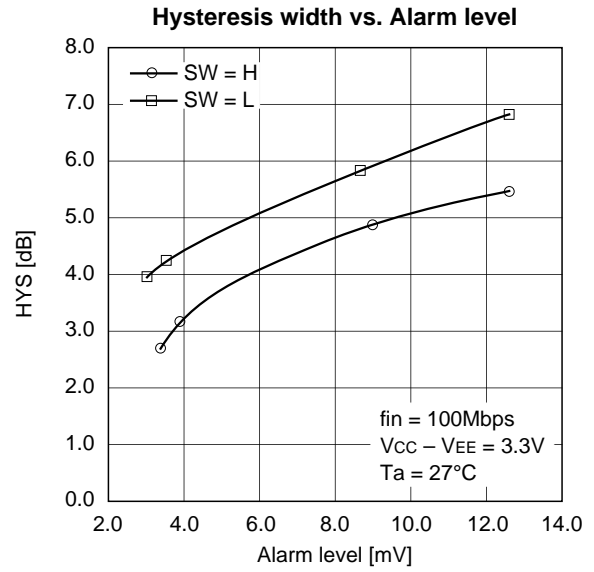


Fig. 21

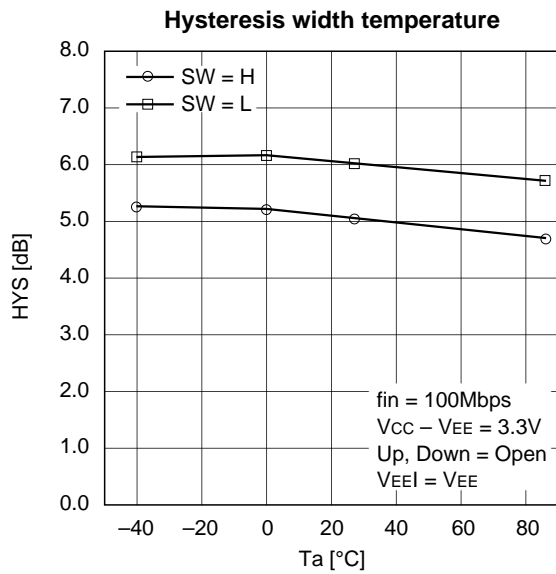


Fig. 22

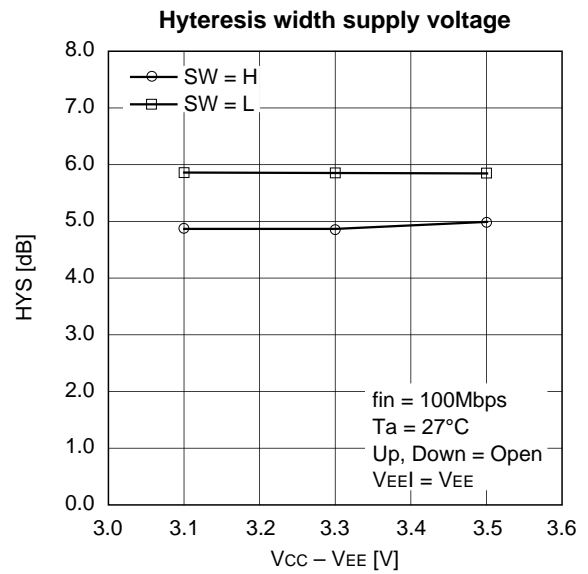


Fig. 23

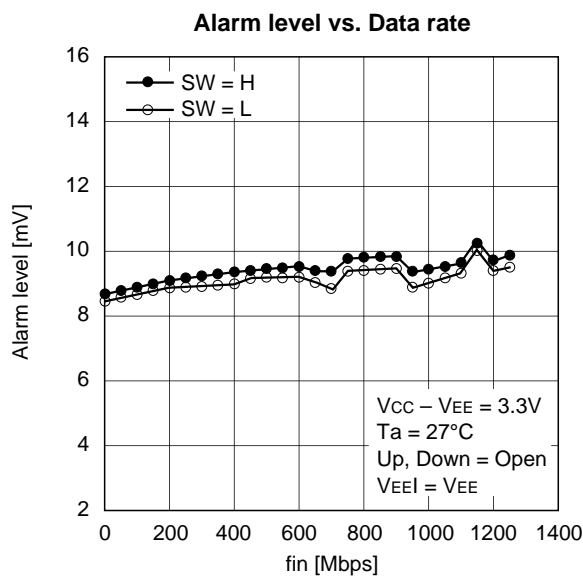


Fig. 24

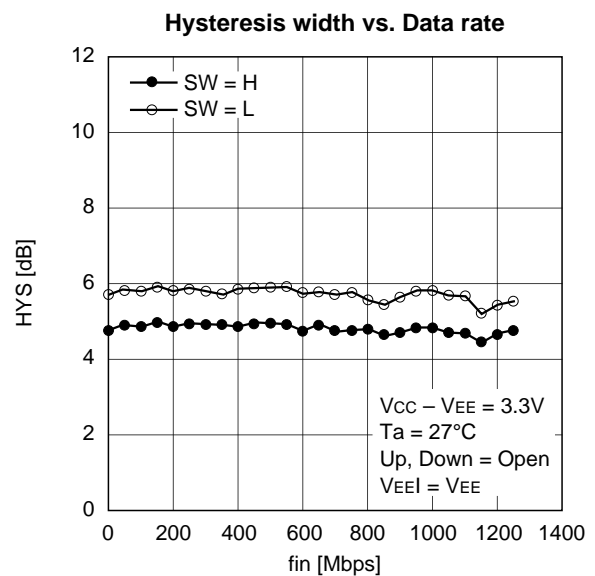


Fig. 25

4. DC voltage

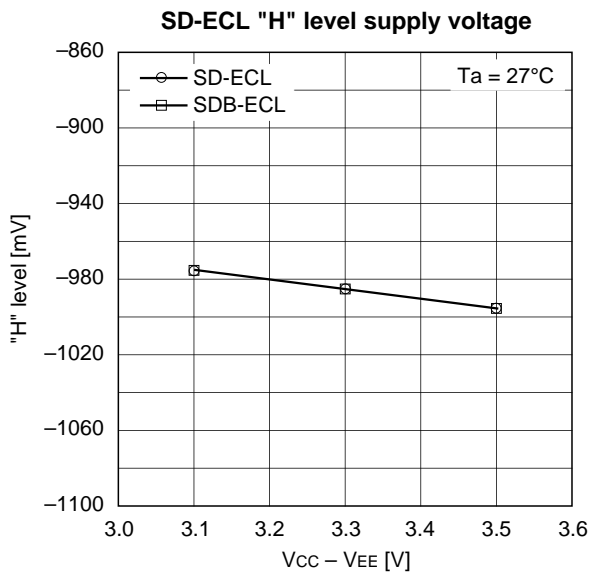


Fig. 26

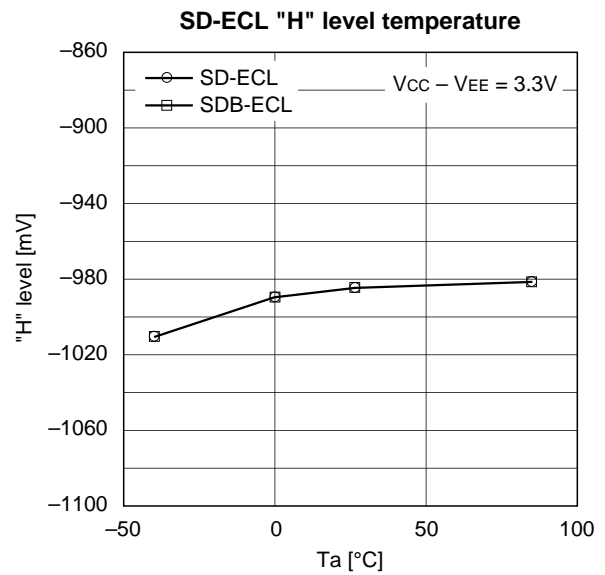


Fig. 27

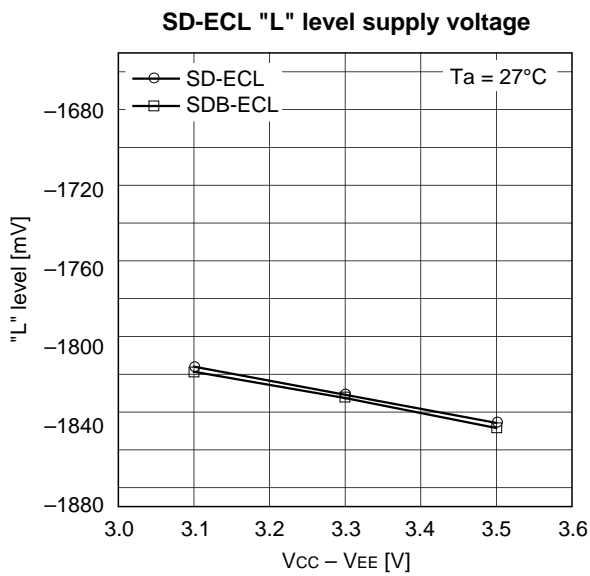


Fig. 28

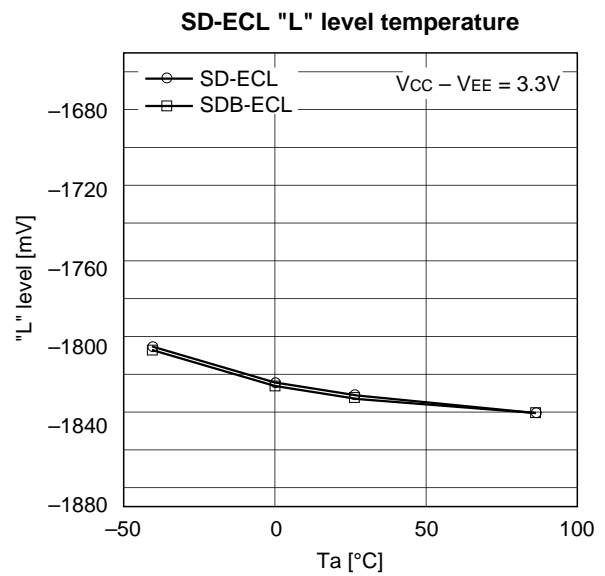


Fig. 29

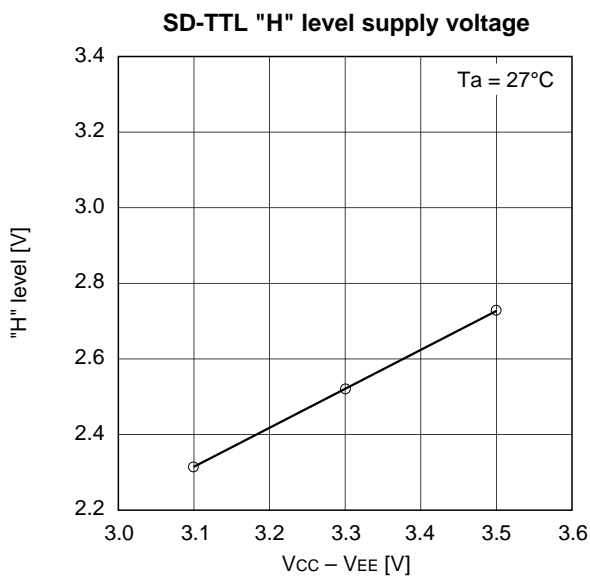


Fig. 30

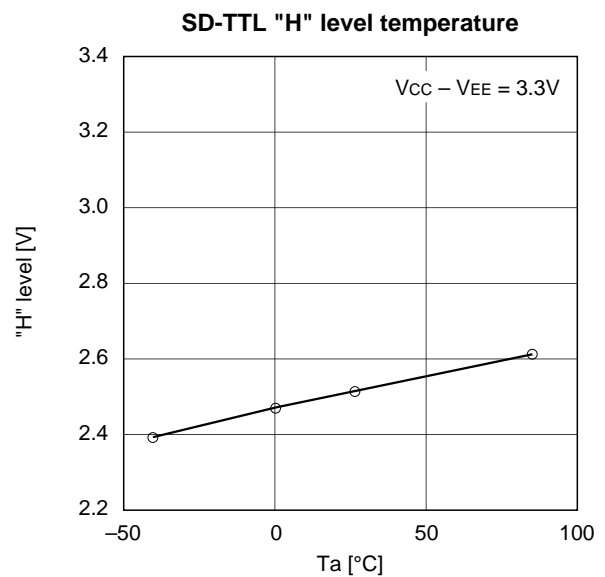


Fig. 31

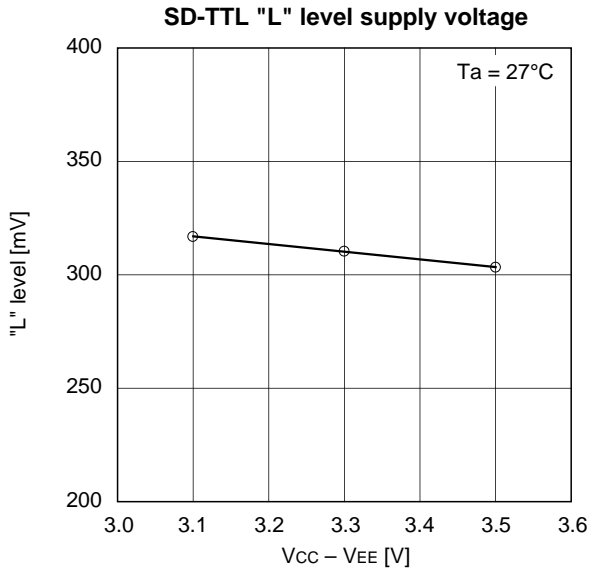


Fig. 32

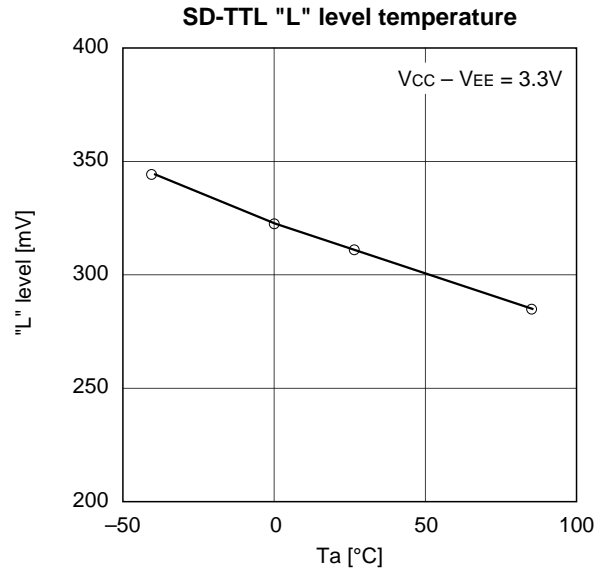


Fig. 33

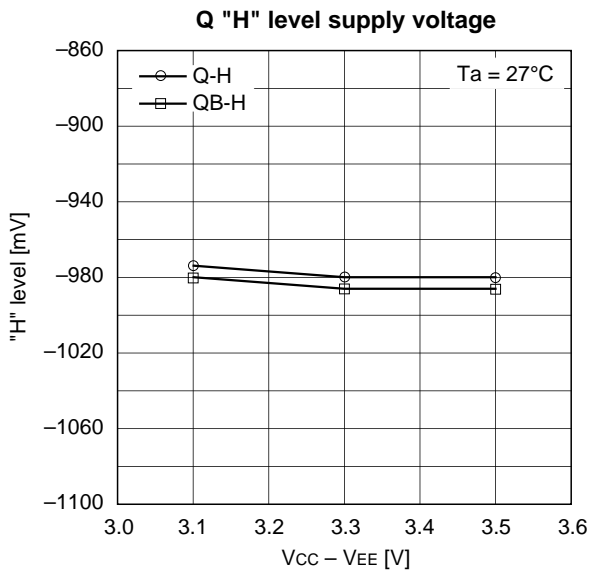


Fig. 34

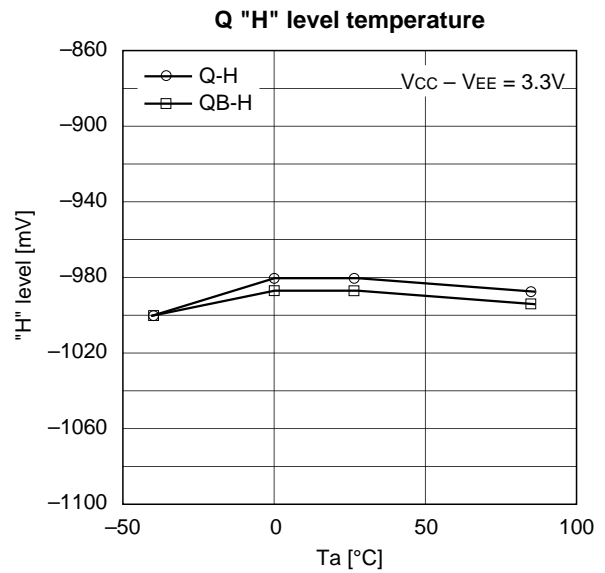


Fig. 35

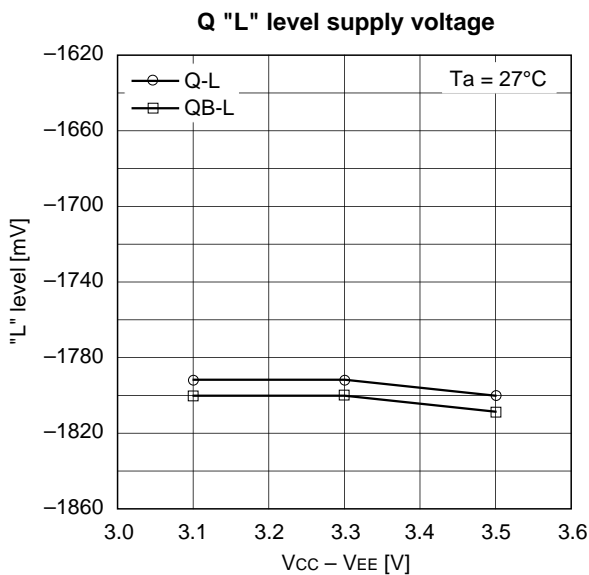


Fig. 36

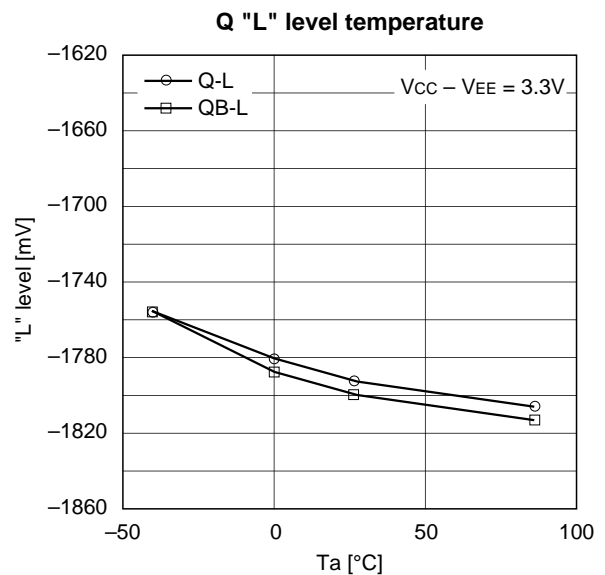
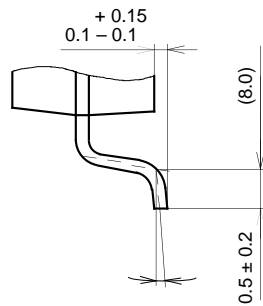
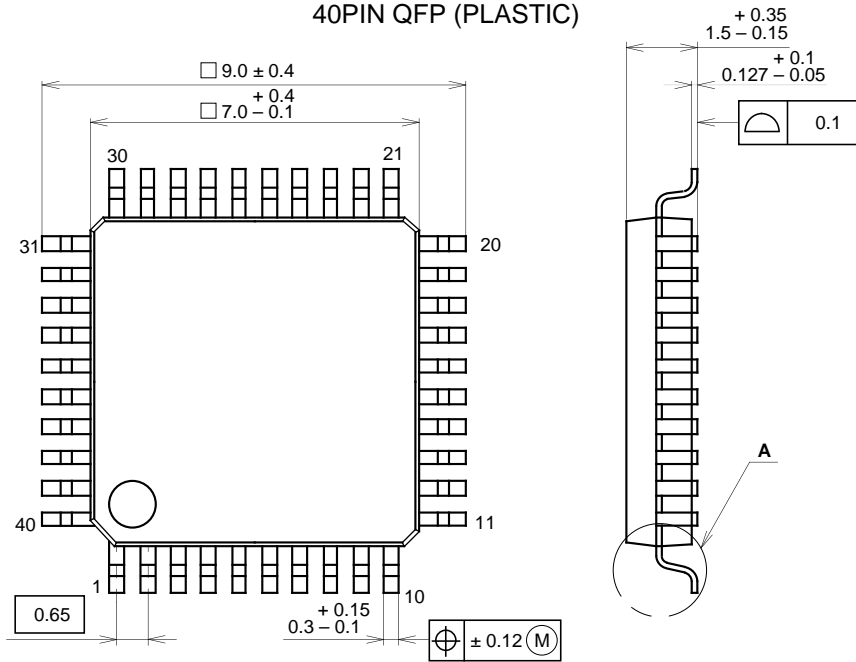


Fig. 37

Package Outline

Unit: mm

40PIN QFP (PLASTIC)



DETAIL A

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g

SONY CODE	QFP-40P-L01
EIAJ CODE	QFP040-P-0707
JEDEC CODE	_____

NOTE : PALLADIUM PLATING

This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).