CMOS LSI

LC89585

CD Encoder LSI for CD-R Systems

Overview

The LC89585 is an LSI that implements the digital processing required for CD-R recording in conformance with the orange book specifications. The LC89585 adds subcode data to record data processed by an A/D converter and the built-in DIR (digital audio interface receiver), FS decoder, and CD decoder circuits, and converts that data to CIRC (cross-interleave reed-solomon code) data. The LC89585 then performs EFM (eight-to-fourteen modulation encoding) conversion in real time.
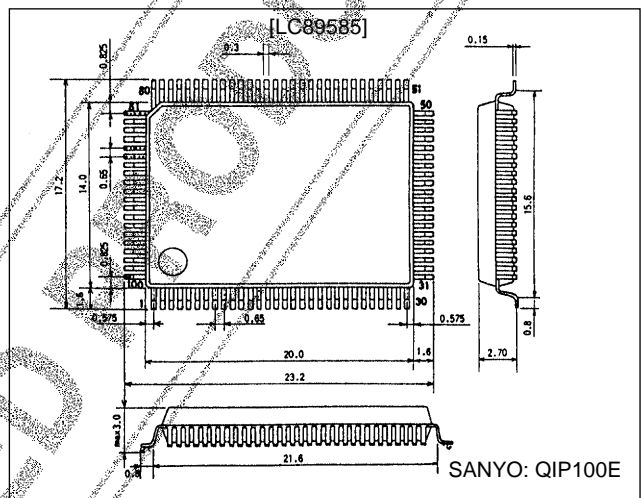
Features

- A/D converter clock generation
- Built-in DIR (conforming to the IEC958 standard) and DIT (Digital audio interface transmitter)
- Built-in fader and muting circuits
- On-chip buffer RAM for encoder processing
- Automatic linking position processing function
- CCB CPU interface

Package Dimensions

unit: mm

3151-QFP100E

SANYO: QIP100E

Specifications

Absolute Maximum Ratings at $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	Ta = 25°C	−0.3 to +7.0	V
I/O voltages	V_I, V_O	Ta = 25°C	−0.3 to V_{DD} + 0.3	V
Operating temperature	Topr		−30 to +70	°C
Storage temperature	Tstg		−55 to +125	°C
Soldering temperature resistance		10 seconds (pins only)	260	°C

Allowable Operating Ranges at Ta = −30 to +70°C, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.5	—	5.5	V
Input voltage	V_{IN}		0	—	V_{DD}	V

DC Electrical Characteristics at Ta = –30 to +70°C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
High-level input voltage	$V_{IH}1$	*1	2.2	—	V_{DD} + 0.3	V
Low-level input voltage	$V_{IL}1$	*1	−0.3	—	+0.8	V
High-level input voltage	$V_{IH}2$	*2	0.7 V_{DD}	—	V_{DD} + 0.3	V
Low-level input voltage	$V_{IL}2$	*2	−0.3	—	0.3 V_{DD}	V
High-level input voltage	$V_{IH}3$	*3	0.8 V_{DD}	—	V_{DD} + 0.3	V
Low-level input voltage	$V_{IL}3$	*3	−0.3	—	0.2 V_{DD}	V
High-level output voltage	$V_{OH}1$	I_{OH} = −1 µA, *4	V_{DD} − 0.05	—	—	V
Low-level output voltage	$V_{OL}1$	I_{OL} = +1 µA, *4	—	—	V_{SS} + 0.05	V
High-level output voltage	$V_{OH}2$	I_{OH} = −20 µA, *5	V_{DD} − 0.05	—	—	V
Low-level output voltage	$V_{OL}2$	I_{OL} = +20 µA, *5	—	—	V_{SS} + 0.05	V

Note: 1. The DIN1 to DIN4, ENCVCOIN, JITVCOIN, A0 to A9, DQ1 to DQ4, $\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$ and $\overline{WR}$ input pins.
2. Input pins other than DIN1 to DIN4, ENCVCOIN, JITVCOIN, A0 to A9, DQ1 to DQ4, $\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$, $\overline{WR}$, $\overline{RESET}$, CCB, CE, CL, DI, DIRRC1 and XTALIN.
3. The $\overline{RESET}$, CCB, CE, CL, DI, DIRRC1 and XTALIN input pins.
4. Output pins other than JITLPFO and ENCLPFO.
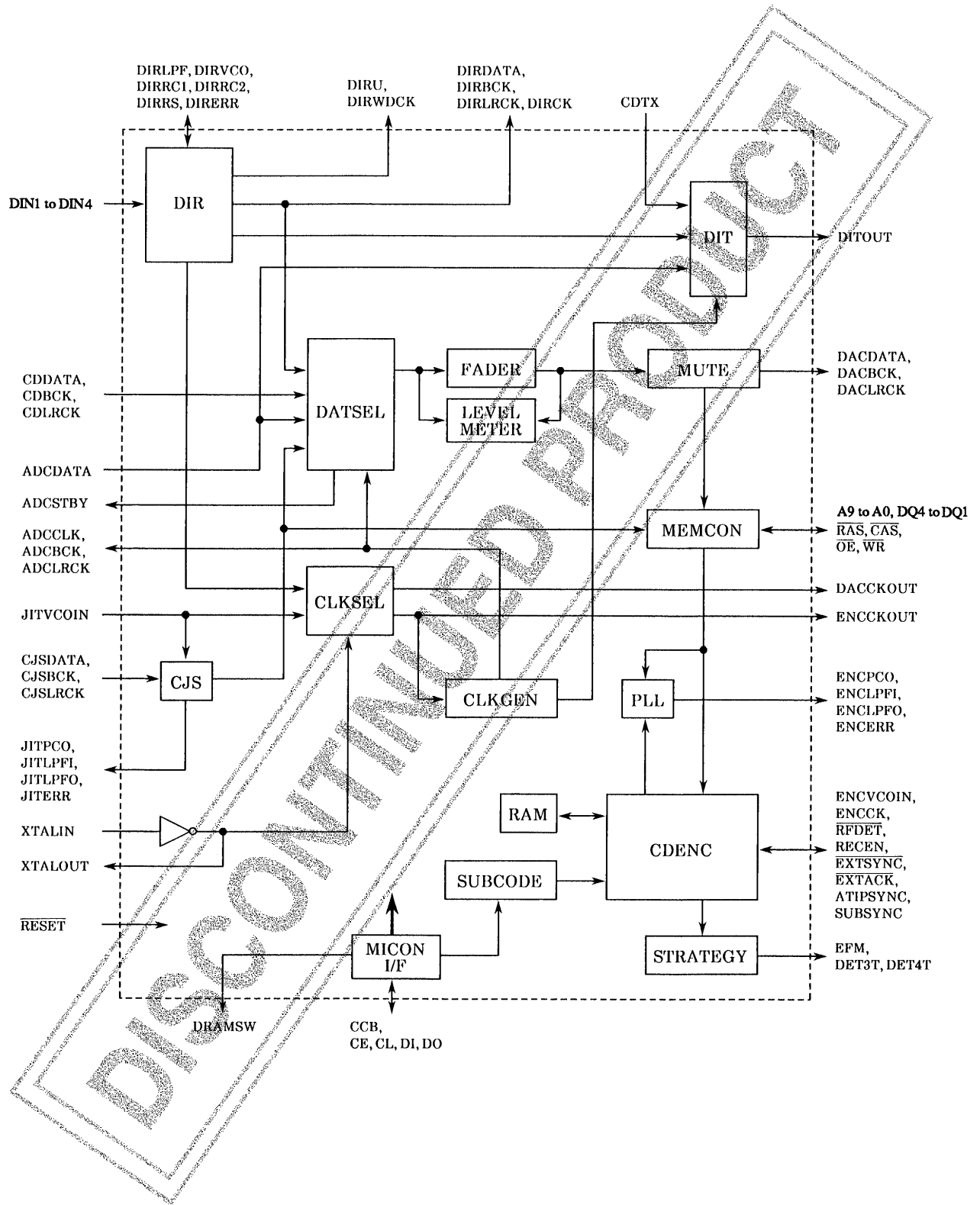5. The JITLPFO and ENCLPFO output pins.

Pin Assignment
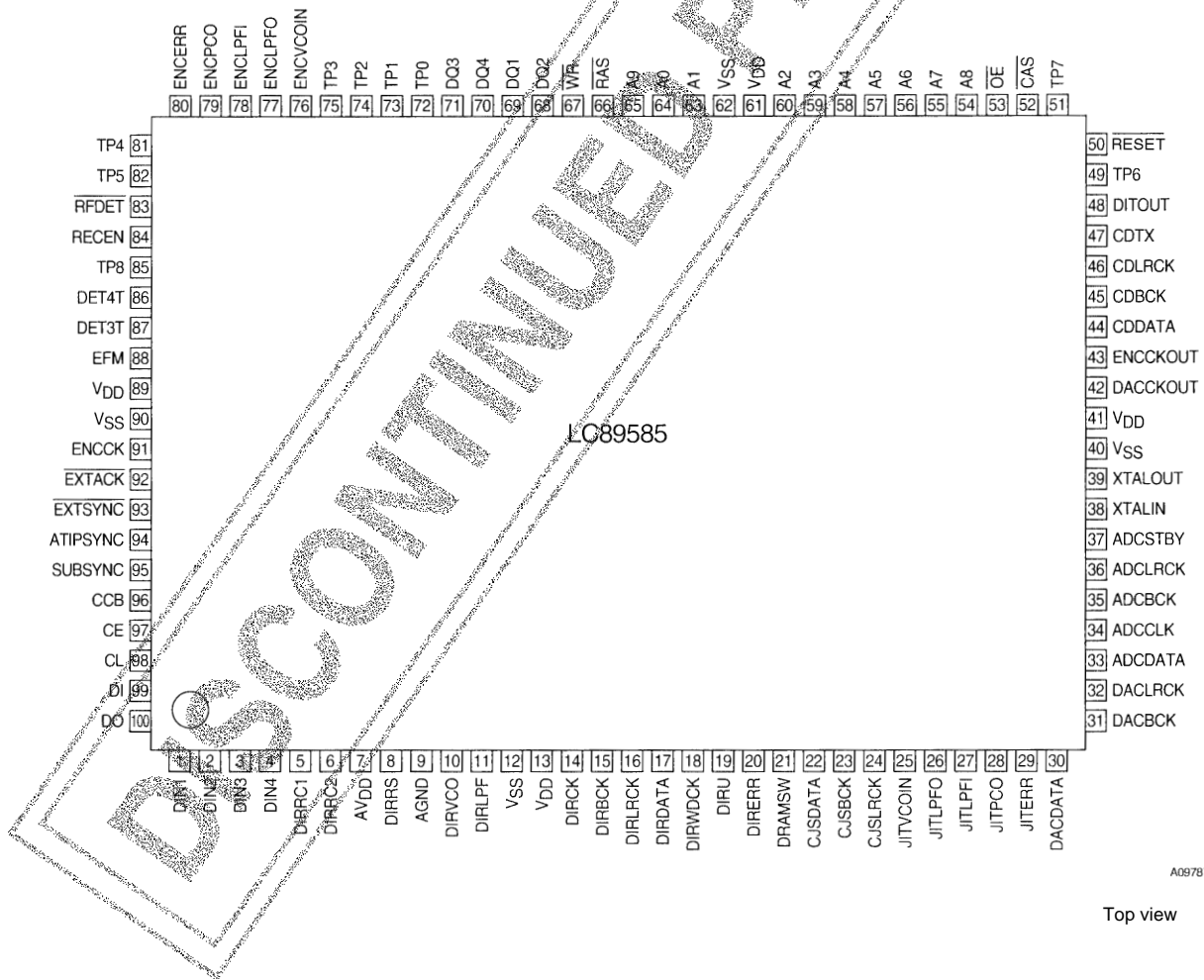
Top view
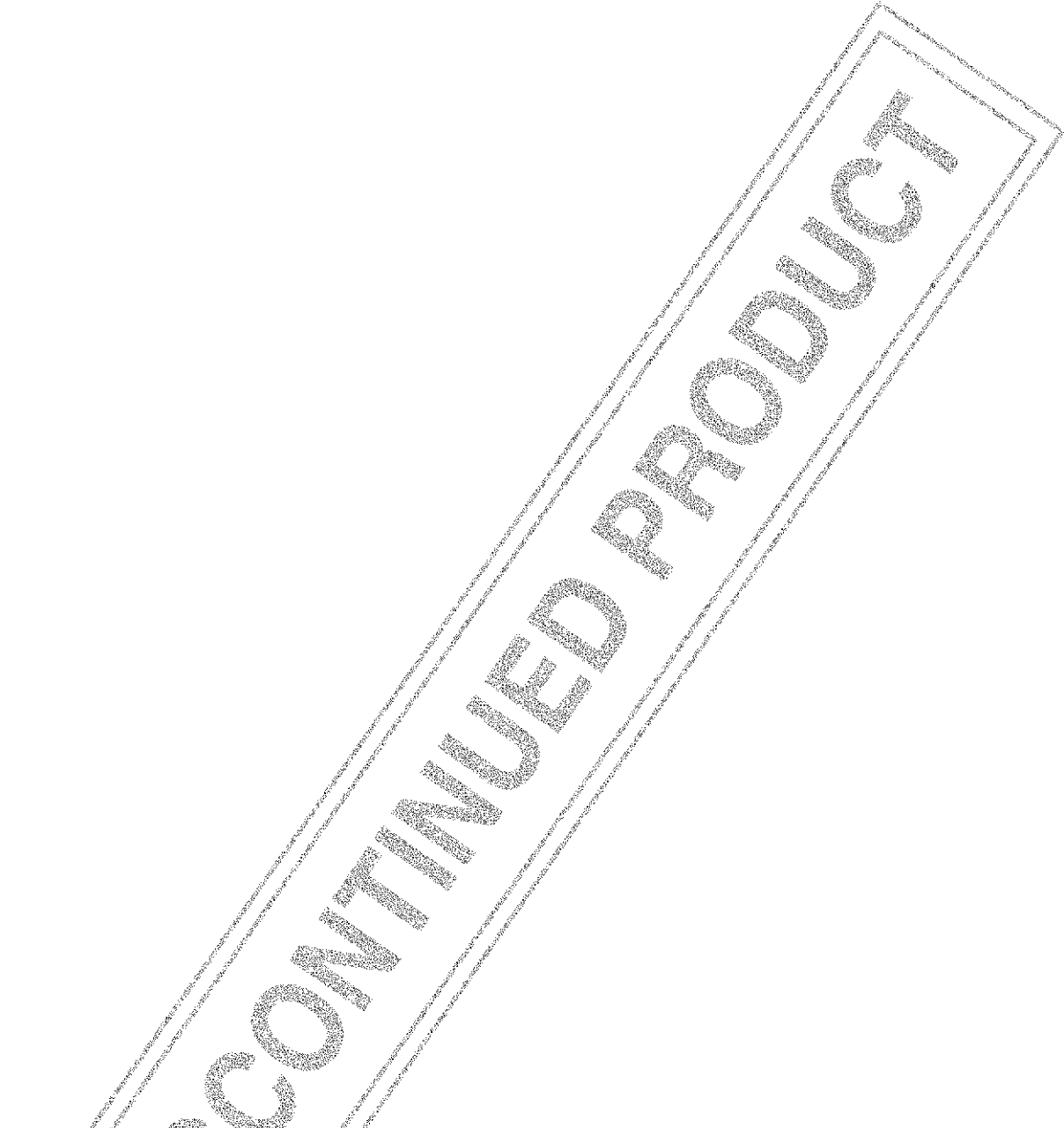
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System Block Diagram

Pin Functions

Pin No.	Symbol	I/O	Function
1	DIN1	I	Optical module data input
2	DIN2	I	Optical module data input
3	DIN3	I	Optical module data input
4	DIN4	I	Optical module data input
5	DIRRC1	I	RC oscillator input
6	DIRRC2	O	RC oscillator output
7	AV_{DD}	—	Analog system power supply
8	DIRRS	I	VCO oscillation band adjustment input
9	AGND	—	Analog system ground
10	DIRVCO	I	VCO free-running frequency setting input
11	DIRLPF	O	PLL low-pass filter connection
12	V_{SS}	—	Ground
13	V_{DD}	—	+5 V power supply
14	DIRCK	O	DIR system clock output
15	DIRBCK	O	DIR bit clock output
16	DIRLRCK	O	DIR L/$\overline{R}$ clock output
17	DIRDATA	O	DIR demodulated data output
18	DIRWDCK	O	DIR word clock output
19	DIRU	O	U-bit output
20	DIRERR	O	Data error and lock state monitor output
21	DRAMSW	O	External DRAM capacity setting output
22	CJSDATA	I	Clock jitter sub-laser data input
23	CJSBCK	I	Clock jitter sub-laser bit clock input
24	CJSLRCK	I	Clock jitter sub-laser L/$\overline{R}$ clock input
25	JITVCOIN	I	VCO input
26	JITLPFO	O	Low-pass filter output
27	JITLPFI	I	Low-pass filter input
28	JITPCO	O	Phase comparator output
29	JITERR	O	Lock state monitor output
30	DACDATA	O	D/A converter data output
31	DACBCK	O	D/A converter bit clock output
32	DACLRCK	O	D/A converter L/$\overline{R}$ clock output
33	ADCDATA	I	A/D converter record data input
34	ADCCLK	O	A/D converter clock output
35	ADCBCK	O	A/D converter bit clock output
36	ADCLRCK	O	A/D converter L/$\overline{R}$ clock output
37	ADCSTBY	O	A/D converter standby signal output
38	XTALIN	I	System clock input
39	XTALOUT	O	System clock output
40	V_{SS}	—	Ground
41	V_{DD}	—	+5 V power supply
42	DACCKOUT	O	D/A converter system clock output
43	ENCCKOUT	O	CD decoder system clock output
44	CDDATA	I	CD decoder data input
45	CDBCK	I	CD decoder bit clock input
46	CDLRCK	I	CD decoder L/$\overline{R}$ clock input
47	CDTX	I	Signal input from the CD decoder output
48	DITOUT	O	Biphase modulation output
49	TP6	I	Test pin
50	$\overline{RESET}$	I	System reset input

Continued from preceding page.

Pin No.	Symbol	I/O	Function
51	TP7	I	Test pin
52	$\overline{CAS}$	O	DRAM column address strobe signal output
53	$\overline{OE}$	O	DRAM output enable signal output
54	A8	O	DRAM address outputs
55	A7	O	
56	A6	O	
57	A5	O	
58	A4	O	
59	A3	O	
60	A2	O	
61	V_{DD}	—	+5 V power supply
62	V_{SS}	—	Ground
63	A1	O	DRAM address outputs
64	A0	O	
65	A9	O	
66	$\overline{RAS}$	O	DRAM row address strobe signal output
67	$\overline{WR}$	O	DRAM read/write signal output
68	DQ2	I/O	DRAM data I/O
69	DQ1	I/O	
70	DQ4	I/O	
71	DQ3	I/O	
72	TP0	I	Test pin
73	TP1	I	
74	TP2	I	
75	TP3	O	
76	ENCVCOIN	I	Encoder circuit clock input
77	ENCLPFO	O	Low-pass filter output
78	ENCLPFI	I	Low-pass filter input
79	ENCPCO	O	Phase comparator output
80	ENCERR	O	Lock state monitor output
81	TP4	O	Test pin
82	TP5	I	
83	$\overline{RFDET}$	I	RF signal input
84	RECEN	I	Record enable signal input
85	TP8	O	Test pin
86	DET4T	O	4T detection signal output
87	DET3T	O	3T detection signal output
88	EFM	O	EFM signal output
89	V_{DD}	—	+5 V power supply
90	V_{SS}	—	Ground
91	ENCCK	O	Encoder clock output
92	$\overline{EXTACK}$	O	ATIP synchronization reporting signal output
93	$\overline{EXTSYNC}$	I	ATIP synchronization enable signal input
94	ATIPSYNC	I	ATIP synchronization signal input
95	SUBSYNC	O	Subcode synchronization signal output
96	CCB	I	CPU interface type switching signal input
97	CE	I	CPU interface chip enable signal input
98	CL	I	CPU interface data transfer clock input
99	DI	I	CPU interface data input
100	DQ	O	CPU interface data output

This catalog provides information as of January, 1998. Specifications and information herein are subject to change without notice.