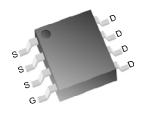


LVS2100N N-Channel PowerJFET®

Product Summary

	Typical	Max	
V_{DS}		24	V
R _{DS(ON)} @ 0 V _{GS}	11.5	14	mΩ

Pinouts





SO-8

Features

- Device is fully on @ $V_{GS} = 0V$.
- Bidirectional blocking when off (no body diode)

Applications

Notebook battery switch:
Each JFET replaces 2 P-Channel series MOSFETs

Absolute Maximum Ratings

Absolute maximum ratings are the values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Symbol	Parameter	Conditions	Rating	Units
V _{DSS}	Drain to Source voltage		24	V
V_{GS}	Gate to Source voltage		-12	V
V_{DG}	Drain to Gate voltage		-28	V
I _D	Drain Current	Continuous, T _C = 25°C	11	Α
		Pulsed, 300µS	50	Α
T _J	Junction Temperature		-55 to 150	°C
T _{STG}	Storage Temperature		-65 to 150	°C
	Lead Soldering Temperature	10 seconds, 1.6mm from case	260	°C
P _D	Power Dissipation	T _A = 25°C, Note 1	2.5	W
		T _A = 25°C, Note 2	1.3	W

Thermal Resistance

Symbol	Resistance from:	Conditions	Rating	Units
$R_{\theta JA}$	Junction to Ambient	Note 1	50	°C/W
		Note 2	96	°C/W
$R_{\theta JC}$	Junction to Case		25	°C/W

Note 1. Mounted on 1 in.², 2 oz copper on FR-4

Note 1. Mounted on 0.05 in.2, 0.5 oz. copper on FR-4

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Electrical Specifications @T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Тур	Max	Units
Static				-	•	1
BV _{DSX}	Breakdown Voltage Drain to Source	$I_D = 0.5 \text{ mA}, V_{GS} = -4 \text{ V}$	24	28		V
BV_GDO	Breakdown Voltage Gate to Drain	$I_G = -50 \mu A$		-32	-28	V
BV _{GSO}	Breakdown Voltage Gate to Source	$I_G = -50 \mu A$		-14	-12	V
R _{DS(ON)}	Drain to Source On Resistance	$V_{GS} = 0V, I_{D} = -7A$		11.5	14	mΩ
		$V_{GS} = 0V$, $I_D = 7A$		13	17	mΩ
V _{GS(OFF)}	Gate Threshold Voltage	$V_{DS} = 16 \text{ V}, I_D = 250 \mu\text{A}$		-2.5		V
Dynamic	;					
Q _G	Total Gate Charge	ΔV_{GS} = 5V, V_{DS} = 15V		9.3		nC
Q_{GD}	Gate to Drain charge	$\Delta V_{DS} = 12V$		6.1		nC
Q _{GS}	Gate to Source Charge			3.2		nC
R _G	Gate resistance			3		Ω
T _{D(ON)}	Turn-on Delay	I _D =15A		4		nS
T _{D(OFF)}	Turn-off Delay	Circuit of Figure 1		9		
T _R	Rise Time	=		2		
T _F	Fall Time	=		7		
C _{ISS}	Input Capacitance			860		pF
Coss	Output Capacitance			350		pF
C _{GS}	Gate-Source Capacitance			588		pF
C_GD	Gate-Drain Capacitance			272		pF
C _{DS}	Drain-Source Capacitance			15		pF

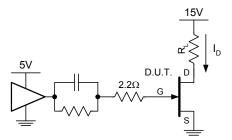
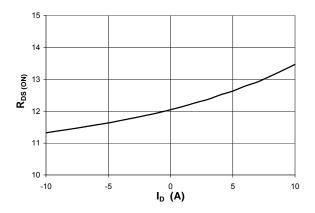


Figure 1. Switching test circuit.



Typical Characteristics $@T_J = 25^{\circ}C$ (unless otherwise specified)



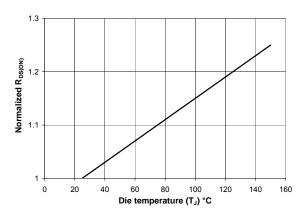
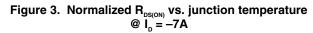


Figure 2. $R_{DS(ON)}$ vs. Drain Current @V_{GS} = 0V



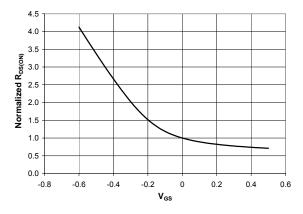


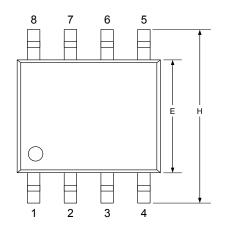
Figure 4. Normalized $R_{DS(ON)}$ vs. @ $I_D = -7A$

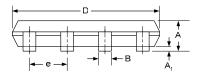


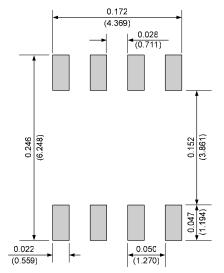
Dimensional Outline Drawing

SO-8 8-lead narrow SOIC

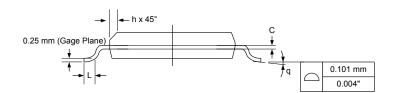
	Millimeters		Inches	
Dim	Min	Max	Min	Max
Α	1.35	1.75	0.0530	0.0690
A1	0.10	0.20	0.0040	0.0080
В	0.35	0.51	0.0140	0.0200
С	0.19	0.25	0.0075	0.0100
D	4.80	5.00	0.1890	0.1960
Е	3.80	4.00	0.1500	0.1570
е	1.27 BSC		0.050 BSC	
Н	5.80	6.20	0.2280	0.2440
h	0.25	0.50	0.0100	0.0200
L	0.50	0.93	0.0200	0.0370
q	0°	8°	0°	8°







Recommended minimum pad layout dimensions in inches (mm)



Conforms to JEDEC part number MS-012



Ordering Information

Part Number	Package	Packing
LVS2001N	SO-8	13" Tape and Reel, 2500 units / reel

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- A critical component in any component of a life support, device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.