April 1990
Edition 3.0

FUJITSU

DATA SHEET

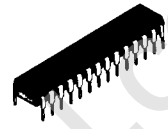
MB81C79A-35/-45
CMOS 72K-BIT HIGH-SPEED SRAM

8K Words x 9 Bits High-Speed CMOS Static Random Access Memory with Automatic Power Down

The Fujitsu MB81C79A is a 8,192 words x 9 bits static random access memory fabricated with a CMOS process. The memory uses asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

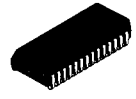
A separate chip select ($\overline{CS_1}$) pin simplifies multipackage systems design by permitting the selection of an individual package when outputs are OR-tied, and then automatically powering down the other deselected packages.

- Organization: 8,192 words x 9 bits
- Static operation: no clocks or refresh required
- Access time: $t_{AA} = t_{ACS1} = 35$ ns max. (MB81C79A-35)
  $t_{ACS2} = t_{OE} = 45$ ns max. (MB81C79A-45)
- Low power consumption: 495 mW max. (Operating)
  138 mW max. (Standby, TTL level)
  83 mW max. (Standby, CMOS level)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capacity
- Chip select for simplified memory expansion, automatic power down
- Electrostatic protection for all inputs and outputs
- Standard 28-pin Plastic Packages:
  Skinny DIP (300 mil) MB81C79A-xxPSK
  SOP MB81C79A-xxPF
  SOJ MB81C79A-xxPJ
- Standard 32-pad Ceramic Package:
  LCC (metal seal) MB81C79A-CV



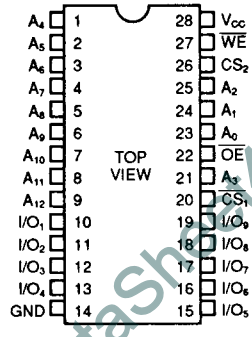
PLASTIC PACKAGE
DIP-28P-M04

PLASTIC PACKAGE
FPT-28P-M02



PLASTIC PACKAGE
LCC-28P-M04

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Absolute Maximum Ratings (See Note)

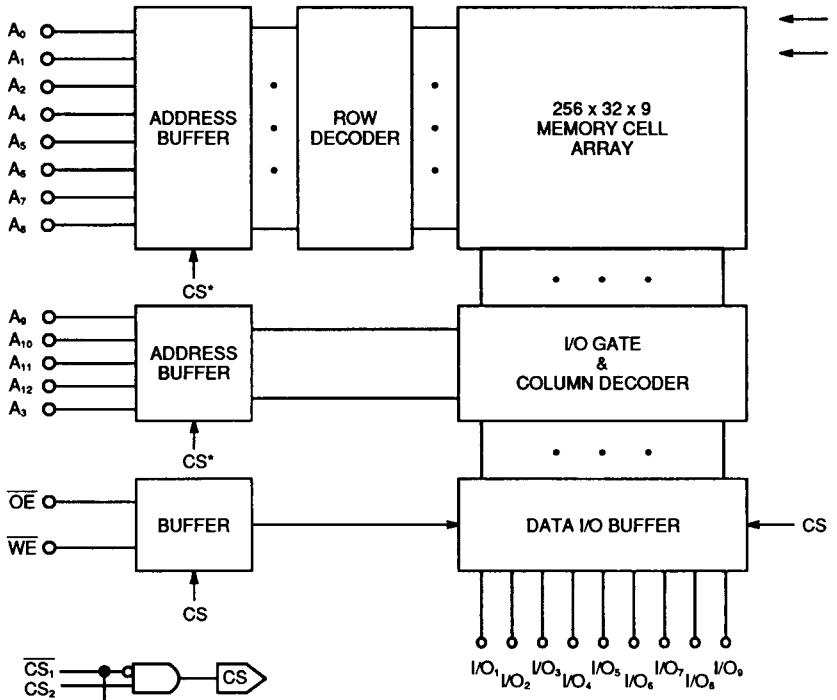
Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage on any pin with respect to GND		V_{IN}	−3.5 to +7.0	V
Output Voltage on any I/O pin with respect to GND		V_{OUT}	−0.5 to +7.0	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature Range	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−40 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Copyright © 1990 by FUJITSU LIMITED and Fujitsu Microelectronics, Inc.

1

Fig. 1 – MB81C79A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O STATE
H	X	X	X	STANDBY	I_{SB}	HIGH-Z
L	L	X	X	DESELECT	I_{CC}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	H	L	READ	I_{CC}	D_{OUT}
L	H	L	X	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN}=0V) ($\overline{CS_1}$, CS_2, $\overline{OE}$, $\overline{WE}$)	C_{I1}		7	pF
Input Capacitance (V_{IN}=0V) (Other Inputs)	C_{I2}		6	pF
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$		8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

1

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Condition
Input Leakage Current	I_{LI}	−10	10	µA	V_{IN}=0V to V_{CC}, V_{CC}=Max.
Output Leakage Current	I_{LO}	−10	10	µA	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V to V_{CC}
Operating Supply Current	I_{CC}		90	mA	$\overline{CS_1}$=V_{IL} I/O=Open, Cycle=Min
Standby Supply Current	I_{SB1}		15	mA	V_{CC}=Min to Max. $\overline{CS_1}$=V_{CC} −0.2V V_{IN}≤0.2V or V_{IN}≥V_{CC} −0.2V
	I_{SB2}		25	mA	$\overline{CS_1}$=V_{IH}
Input Low Voltage	V_{IL}	−2.0*	0.8	V	
Input High Voltage	V_{IH}	2.2	6.0	V	
Output Low Voltage	V_{OL}		0.4	V	I_{OL}=8mA
Output High Voltage	V_{OH}	2.4		V	I_{OH}=−4mA
Peak Power-on Current	I_{PO}		50	mA	V_{CC}=0V to V_{CC} Min. $\overline{CS_1}$=Lower of V_{CC} or V_{IH} Min.

* −2.0V Min. for pulse width less than 20ns. (V_{IL} Min=−0.5V at DC level)

1

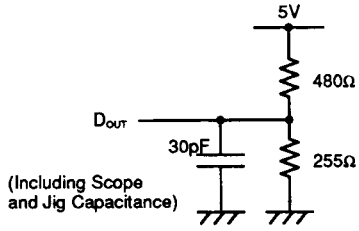
AC TEST CONDITIONS

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise And Fall Times:	5ns (Transient time between 0.8V and 2.2V)
Timing Measurement Reference Levels:	Input: 1.5V Output: 1.5V

Fig. 2

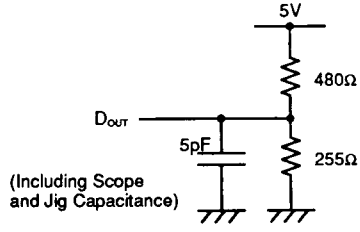
Output Load I.

For all except t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



Output Load II.

For t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

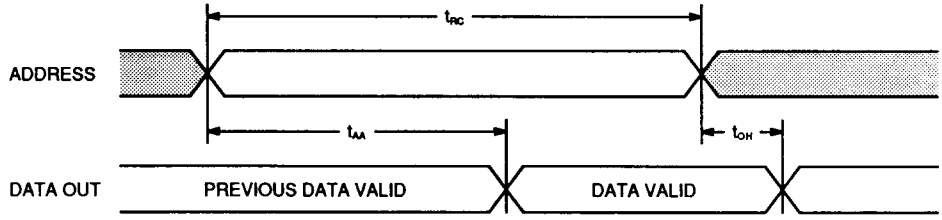
Parameter	Symbol	MB81C79A-35		MB81C79A-45		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		ns
Address Access Time*2	t_{AA}		35		45	ns
$\overline{CS_1}$ Access Time*3	t_{ACS1}		35		45	ns
CS_2 Access Time*3	t_{ACS2}		15		20	ns
Output Hold from Address Change	t_{OH}	3		3		ns
$\overline{OE}$ Access Time	t_{OE}		15		20	ns
Output Active from $\overline{CS_1}$*4	t_{LZ1}	5		5		ns
Output Active from CS_2*4	t_{LZ2}	3		3		ns
Output Active from $\overline{OE}$*4	t_{OLZ}	3		3		ns
Output Disable from $\overline{CS_1}$*4	t_{HZ1}		20		25	ns
Output Disable from CS_2*4	t_{HZ2}		20		25	ns
Output Disable from $\overline{OE}$*4	t_{OHZ}		20		25	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1}=V_{IL}$, $CS_2=V_{IH}$ and $\overline{OE}=V_{IL}$.
*3 Address valid prior to or coincident with CS_1 transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

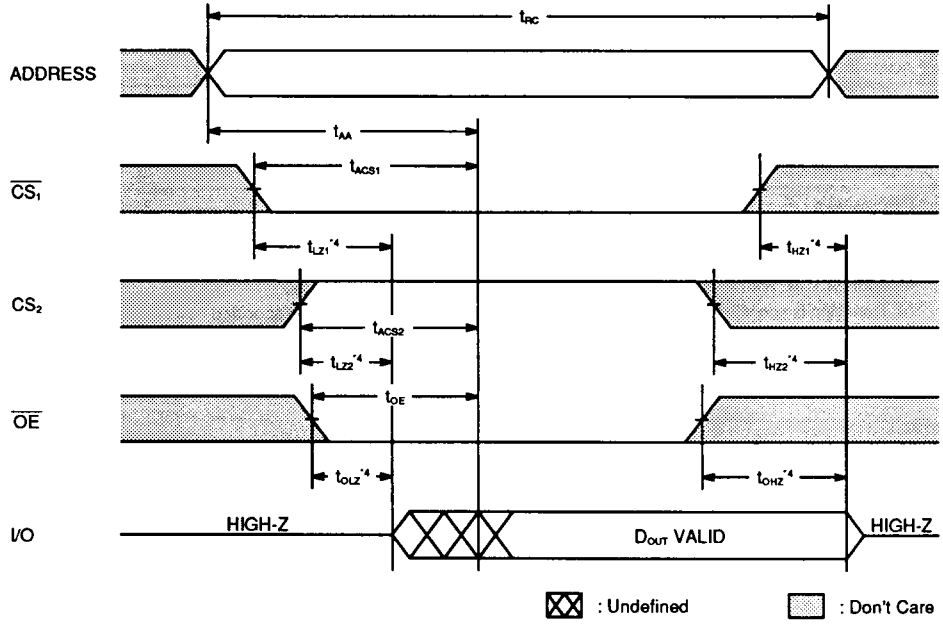
1

READ CYCLE TIMING DIAGRAM*1

READ CYCLE I: ADDRESS CONTROLLED*2



READ CYCLE II: $\overline{CS_1}$, CS_2 CONTROLLED*3



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE*1

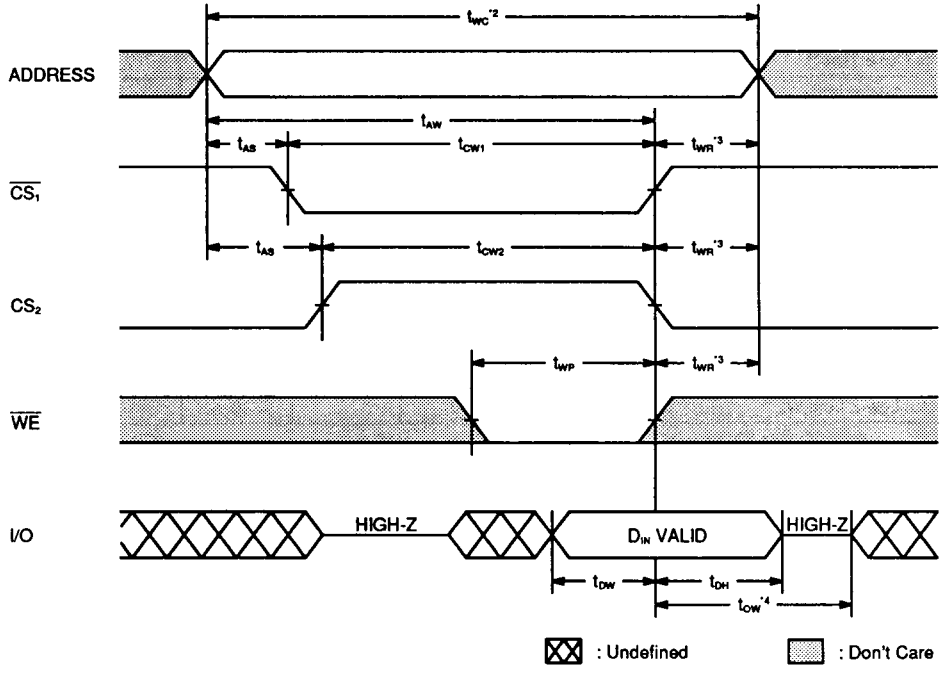
Parameter	Symbol	MB81C79A-35		MB81C79A-45		Unit
		Min	Max	Min	Max	
Write Cycle Time*2	t_{WC}	35		45		ns
$\overline{CS_1}$ to End of Write	t_{CW1}	30		40		ns
CS_2 to End of Write	t_{CW2}	20		25		ns
Address Valid to End of Write	t_{AW}	30		40		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	20		25		ns
Data Setup Time	t_{DW}	17		20		ns
Write Recovery Time*3	t_{WR}	3		3		ns
Data Hold Time	t_{DH}	0		0		ns
Output High-Z from $\overline{WE}$*4	t_{WZ}		15		20	ns
Output Low-Z from $\overline{WE}$*4	t_{OW}	0		0		ns

Note: *1 If $\overline{CS_1}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

1

WRITE CYCLE TIMING DIAGRAM*1

WRITE CYCLE I: $\overline{CS_1}$, CS_2 CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

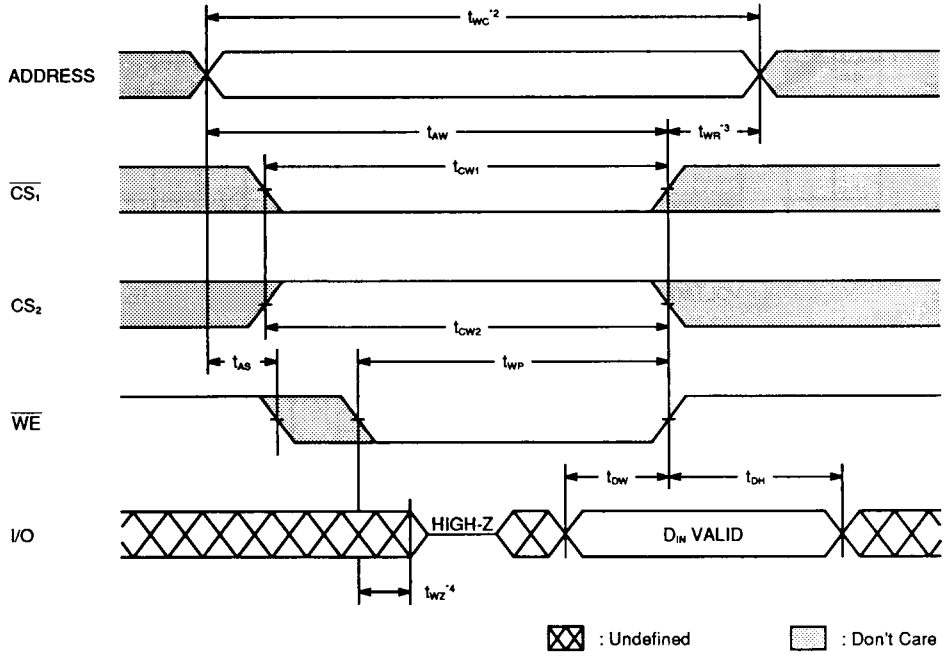
*2 All write cycle are determined from the last address transition to the first address transition of next address.

*3 t_{WR} is defined from the end point of WRITE Mode.

*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM*1

WRITE CYCLE II: $\overline{WE}$ CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 All write cycles are determined from the last address transition to the first address transition of next address.

*3 t_{WR} is defined from the end point of WRITE Mode.

*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

1

Fig. 3 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

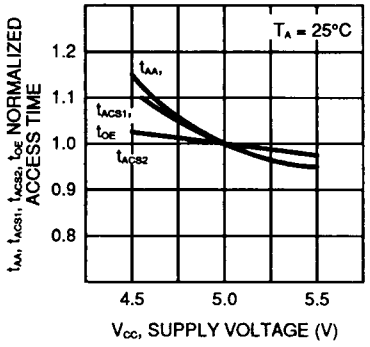


Fig. 4 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

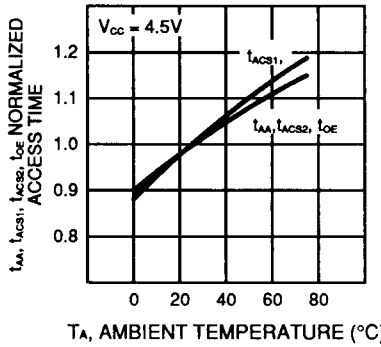


Fig. 5 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

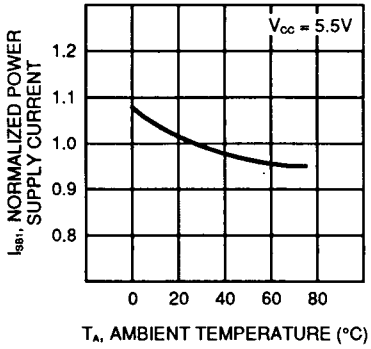


Fig. 6 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

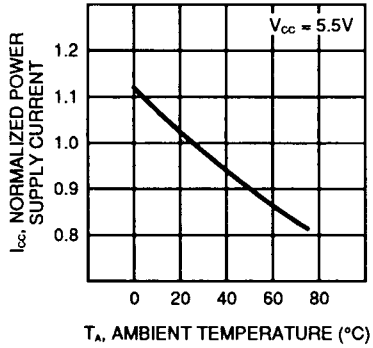


Fig. 7 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

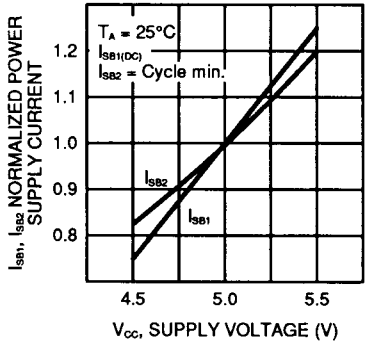


Fig. 8 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

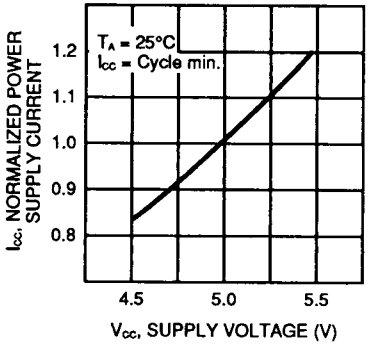


Fig. 9 – NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

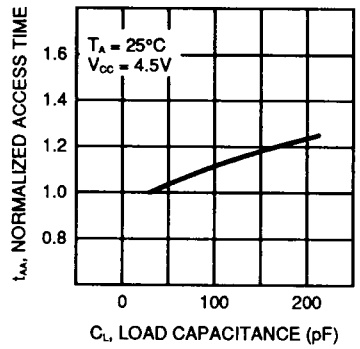


Fig. 10 – NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

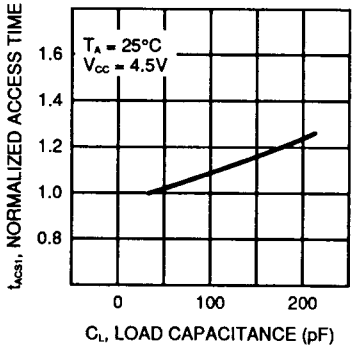


Fig. 11 – NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

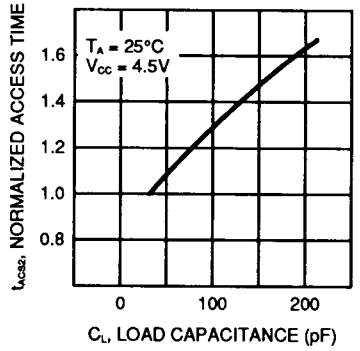
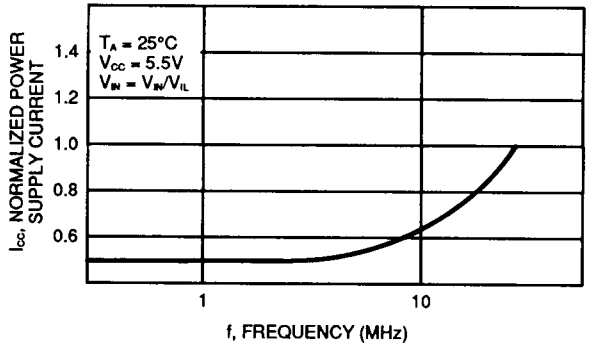


Fig. 12 – NORMALIZED POWER SUPPLY CURRENT vs. FREQUENCY

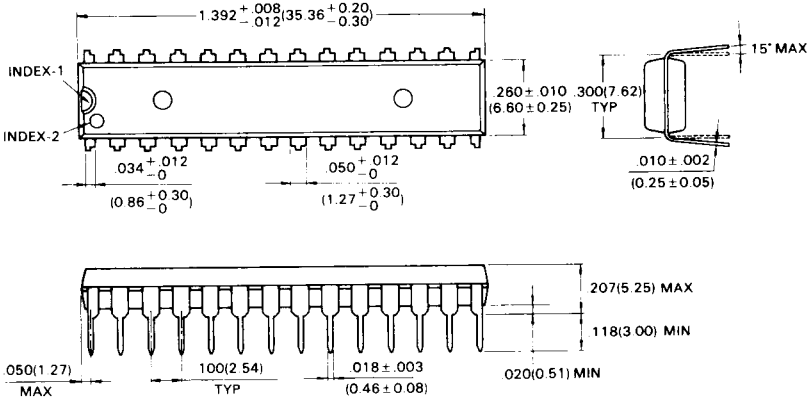


PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: P-SK)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-28P-M04)

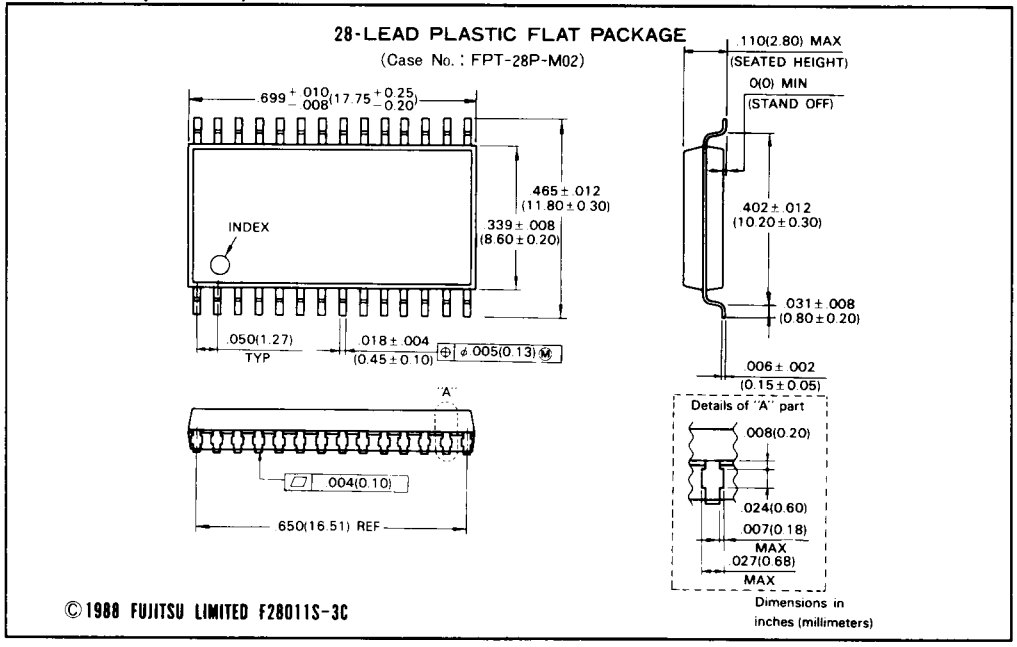


© 1988 FUJITSU LIMITED D28018S-2C

Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

PLASTIC FPT (Suffix: PF)



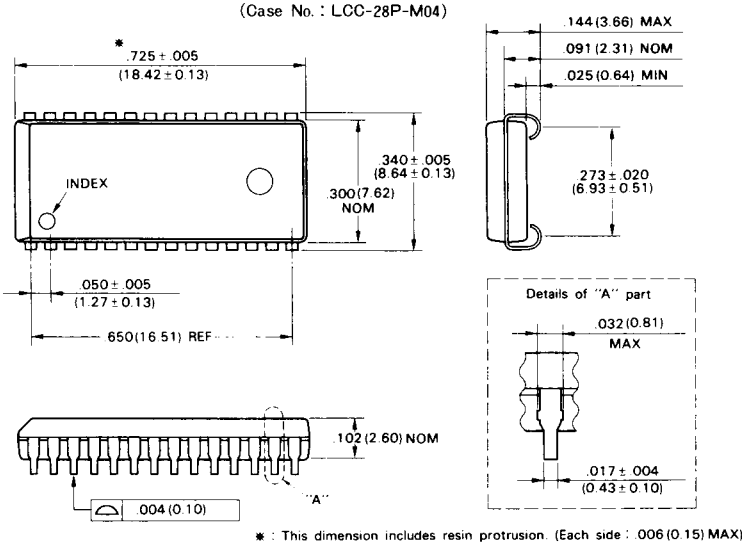
©1988 FUJITSU LIMITED F28011S-3C

PACKAGE DIMENSIONS (Cont'd)

PLASTIC (Suffix: PJ)

28-LEAD PLASTIC LEADED CHIP CARRIER

(Case No. : LCC-28P-M04)

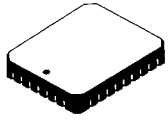


* : This dimension includes resin protrusion. (Each side : .006 (0.15) MAX)

©1989 FUJITSU LIMITED C28054S-1C

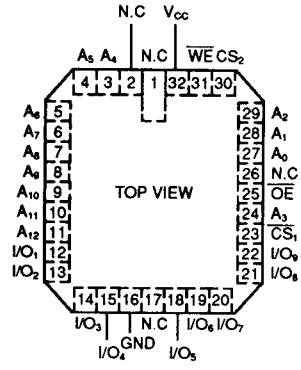
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Cont'd)



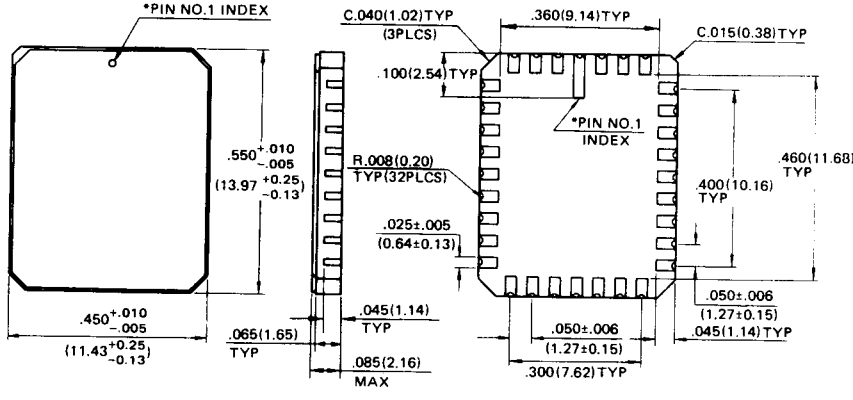
CERAMIC PACKAGE
LCC-32C-A02

PIN ASSIGNMENT



CERAMIC LCC (Suffix: CV)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches
(millimeters)

©1988 FUJITSU LIMITED C32011S-3C