

# MOSTEK®

INDUSTRIAL PRODUCTS

## Top-Octave Frequency Generator

### MK50240/1/2(P/N)

#### FEATURES

- Single power supply
- Broad supply voltage operating range
- Low power consumption
- High output drive capability
  - MK50240 - 50% output duty cycle
  - MK50241 - 30% output duty cycle
  - MK50242 - 50% output duty cycle
- RFI minimization\*
- One full octave on a chip

#### DESCRIPTION

Refer to Figure 2 for Block Diagram. The MK50240 is one of a family of ion-implanted, P-channel MOS, synchronous frequency dividers.

Low-threshold voltage enhancement-mode devices, as well as depletion-mode devices, are fabricated on the same chip, allowing the MK50240 family to operate from a single, wide-tolerance supply. Depletion-mode technology also allows the entire circuit to operate on less than 600 mW of power. The circuits are packaged in 16-pin dual-in-line packages.

RF interference and feed-through is minimized by placing the input clock between the  $V_{DD}$  and  $V_{SS}$  pins.\* Internally, the layout of the chip isolates the output buffer circuitry from the divisor circuit clock lines. Also, the output buffers limit the minimum rise-time under no load conditions to reduce the RF harmonic content of each output signal.

Each output frequency is related to the others by a multiple of  $\sqrt[2]{2}$ , providing a full octave plus one note\* on the equal-tempered scale.

#### FUNCTIONAL DESCRIPTION

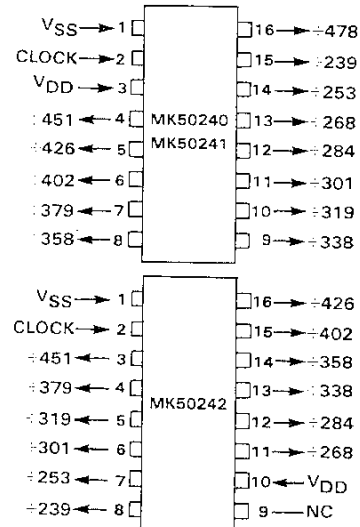
$V_{SS}$ , Pin 1

$V_{SS}$  is the positive supply voltage and should be maintained

\*MK50240 & MK50241 only

#### PIN CONNECTIONS

Figure 1



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between 11 V and 16 V with respect to  $V_{DD}$ .

#### CLOCK, Pin 2

The external clock signal is supplied to the chip through this pin. (Refer to ELECTRICAL CHARACTERISTICS and Figure 3).

$V_{DD}$ , Pin 3 (MK50240/1); Pin 10 (MK50242)

$V_{DD}$  is the negative supply voltage and is nominally ground.

NC, Pin 9 (MK50242 only)

There is no internal connection to the chip at this pin.

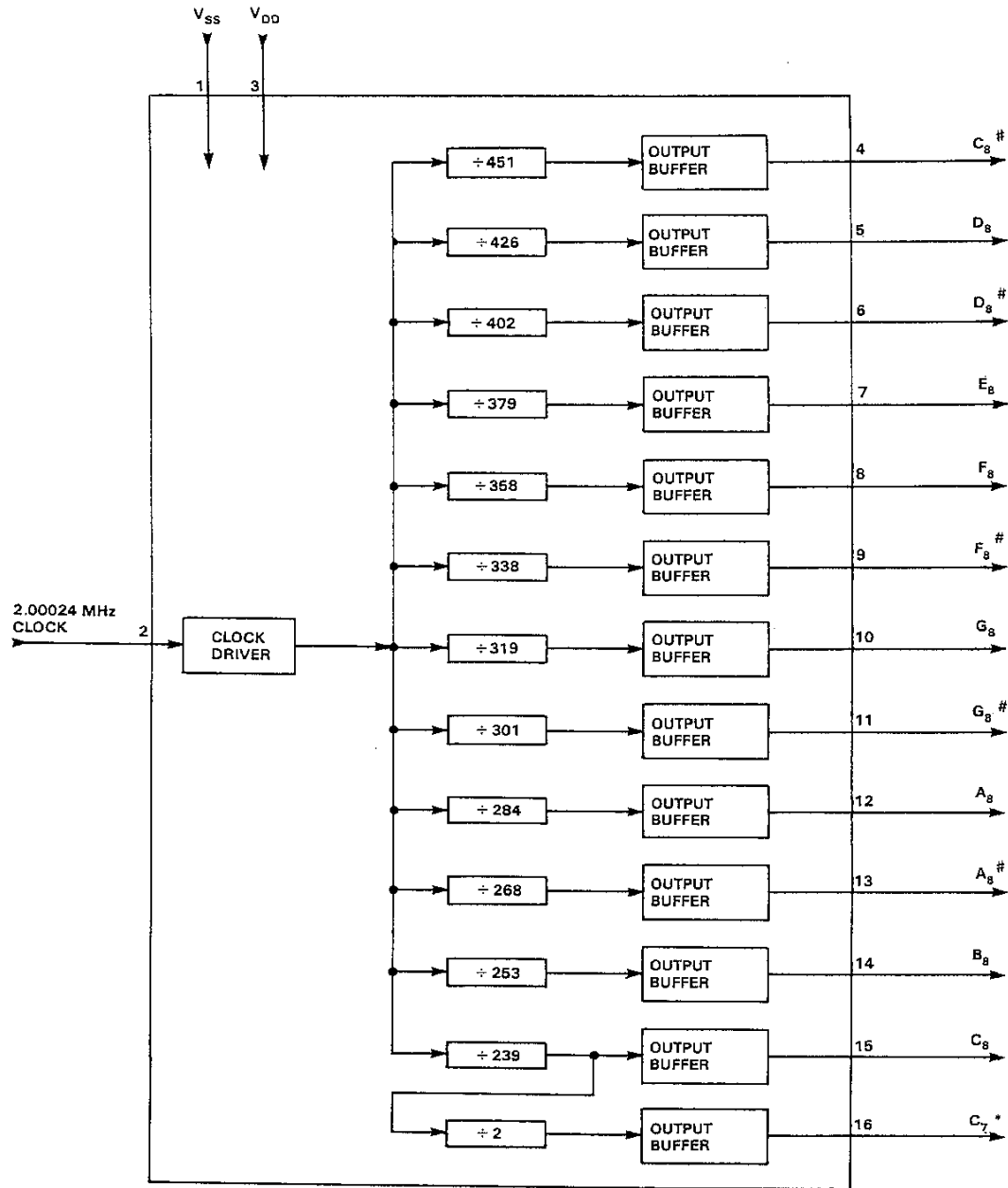
#### OUTPUTS

Figure 4 shows maximum permissible output loading.

#### TYPICAL APPLICATION

Figure 6 shows one octave of tone generation.

**BLOCK DIAGRAM \*\***  
Figure 2



\*This output available on MK50240/1 only.

\*\*Pin numbers shown are for MK50240/1 only.

**ABSOLUTE MA**

Voltage on any p  
Operating Tempe  
Storage Tempera

\*Stresses above those l  
device at these or any ot  
for extended periods me

**ELECTRICAL CI**

**DC CHARACTE**  
(VDD = 0 V, 11.0

SYM	PAI
VSS	Sup
IDD	Sup
VIL	Inpu
VIH	Inpu
Cj	Inpu
VOL	Out
VOH	Out

**AC CHARACTE**  
(VDD = 0 V, 11.0 V)

SYM	PAI
fI	Inpu
tR, tF	Inpu Rise 10%
tON, tOFF	Inpu On @ 2
tRO, tFO	Out 500
tON, tOFF	Out MK MK

NOTES: 1. Pin 16 has  
2. Outputs u

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on any pin relative to  $V_{SS}$  ..... +0.3 V to -20 V  
 Operating Temperature (Ambient) ..... 0°C to 50°C  
 Storage Temperature (Ambient) ..... -40°C to 100°C

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ELECTRICAL CHARACTERISTICS**

**DC CHARACTERISTICS**

( $V_{DD} = 0\text{ V}$ ,  $11.0\text{ V} \leq V_{SS} \leq 16.0\text{ V}$ ,  $0^\circ\text{C} \leq T_A \leq 50^\circ\text{C}$ , unless otherwise specified)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
$V_{SS}$	Supply Voltage	11.0	15.0	16.0	V	
$I_{DD}$	Supply Current		24	37	mA	Note 2
$V_{IL}$	Input Clock, Low	0		1.0	V	Figure 3
$V_{IH}$	Input Clock, High	$V_{SS}-1.0$		$V_{SS}$	V	Figure 3
$C_I$	Input Capacitance		5	10	pF	
$V_{OL}$	Output, Low @ .70 mA	0		1.5	V	Figure 4
$V_{OH}$	Output, High @ .75 mA	$V_{SS}-1.0$		$V_{SS}$	V	Figure 4

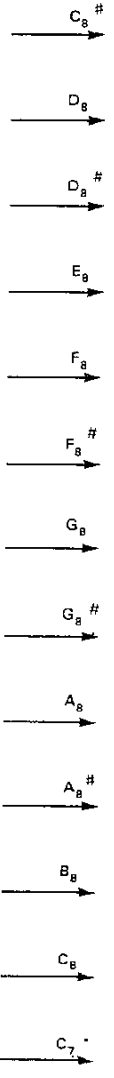
**AC CHARACTERISTICS**

( $V_{DD} = 0\text{ V}$ ,  $11.0\text{ V} \leq V_{SS} \leq 16.0\text{ V}$ ,  $0^\circ\text{C} \leq T_A \leq 50^\circ\text{C}$ , unless otherwise specified)

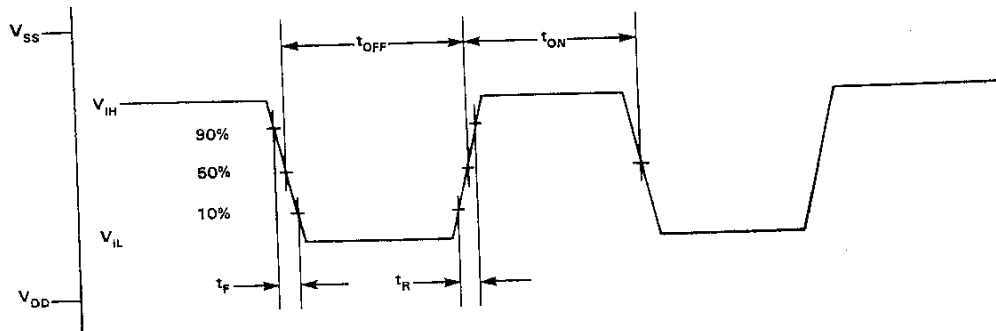
SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
$f_I$	Input Clock Frequency	100	2000.240	2500	kHz	
$t_R, t_F$	Input Clock Rise and Fall Times 10% to 90% @ 2.5 MHz			30	ns	Figure 3
$t_{ON}, t_{OFF}$	Input Clock On and Off Times @ 2.5 MHz		200		ns	Figure 3
$t_{RO}, t_{FO}$	Output Rise and Fall Times, 500 pF Load	250		2500	ns	Figure 5
$t_{ON}, t_{OFF}$	Output Duty Cycle MK50240 and MK50242 MK50241		50 30		% %	Note 1

NOTES: 1. Pin 16 has a 50% output duty cycle  
 2. Outputs unloaded.

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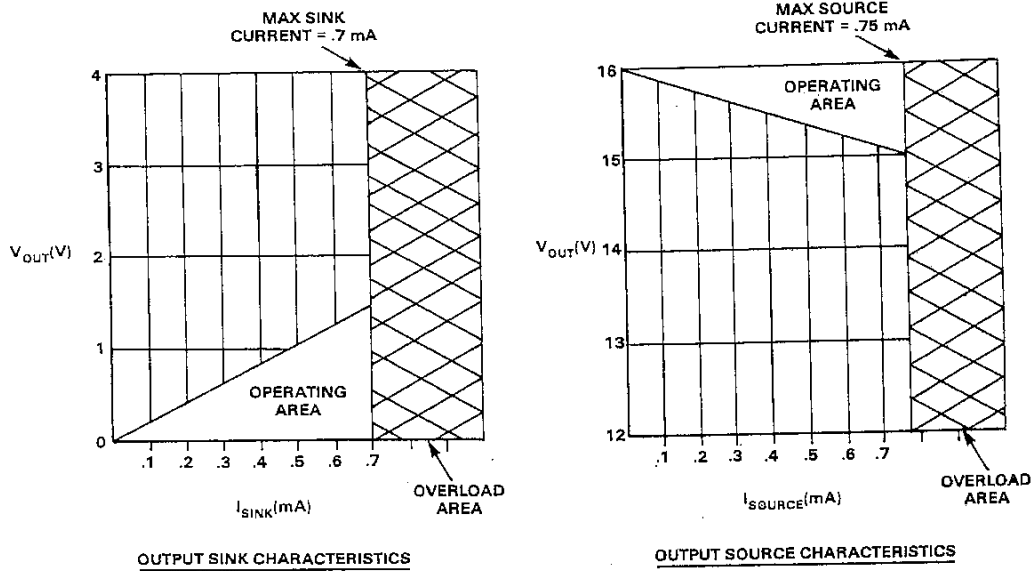
INPUT CLOCK WAVEFORM  
Figure 3



OUTPUT LOA  
Figure 5

CLOCK -

OUTPUT DRIVER CHARACTERISTICS  
Figure 4

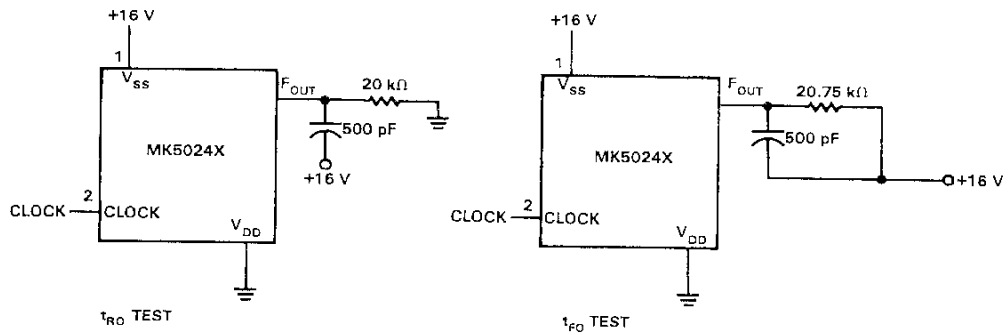


TYPICAL APF  
Figure 6

OTHER OCTAVES

OUTPUT LOADING

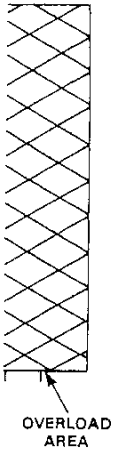
Figure 5



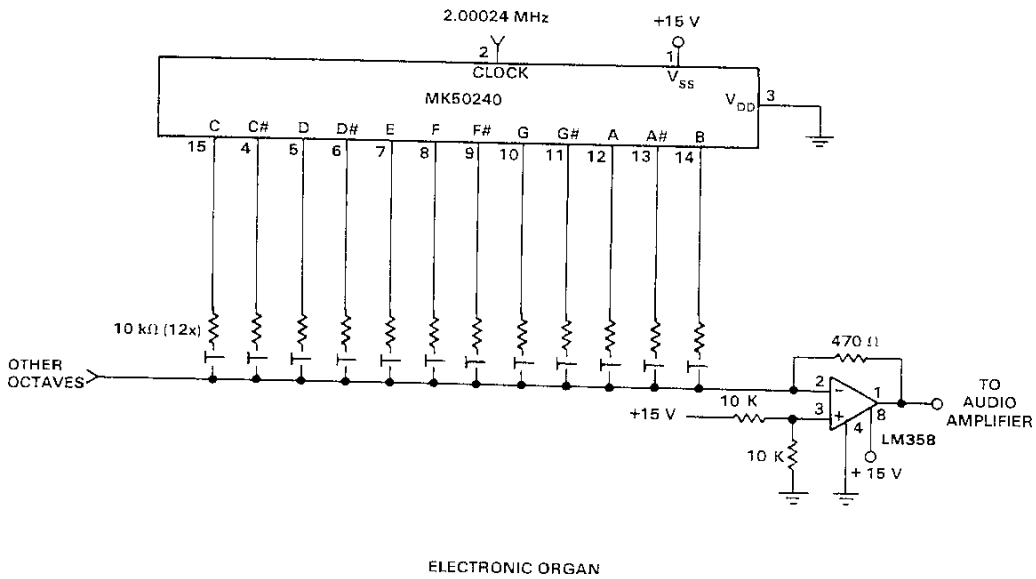
TYPICAL APPLICATION

Figure 6

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