



STB130NH02L

N-CHANNEL 24V - 0.0034 Ω - 120A D²PAK STripFET™ III POWER MOSFET FOR DC-DC CONVERSION

| TYPE | V _{DSS} | R _{DS(on)} | I _D |
|-------------|------------------|---------------------|---------------------|
| STB130NH02L | 24 V | < 0.0044 Ω | 90 A ⁽²⁾ |

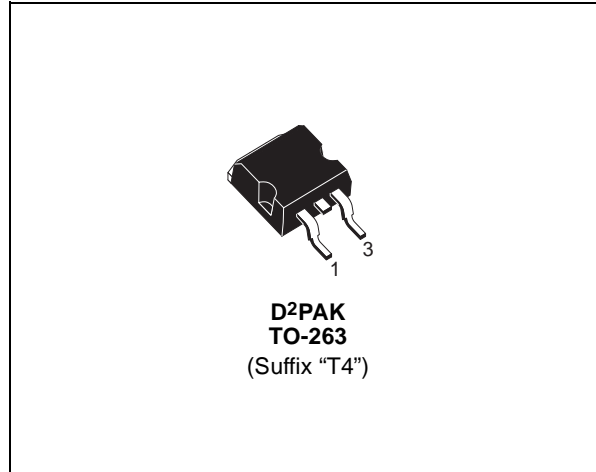
- TYPICAL R_{DS(on)} = 0.0034 Ω @ 10 V
- TYPICAL R_{DS(on)} = 0.005 Ω @ 5 V
- R_{DS(ON)} * Q_g INDUSTRY'S BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE
- SURFACE-MOUNTING D²PAK (TO-263)
POWER PACKAGE IN TUBE (NO SUFFIX) OR
IN TAPE & REEL (SUFFIX "T4")

DESCRIPTION

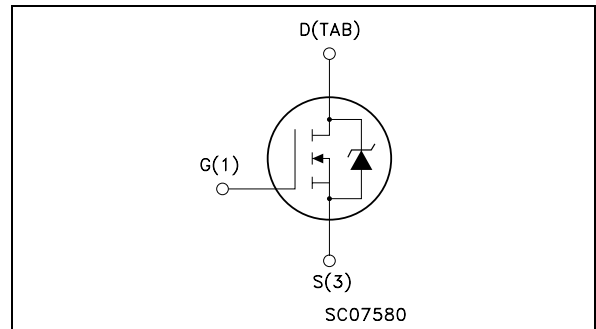
The STB130NH02L utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. It is ideal in high performance DC-DC converter applications where efficiency is to be achieved at very high output currents.

APPLICATIONS

- SYNCHRONOUS RECTIFICATIONS FOR TELECOM AND COMPUTER
- OR-ING DIODE



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|--------------------------------|--|------------|------|
| V _{spike(1)} | Drain-source Voltage Rating | 30 | V |
| V _{DS} | Drain-source Voltage (V _{GS} = 0) | 24 | V |
| V _{DGR} | Drain-gate Voltage (R _{GS} = 20 kΩ) | 24 | V |
| V _{GS} | Gate- source Voltage | ± 20 | V |
| I _D ⁽²⁾ | Drain Current (continuous) at T _C = 25°C | 90 | A |
| I _D ⁽²⁾ | Drain Current (continuous) at T _C = 100°C | 90 | A |
| I _{DM} ⁽³⁾ | Drain Current (pulsed) | 360 | A |
| P _{tot} | Total Dissipation at T _C = 25°C | 150 | W |
| | Derating Factor | 1 | W/°C |
| E _{AS} ⁽⁴⁾ | Single Pulse Avalanche Energy | 900 | mJ |
| T _{stg} | Storage Temperature | -55 to 175 | °C |
| T _j | Max. Operating Junction Temperature | | |

STB130NH02L**THERMAL DATA**

| | | | | |
|----------------|--|-----|------|------|
| Rthj-case | Thermal Resistance Junction-case | Max | 1.0 | °C/W |
| Rthj-amb | Thermal Resistance Junction-ambient | Max | 62.5 | °C/W |
| T _I | Maximum Lead Temperature For Soldering Purpose | | 300 | °C |

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C UNLESS OTHERWISE SPECIFIED)
OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|----------------------|---|---|------|------|---------|----------|
| V _{(BR)DSS} | Drain-source Breakdown Voltage | I _D = 25 mA, V _{GS} = 0 | 24 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current (V _{GS} = 0) | V _{DS} = 20 V V _{DS} = 20 V T _C = 125°C | | | 1 10 | μA μA |
| I _{GSS} | Gate-body Leakage Current (V _{DS} = 0) | V _{GS} = ± 20 V | | | ±100 | nA |

ON (5)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---------------------|-----------------------------------|---|------|-----------------|-----------------|--------|
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} = V _{GS} I _D = 250 μA | 1 | | | V |
| R _{DS(on)} | Static Drain-source On Resistance | V _{GS} = 10 V I _D = 45 A V _{GS} = 5 V I _D = 22.5 A | | 0.0034 0.005 | 0.0044 0.008 | Ω Ω |

DYNAMIC

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|------|---------------------|------|----------------|
| g _{fs} (5) | Forward Transconductance | V _{DS} = 10 V I _D = 45 A | | 55 | | S |
| C _{iss} C _{oss} C _{riss} | Input Capacitance Output Capacitance Reverse Transfer Capacitance | V _{DS} = 15V f = 1 MHz V _{GS} = 0 | | 4450 1126 141 | | pF pF pF |
| R _G | Gate Input Resistance | f = 1 MHz Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain | | 1.6 | | Ω |

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ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------|--|--|------|---------------|------|----------------|
| $t_{d(on)}$ t_r | Turn-on Delay Time Rise Time | $V_{DD} = 10\text{ V}$ $I_D = 45\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3) | | 14 224 | | ns ns |
| Q_g Q_{gs} Q_{gd} | Total Gate Charge Gate-Source Charge Gate-Drain Charge | $V_{DD}=10\text{ V}$ $I_D=90\text{ A}$ $V_{GS}=10\text{ V}$ | | 69 13 9 | 93 | nC nC nC |
| $Q_{oss}^{(6)}$ | Output Charge | $V_{DS} = 16\text{ V}$ $V_{GS} = 0\text{ V}$ | | 27 | | nC |
| $Q_{gls}^{(7)}$ | Third-quadrant Gate Charge | $V_{DS} < 0\text{ V}$ $V_{GS} = 10\text{ V}$ | | 64 | | nC |

SWITCHING OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-----------------------|----------------------------------|--|------|----------|------|----------|
| $t_{d(off)}$ t_f | Turn-off Delay Time Fall Time | $V_{DD} = 10\text{ V}$ $I_D = 45\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3) | | 69 40 | 54 | ns ns |

SOURCE DRAIN DIODE

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-----------------------------------|--|---|------|-----------------|-----------|---------------|
| I_{SD} $I_{SDM}^{(3)}$ | Source-drain Current Source-drain Current (pulsed) | | | | 90 360 | A A |
| $V_{SD}^{(5)}$ | Forward On Voltage | $I_{SD} = 45\text{ A}$ $V_{GS} = 0$ | | | 1.3 | V |
| t_{rr} Q_{rr} I_{RRM} | Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current | $I_{SD} = 90\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5) | | 47 58 2.5 | | ns nC A |

(1) Guaranteed when external $R_g=4.7\ \Omega$ and $t_f < t_{fmax}$.

(2) Value limited by wire bonding

(3) Pulse width limited by safe operating area.

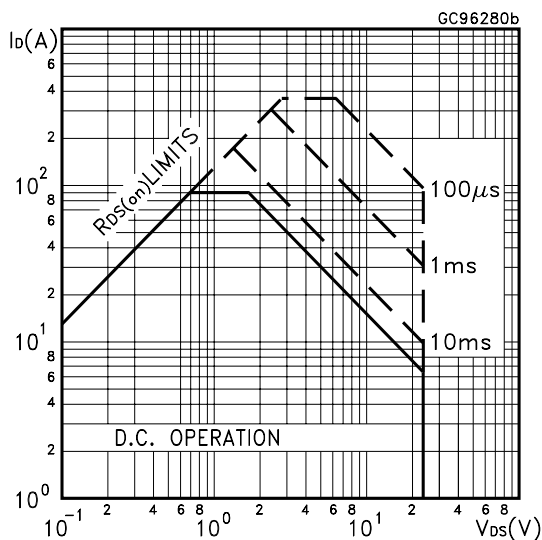
(4) Starting $T_j = 25^\circ\text{C}$, $I_D = 45\text{ A}$, $V_{DD} = 10\text{ V}$.

(5) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

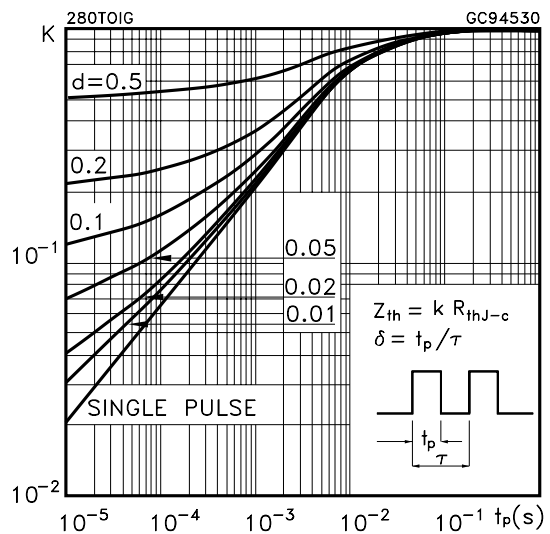
(6) $Q_{oss} = C_{oss} \cdot \Delta V_{in}$, $C_{oss} = C_{gd} + C_{ds}$. See Appendix A

(7) Gate charge for synchronous operation

Safe Operating Area

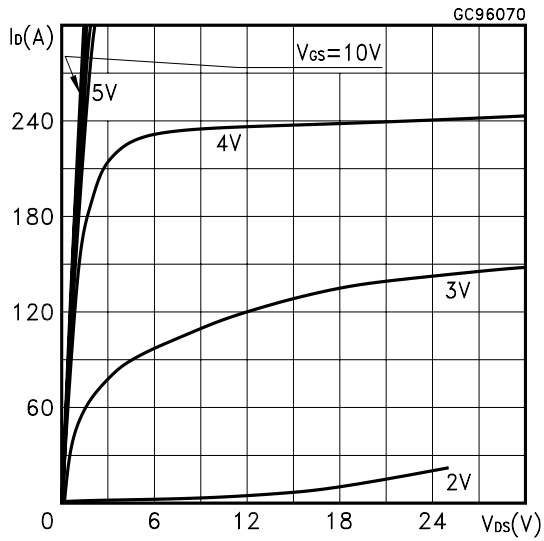


Thermal Impedance

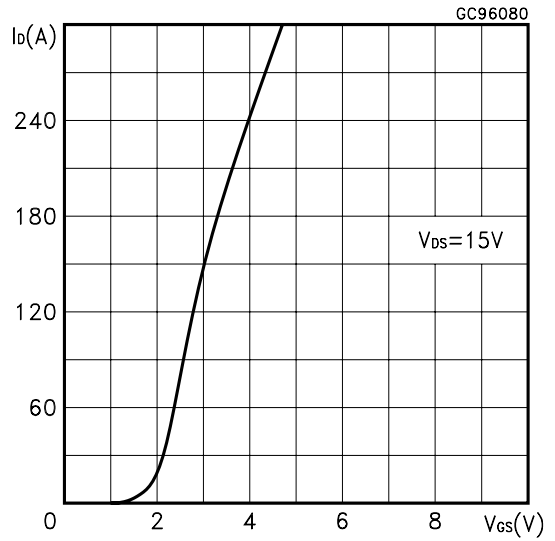


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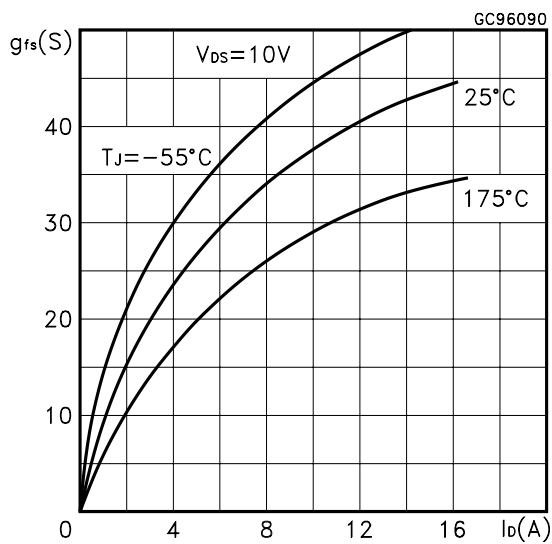
Output Characteristics



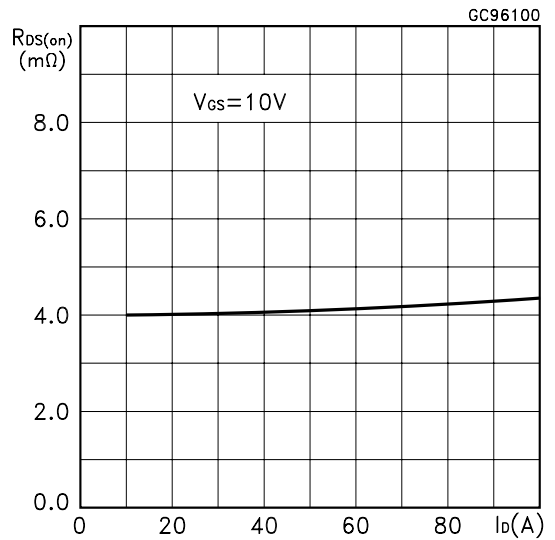
Transfer Characteristics



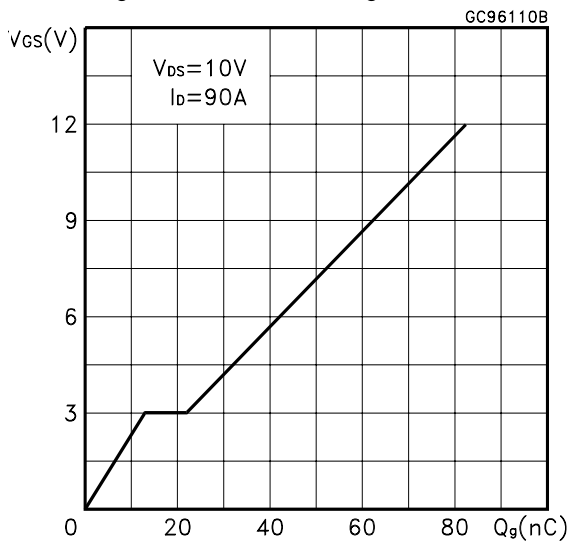
Transconductance



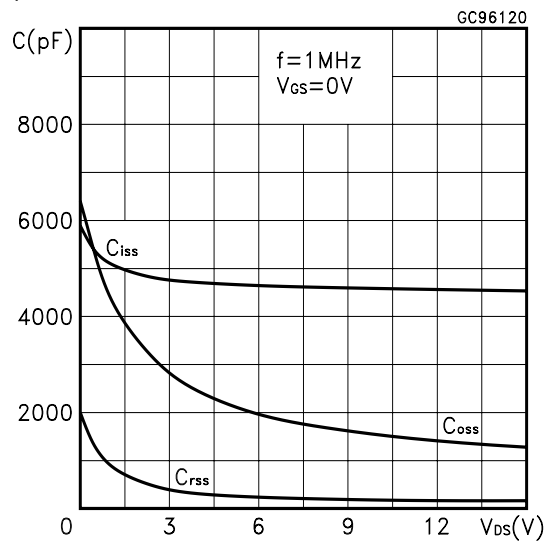
Static Drain-source On Resistance



Gate Charge vs Gate-source Voltage

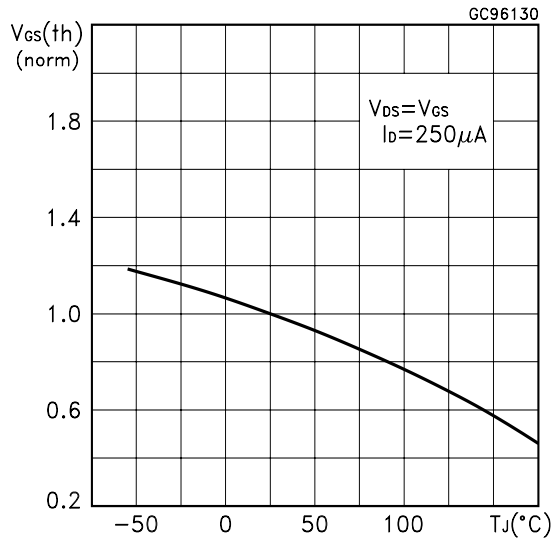


Capacitance Variations

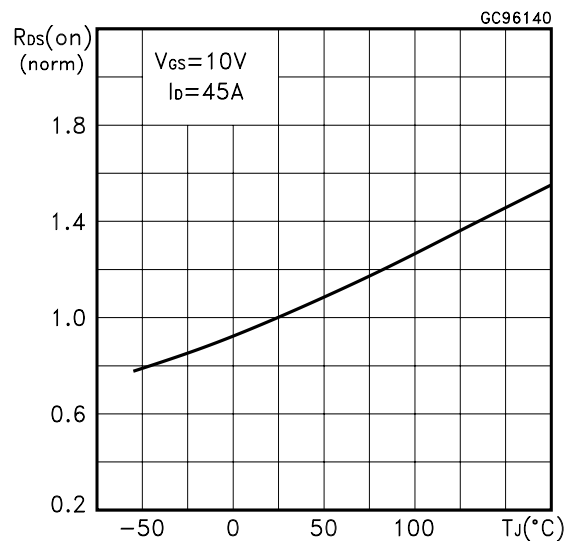


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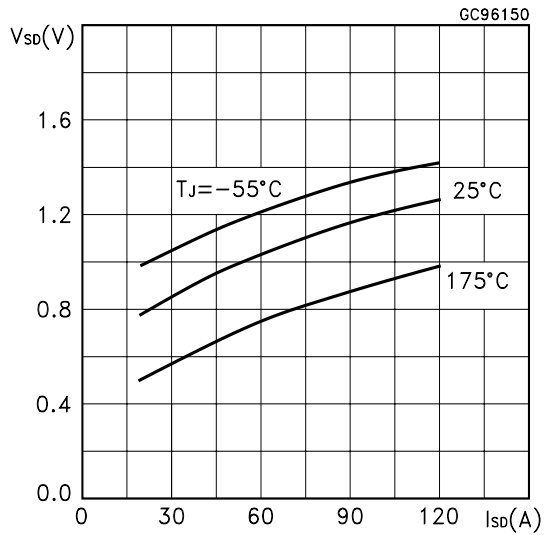
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage vs Temperature

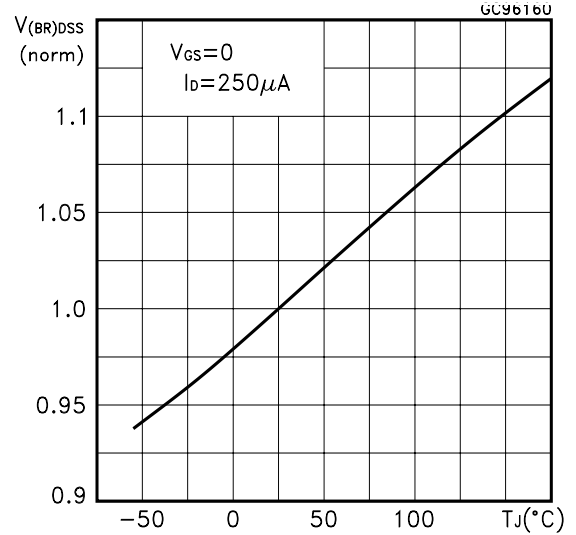


Fig. 1: Unclamped Inductive Load Test Circuit

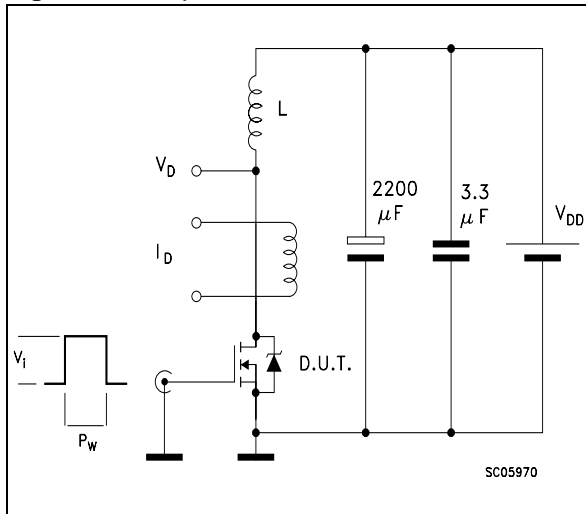


Fig. 2: Unclamped Inductive Waveform

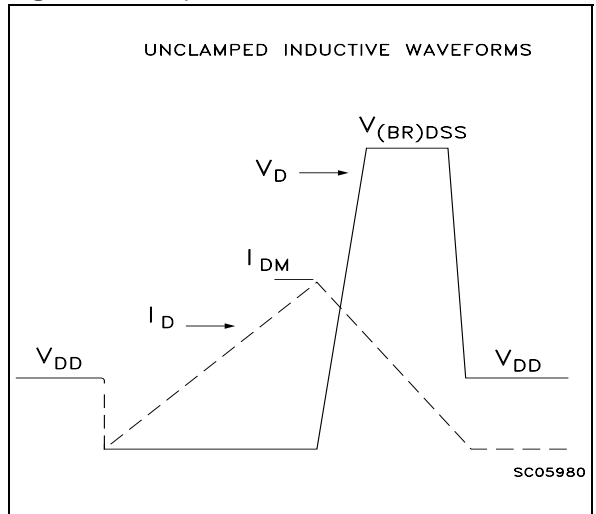


Fig. 3: Switching Times Test Circuits For Resistive Load

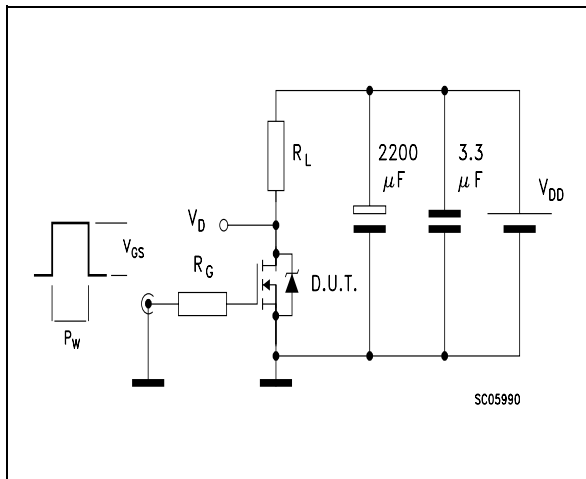


Fig. 4: Gate Charge test Circuit

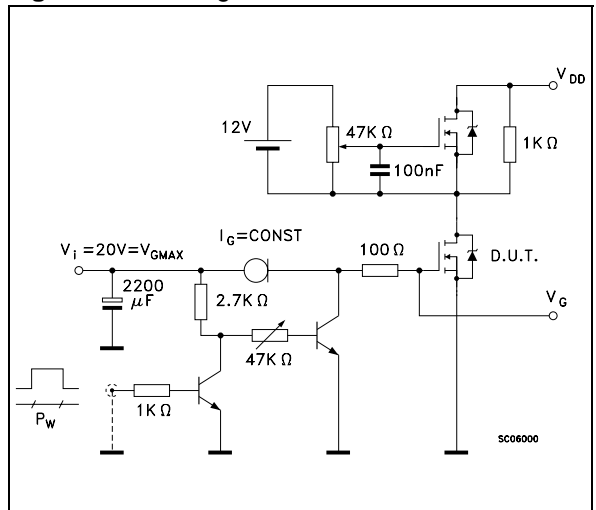
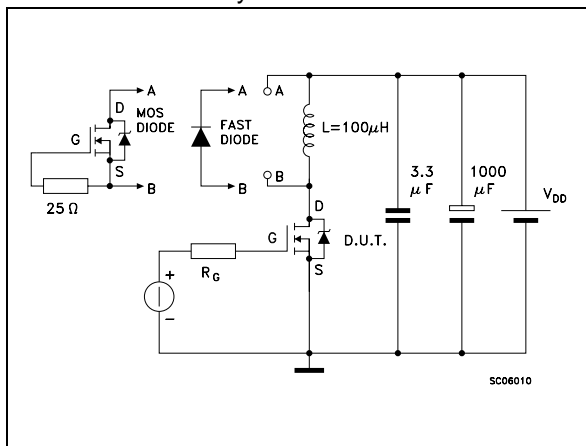
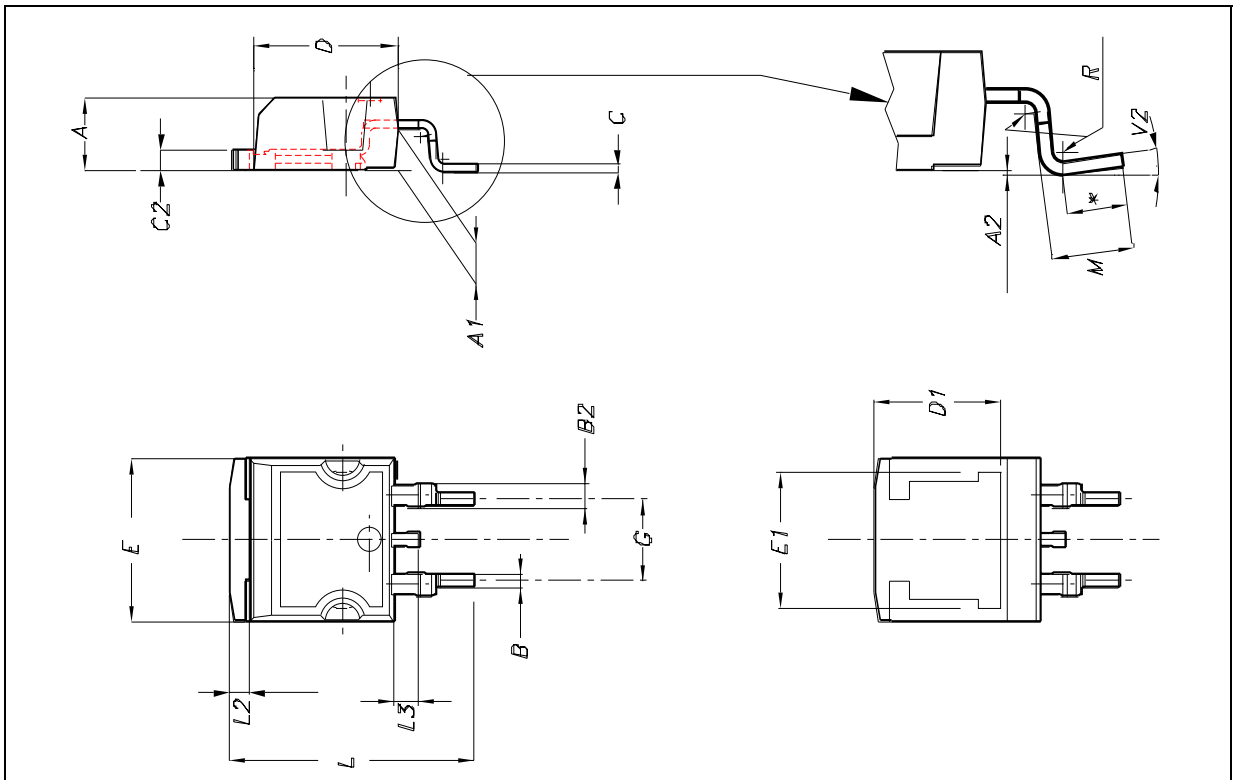


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

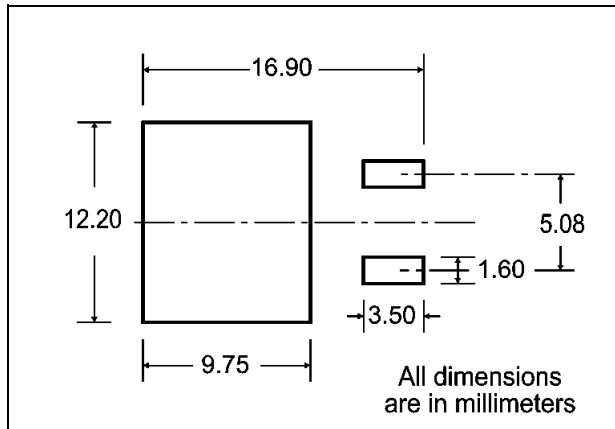


D²PAK MECHANICAL DATA

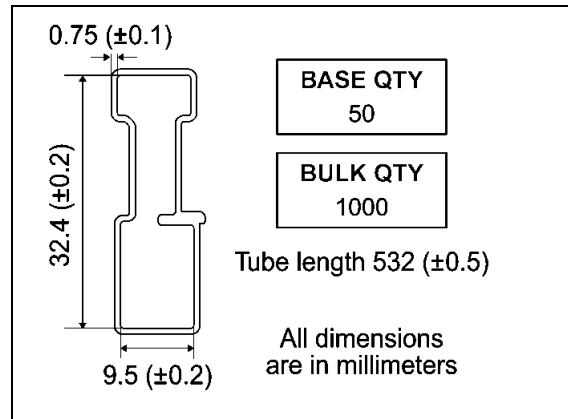
| DIM. | mm. | | | inch. | | |
|------|------|------|-------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | TYP. |
| A | 4.4 | | 4.6 | 0.173 | | 0.181 |
| A1 | 2.49 | | 2.69 | 0.098 | | 0.106 |
| A2 | 0.03 | | 0.23 | 0.001 | | 0.009 |
| B | 0.7 | | 0.93 | 0.028 | | 0.037 |
| B2 | 1.14 | | 1.7 | 0.045 | | 0.067 |
| C | 0.45 | | 0.6 | 0.018 | | 0.024 |
| C2 | 1.21 | | 1.36 | 0.048 | | 0.054 |
| D | 8.95 | | 9.35 | 0.352 | | 0.368 |
| D1 | | 8 | | | 0.315 | |
| E | 10 | | 10.4 | 0.394 | | 0.409 |
| E1 | | 8.5 | | | 0.334 | |
| G | 4.88 | | 5.28 | 0.192 | | 0.208 |
| L | 15 | | 15.85 | 0.591 | | 0.624 |
| L2 | 1.27 | | 1.4 | 0.050 | | 0.055 |
| L3 | 1.4 | | 1.75 | 0.055 | | 0.069 |
| M | 2.4 | | 3.2 | 0.094 | | 0.126 |
| R | | 0.4 | | | 0.015 | |
| V2 | 0° | | 8° | 0° | | 8° |



D2PAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

G measured at hub

REEL MECHANICAL DATA

| DIM. | mm | | inch | |
|------|------|------|-------|--------|
| | MIN. | MAX. | MIN. | MAX. |
| A | | 330 | | 12.992 |
| B | 1.5 | | 0.059 | |
| C | 12.8 | 13.2 | 0.504 | 0.520 |
| D | 20.2 | | 0.795 | |
| G | 24.4 | 26.4 | 0.960 | 1.039 |
| N | 100 | | 3.937 | |
| T | | 30.4 | | 1.197 |

| BASE QTY | BULK QTY |
|----------|----------|
| 1000 | 1000 |

TAPE MECHANICAL DATA

| DIM. | mm | | inch | |
|------|------|------|--------|--------|
| | MIN. | MAX. | MIN. | MAX. |
| A0 | 10.5 | 10.7 | 0.413 | 0.421 |
| B0 | 15.7 | 15.9 | 0.618 | 0.626 |
| D | 1.5 | 1.6 | 0.059 | 0.063 |
| D1 | 1.59 | 1.61 | 0.062 | 0.063 |
| E | 1.65 | 1.85 | 0.065 | 0.073 |
| F | 11.4 | 11.6 | 0.449 | 0.456 |
| K0 | 4.8 | 5.0 | 0.189 | 0.197 |
| P0 | 3.9 | 4.1 | 0.153 | 0.161 |
| P1 | 11.9 | 12.1 | 0.468 | 0.476 |
| P2 | 1.9 | 2.1 | 0.075 | 0.082 |
| R | 50 | | 1.574 | |
| T | 0.25 | 0.35 | 0.0098 | 0.0137 |
| W | 23.7 | 24.3 | 0.933 | 0.956 |

10 pitches cumulative tolerance on tape +/- 0.2 mm

Center line of cavity

User Direction of Feed

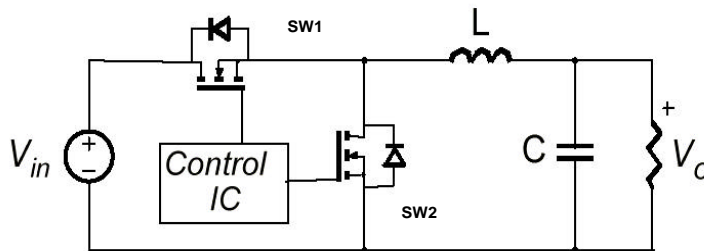
FEED DIRECTION

Bending radius R min.

* on sales type

APPENDIX A

Buck Converter: Power Losses Estimation



The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

The low side (SW2) device requires:

- Very low $R_{DS(on)}$ to reduce conduction losses
- Small Q_{gls} to reduce the gate charge losses
- Small C_{oss} to reduce losses due to output capacitance
- Small Q_{rr} to reduce losses on SW₁ during its turn-on
- The C_{gd}/C_{gs} ratio lower than V_{th}/V_{gg} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;

The high side (SW1) device requires:

- Small R_g and L_s to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Q_g to have a faster commutation and to reduce gate charge losses
- Low $R_{DS(on)}$ to reduce the conduction losses.

| | | High Side Switch (SW1) | Low Side Switch (SW2) |
|----------------------------------|------------|--|--|
| P _{conduction} | | $R_{DS(on)SW1} * I_L^2 * d$ | $R_{DS(on)SW2} * I_L^2 * (1-d)$ |
| P _{switching} | | $V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$ | Zero Voltage Switching |
| P _{diode} | Recovery | Not Applicable | ¹ V _{in} * Q _{rr(SW2)} * f |
| | Conduction | Not Applicable | V _{f(SW2)} * I _L * t _{deadtime} * f |
| P _{gate(Q_G)} | | $Q_{g(SW1)} * V_{gg} * f$ | $Q_{gls(SW2)} * V_{gg} * f$ |
| P _{Qoss} | | $\frac{V_{in} * Q_{oss(SW1)} * f}{2}$ | $\frac{V_{in} * Q_{oss(SW2)} * f}{2}$ |

| Parameter | Meaning |
|-------------------------|--|
| d | Duty-cycle |
| Q _{gsth} | Post threshold gate charge |
| Q _{gls} | Third quadrant gate charge |
| P _{conduction} | On state losses |
| P _{switching} | On-off transition losses |
| P _{diode} | Conduction and reverse recovery diode losses |
| P _{gate} | Gate drive losses |
| P _{Qoss} | Output capacitance losses |

¹ Dissipated by SW1 during turn-on

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