

2700 × 3pixel CCD Linear Sensor (Color)

Description

The ILX724K is a reduction type CCD linear sensor developed for color image scanner, and has shutter function per each color. This sensor reads A4-size documents at a density of 300 DPI.

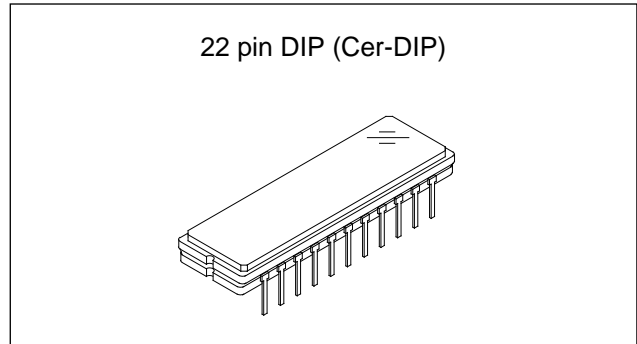
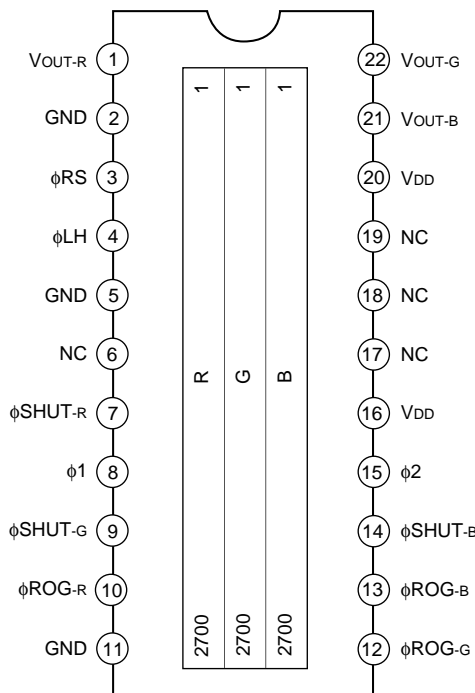
Features

- Number of effective pixels: 8100 pixels (2700 pixels × 3)
- Pixel size: 8μm × 8μm (8μm pitch)
- Distance between line: 64μm (8 Lines)
- Single-sided readout
- Shutter function
- Ultra low lag / High sensitivity
- Single 12V power supply
- Input clock pulse: CMOS 5V drive
- Number of output: 3 (R, G, B)
- Package: 22 pin cer-DIP (400 mil)

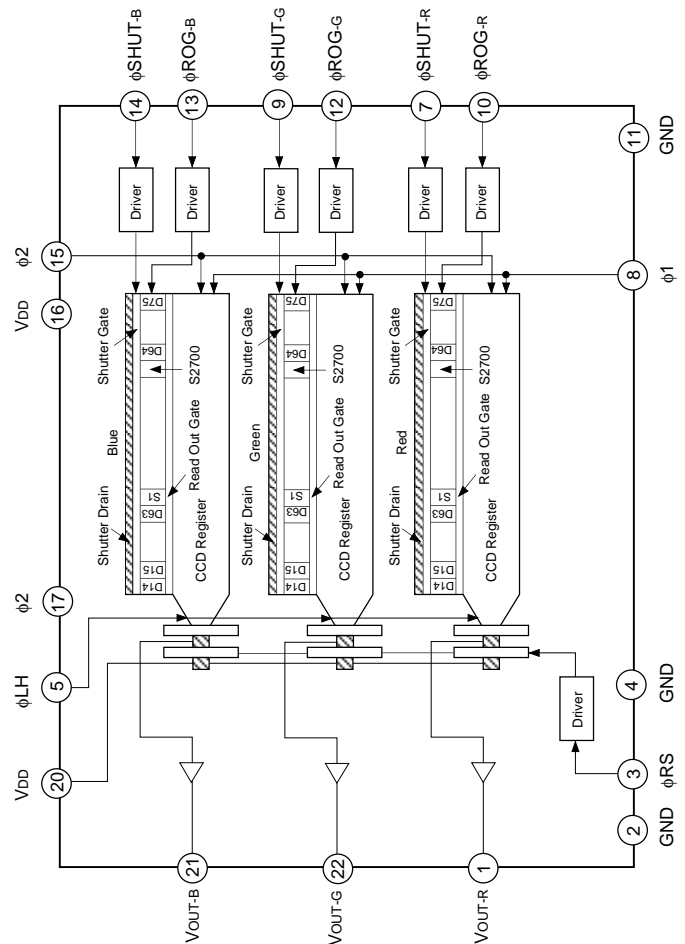
Absolute Maximum Ratings

- Supply voltage V_{DD} 15 V
- Operating temperature -10 to +55 °C
- Storage temperature -30 to +80 °C

Pin Configuration (Top View)



Block Diagram



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Pin Description

| Pin No. | Symbol | Description | Pin No. | Symbol | Description |
|---------|--------------------|-------------------|---------|--------------------|--------------------|
| 1 | V _{OUT-R} | Signal out (red) | 12 | ϕ ROG-G | Clock pulse input |
| 2 | GND | GND | 13 | ϕ ROG-B | Clock pulse input |
| 3 | ϕ RS | Clock pulse input | 14 | ϕ SHUT-B | Clock pulse input |
| 4 | ϕ LH | Clock pulse input | 15 | ϕ 2 | Clock pulse input |
| 5 | GND | GND | 16 | V _{DD} | 12V power supply |
| 6 | NC | NC | 17 | NC | NC |
| 7 | ϕ SHUT-R | Clock pulse input | 18 | NC | NC |
| 8 | ϕ 1 | Clock pulse input | 19 | NC | NC |
| 9 | ϕ SHUT-G | Clock pulse input | 20 | V _{DD} | 12V power supply |
| 10 | ϕ ROG-R | Clock pulse input | 21 | V _{OUT-B} | Signal out (blue) |
| 11 | GND | GND | 22 | V _{OUT-G} | Signal out (green) |

Recommended Supply Voltage

| Item | Min. | Typ. | Max. | Unit |
|-----------------|------|------|------|------|
| V _{DD} | 11.4 | 12 | 12.6 | V |

Clock Characteristics

| Item | Symbol | Min. | Typ. | Max. | Unit |
|--------------------------------------|------------------------|------|------|------|------|
| Input capacity of ϕ 1, ϕ 2 | C ϕ 1, C ϕ 2 | — | 400 | — | pF |
| Input capacity of ϕ LH | C ϕ LH | — | 10 | — | pF |
| Input capacity of ϕ RS | C ϕ RS | — | 10 | — | pF |
| Input capacity of ϕ ROG*1 | C ϕ ROG | — | 10 | — | pF |
| Input capacity of ϕ SHUT*1 | C ϕ SHUT | — | 10 | — | pF |

*1 It indicates that ϕ ROG-R, ϕ ROG-G, ϕ ROG-B as ϕ ROG, ϕ SHUT-R, ϕ SHUT-G, ϕ SHUT-B as ϕ SHUT.

Clock Frequency

| Item | Symbol | Min. | Typ. | Max. | Unit |
|--|--|------|------|------|------|
| ϕ 1, ϕ 2, ϕ LH, ϕ RS | f ϕ 1, f ϕ 2, f ϕ LH, f ϕ RS | — | 1 | 5 | MHz |

Input Clock Pulse Voltage Condition

| Item | Min. | Typ. | Max. | Unit | |
|---|------------|------|------|------|---|
| ϕ 1, ϕ 2, ϕ LH, ϕ RS, ϕ ROG, ϕ SHUT pulse voltage | High level | 4.75 | 5.0 | 5.25 | V |
| | Low level | — | 0 | 0.1 | V |

Electrooptical Characteristics (Note 1)

Ta = 25°C, VDD = 12V, f_{DRS} = 1MHz, Input clock = 5Vp-p, Light source = 3200K, IR cut filter CM-500S (t = 1.0mm)

| Item | | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---------------------------|-------|------------------|------|-------|------|------------|---------|
| Sensitivity | Red | R _R | 1.3 | 2.0 | 2.7 | V/(lx · s) | Note 2 |
| | Green | R _G | 2.1 | 3.2 | 4.3 | | |
| | Blue | R _B | 1.6 | 2.5 | 3.4 | | |
| Sensitivity nonuniformity | | PRNU | — | 4 | 20 | % | Note 3 |
| Saturation output voltage | | V _{SAT} | 2 | 3.2 | — | V | Note 4 |
| Saturation exposure | Red | SE _R | 0.74 | 1.6 | — | lx · s | Note 5 |
| | Green | SE _G | 0.46 | 1 | — | | |
| | Blue | SE _B | 0.58 | 1.28 | — | | |
| Dark voltage average | | V _{DRK} | — | 0.3 | 2 | mV | Note 6 |
| Dark signal nonuniformity | | DSNU | — | 1.5 | 5 | mV | Note 6 |
| Image lag | | IL | — | 0.02 | — | % | Note 7 |
| Supply current | | I _{VDD} | — | 26 | 50 | mA | — |
| Total transfer efficiency | | TTE | 92 | 98 | — | % | — |
| Output impedance | | Z _O | — | 250 | — | Ω | — |
| Offset level | | V _{OS} | — | 6.5 | — | V | Note 8 |
| Dynamic range | | DR | 1000 | 10670 | — | — | Note 9 |

Note

- 1) In accordance with the given electrooptical characteristics, the black level is defined as the average value of D2, D3 to D12.
- 2) For the sensitivity test light is applied with a uniform intensity of illumination.
- 3) PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 2.

$$V_{OUT-G} = 500\text{mV (Typ.)}$$

$$PRNU = \frac{(V_{MAX} - V_{MIN}) / 2}{V_{AVE}} \times 100 [\%]$$

Where the 2700 pixels are divided into blocks of 100. The maximum output of each block is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.

- 4) Use below the minimum value of the saturation output voltage.
- 5) Saturation exposure is defined as follows.

$$SE = \frac{V_{SAT}}{R}$$

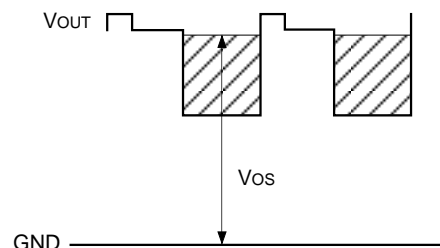
Where R indicates R_R, R_G, R_B, and SE indicates SE_R, SE_G, SE_B.

- 6) Optical signal accumulated time τ int stands at 10ms.
- 7) V_{OUT-G} = 500mV (Typ.)
- 8) V_{OS} is defined as indicated bellow.

V_{OUT} indicates V_{OUT-R}, V_{OUT-G}, and V_{OUT-B}.

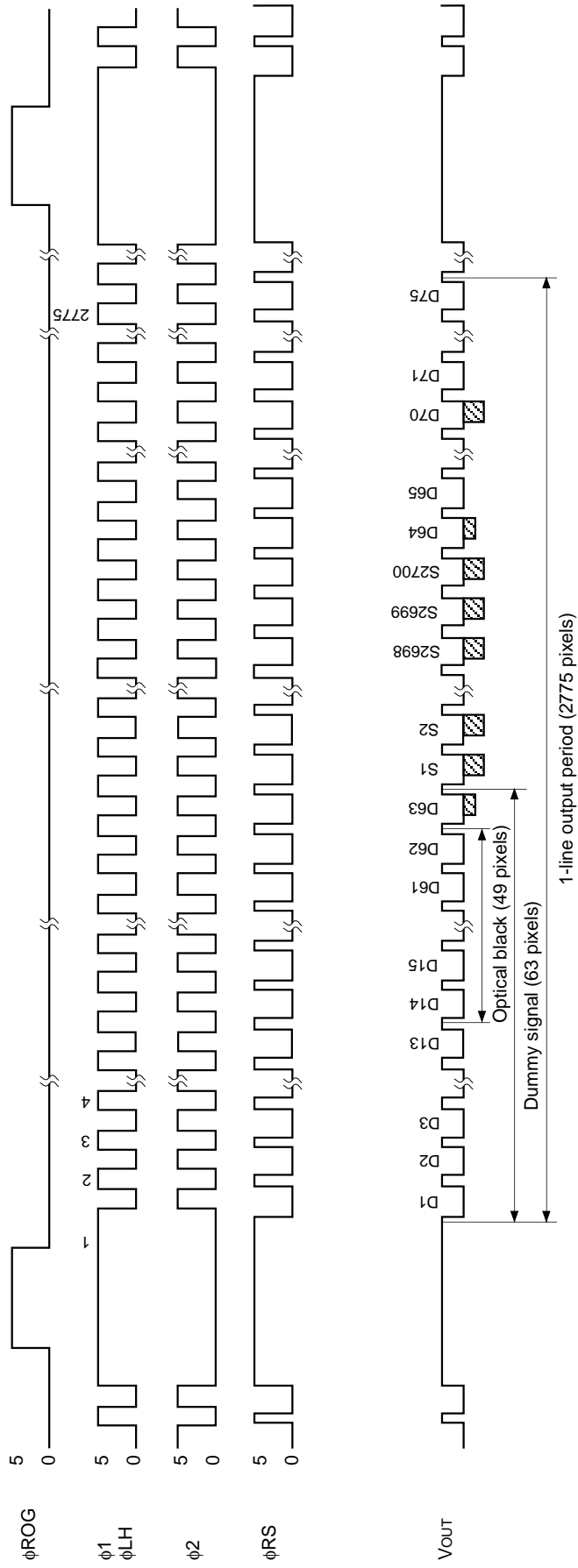
- 9) Dynamic range is defined as follows.

$$DR = \frac{V_{SAT}}{V_{DRK}}$$



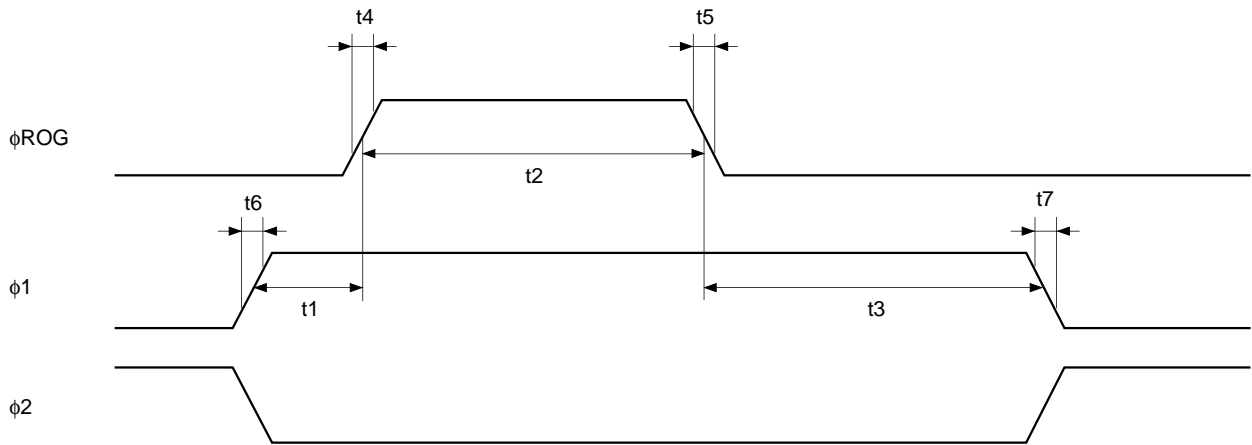
When the optical signal accumulated time is shorter, the dynamic range gets wider because the optical signal accumulated time is in proportion to the dark voltage.

Clock Timing Chart 1

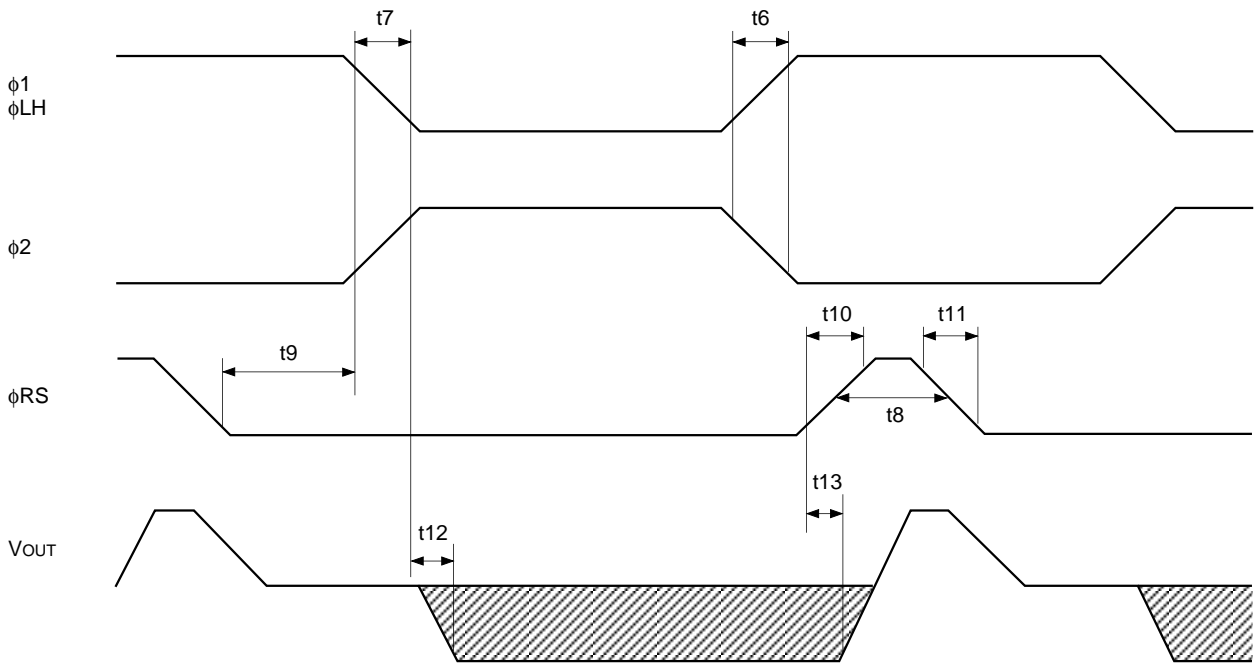


Note) The transfer pulses ($\phi 1$, $\phi 2$, ϕLH) must have more than 2775 cycles.
 Vout indicates Vout-R, Vout-G, Vout-B.

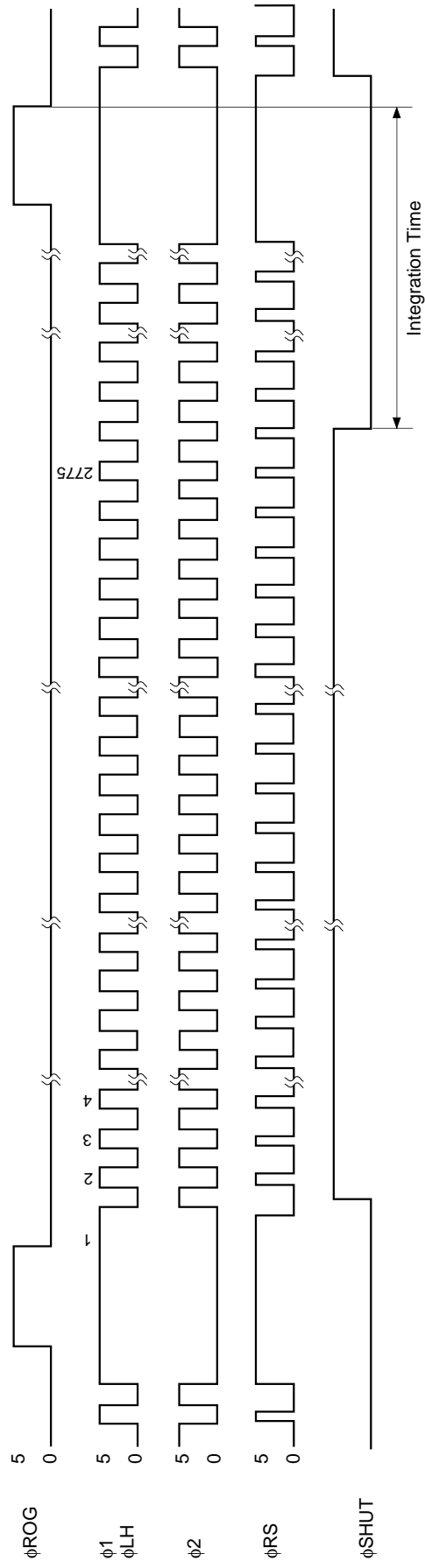
Clock Timing Chart 2



Clock Timing Chart 3



Clock Timing Chart 4 (Shutter Operation)



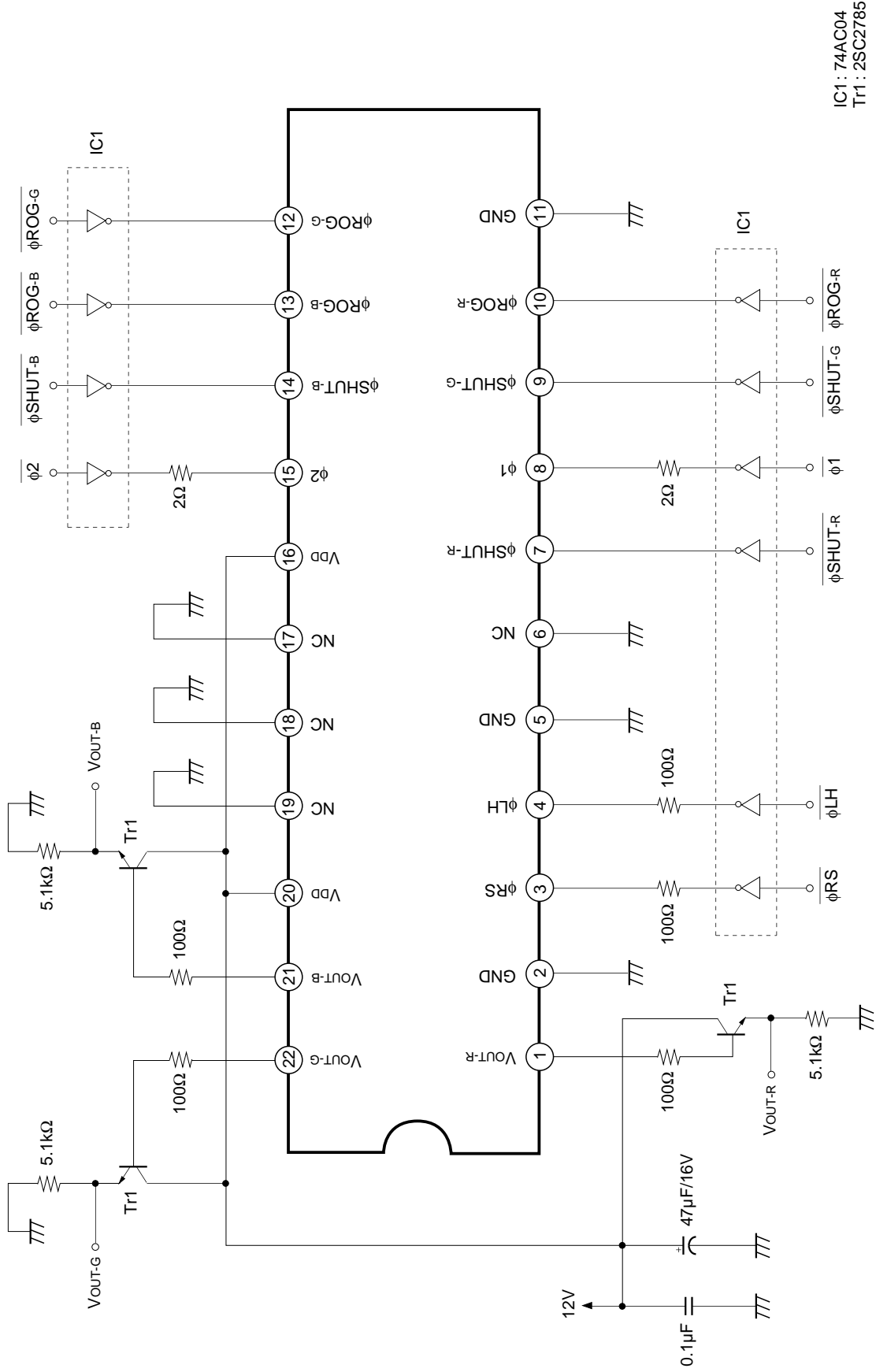
Note) Shutter pulse must be low level during from 2 to 2775 of ϕ 1.

Clock Pulse Recommended Timing

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|--------|------|-------|------|------|
| ϕ ROG, ϕ 1 pulse timing | t1 | 50 | 100 | — | ns |
| ϕ ROG pulse high level period | t2 | 800 | 1000 | — | ns |
| ϕ ROG, ϕ 1 pulse timing | t3 | 800 | 1000 | — | ns |
| ϕ ROG pulse rise time | t4 | 0 | 5 | 10 | ns |
| ϕ ROG pulse fall time | t5 | 0 | 5 | 10 | ns |
| ϕ 1 pulse rise time / ϕ 2 pulse fall time | t6 | 0 | 20 | 60 | ns |
| ϕ 1 pulse fall time / ϕ 2 pulse rise time | t7 | 0 | 20 | 60 | ns |
| ϕ RS pulse high level period | t8 | 45 | 250*1 | — | ns |
| ϕ RS, ϕ LH pulse timing | t9 | 45 | 250*1 | — | ns |
| ϕ RS pulse rise time | t10 | 0 | 10 | 30 | ns |
| ϕ RS pulse fall time | t11 | 0 | 10 | 30 | ns |
| Signal output delay time | t12 | — | 10 | — | ns |
| | t13 | — | 10 | — | ns |

*1 These timing is the recommended condition under $f_{\phi RS} = 1\text{MHz}$.

Application Circuit*

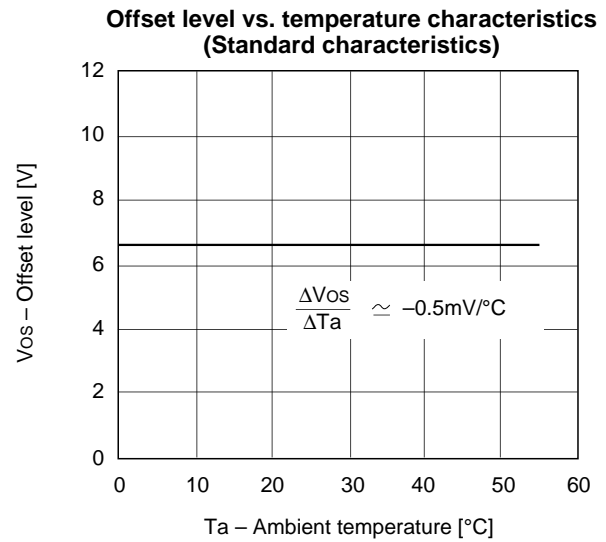
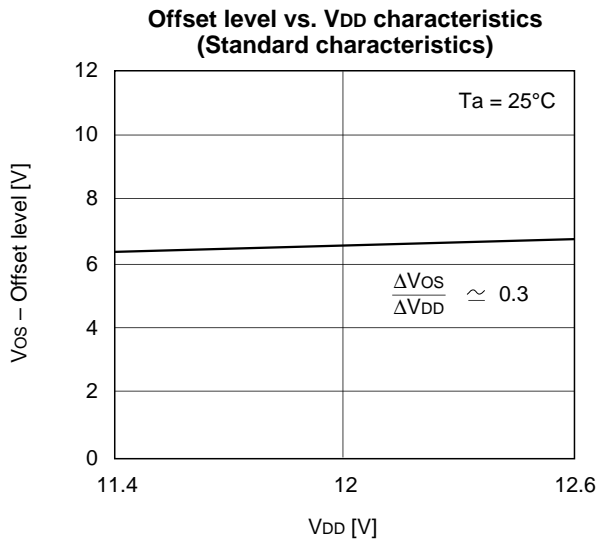
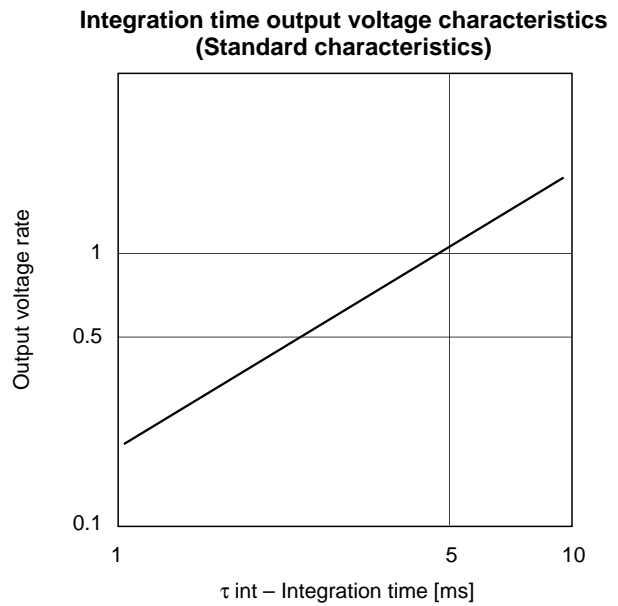
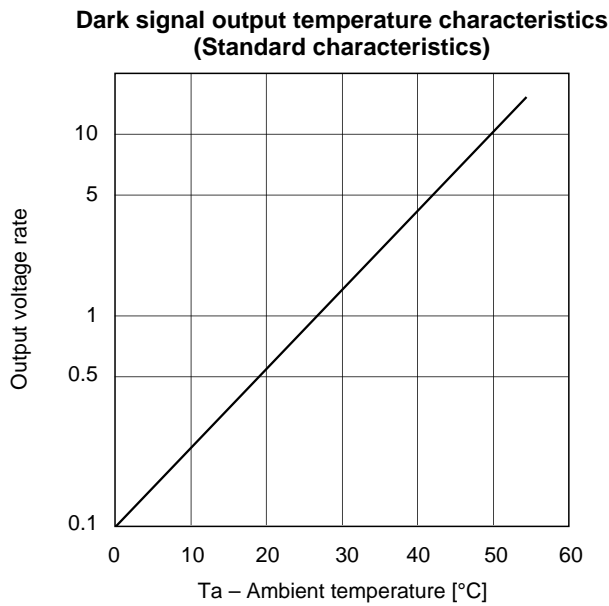
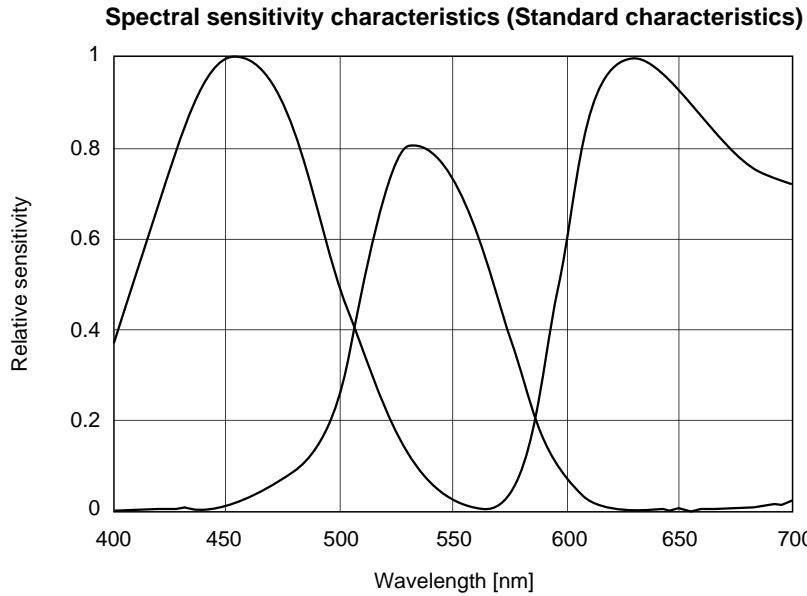


IC1 : 74AC04
Tr1 : 2SC2785

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

* Data rate φRS = 1MHz

Example of Representative Characteristics ($V_{DD} = 12V$, $T_a = 25^\circ C$)



Notes of Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

- a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
- b) When handling directly use an earth band.
- c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
- d) Ionized air is recommended for discharge when handling CCD image sensor.
- e) For the shipment of mounted substrates, use boxes treated for prevention of static charges.

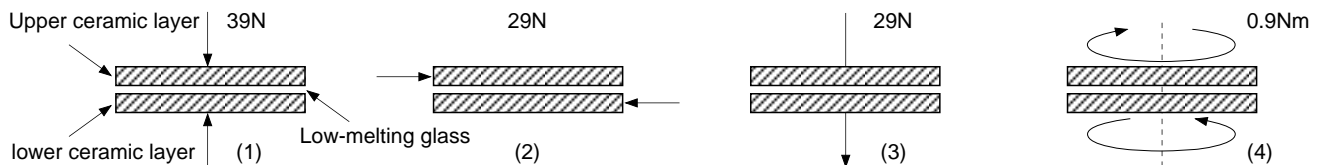
2) Notes on Handling CCD Cer-DIP Packages

The following points should be observed when handling and installing cer-DIP packages.

a) Remain within the following limits when applying static load to the ceramic portion of the package:

- (1) Compressive strength: 39N/surface (Do not apply load more than 0.7mm inside the outer perimeter of the glass portion.)
- (2) Shearing strength: 29N/surface
- (3) Tensile strength: 29N/surface
- (4) Torsional strength: 0.9Nm

b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.



c) Be aware that any of the following can cause the glass to crack: because the upper and lower ceramic layers are shielded by low-melting glass,

- (1) Applying repetitive bending stress to the external leads.
- (2) Applying heat to the external leads for an extended period of time with soldering iron.
- (3) Rapid cooling or heating.
- (4) Rapid cooling or impact to a limited portion of the low-melting glass with a small-tipped tool such as tweezers.
- (5) Prying the upper or lower ceramic layers away at a support point of the low-melting glass.

Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

3) Soldering

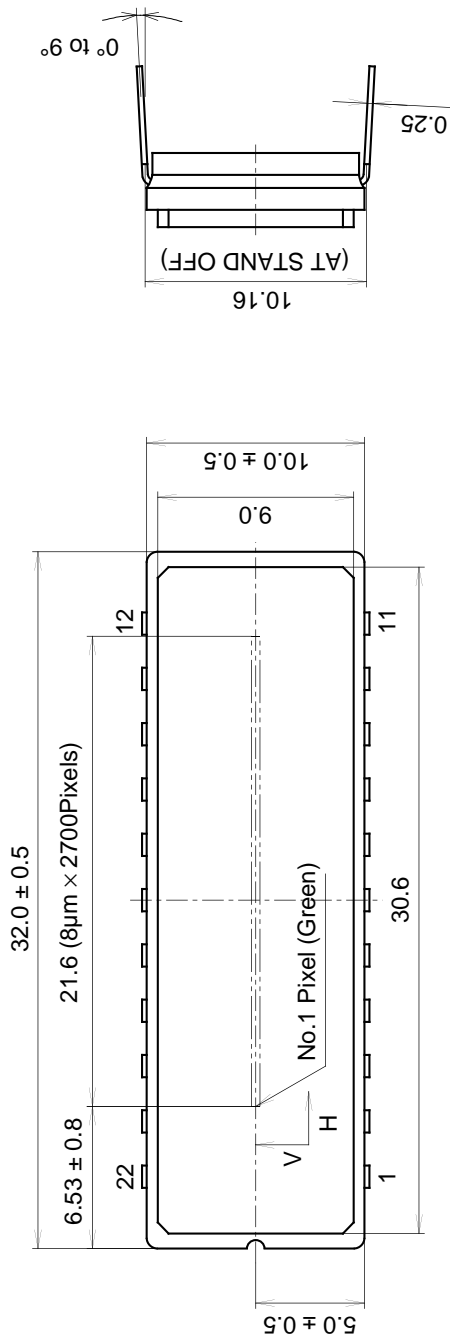
- a) Make sure the package temperature does not exceed 80°C.
- b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
- c) To dismount an imaging device, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

- 4) Dust and dirt protection
 - a) Operate in clean environments.
 - b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
 - c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
 - d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
- 5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
- 6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

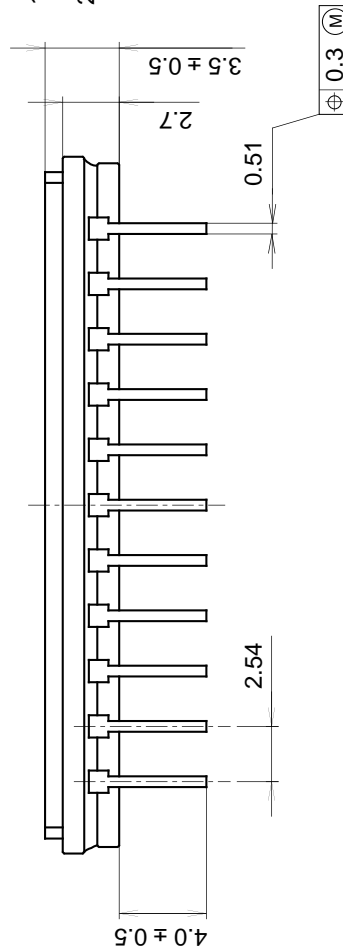
Package Outline

Unit: mm

22pin DIP (400mil)



1. The height from the bottom to the sensor surface is 1.61 ± 0.3 mm.
2. The thickness of the cover glass is 0.8mm, and the refractive index is 1.5.



PACKAGE STRUCTURE

| | |
|------------------|-------------|
| PACKAGE MATERIAL | Cer-DIP |
| LEAD TREATMENT | TIN PLATING |
| LEAD MATERIAL | 42 ALLOY |
| PACKAGE WEIGHT | 3.0g |