Data Sheet No. PD-9.509A
T-39-13

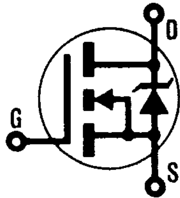
INTERNATIONAL RECTIFIER IOR

AVALANCHE AND dv/dt RATED

175°C OPERATING TEMPERATURE

HEXFET® TRANSISTORS

IRFZ34
IRFZ35



N-CHANNEL

TO-220

60 Volt, 0.050 Ohm HEXFET
TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dv/dt capability.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.

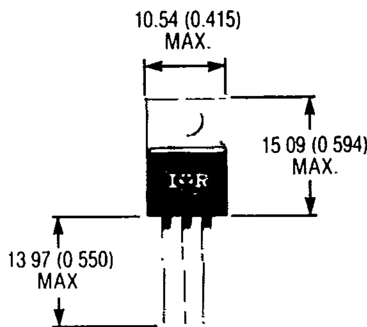
Product Summary

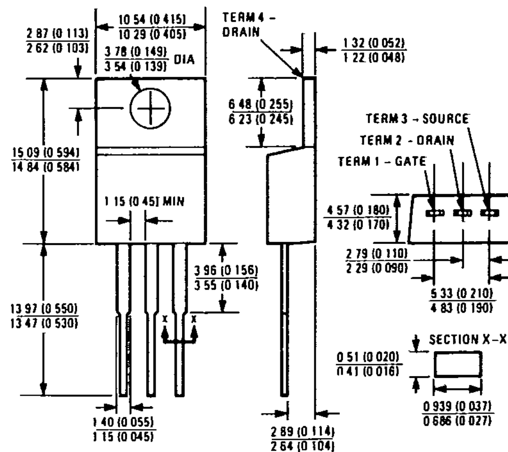
Part Number	BV_{DSS}	$R_{DS(on)}$	I_D
IRFZ34	60V	0.050Ω	30A
IRFZ35	60V	0.070Ω	25A

FEATURES

- Avalanche Rated
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling

CASE STYLE AND DIMENSIONS





Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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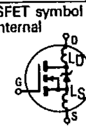
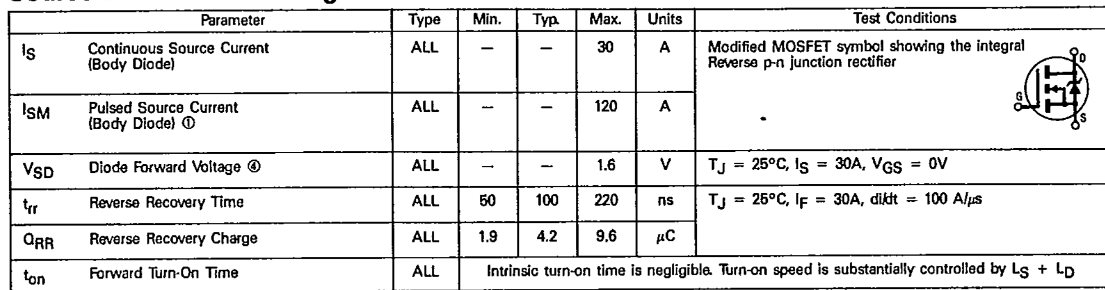
Absolute Maximum Ratings

	Parameter	IRFZ34	IRFZ35	Units
I_D @ T_C = 25°C	Continuous Drain Current	30	25	A
I_D @ T_C = 100°C	Continuous Drain Current	21	18	A
I_{DM}	Pulsed Drain Current ①	120	100	A
P_D @ T_C = 25°C	Max. Power Dissipation	90		W
	Linear Derating Factor	0.60		W/K ⑤
V_{GS}	Gate-to-Source Voltage	±20		V
E_{AS}	Single Pulse Avalanche Energy ②	19 (See Fig. 14)		mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5 (See Fig. 17)		V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	−55 to 175		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRFZ34 IRFZ35	60	–	–	V	V_{GS} = 0V, I_D = 250 μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ④	IRFZ34	–	0.040	0.050	Ω	V_{GS} = 10V, I_D = 18A
		IRFZ35	–	0.050	0.070		
$I_{D(on)}$	On-State Drain Current ④	IRFZ34	30	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ Max. V_{GS} = 10V
		IRFZ35	25				
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
g_{fs}	Forward Transconductance ④	ALL	9.3	14	–	S (℧)	V_{DS} ≥ 50V, I_{DS} = 18A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000		V_{DS} = 0.8 x Max. Rating V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	–	–	−500	nA	V_{GS} = −20V
Q_g	Total Gate Charge	ALL	–	32	47	nC	V_{GS} = 10V, I_D = 30A V_{DS} = 0.8 x Max. Rating
Q_{gs}	Gate-to-Source Charge	ALL	–	6.8	10	nC	See Fig. 16
Q_{gd}	Gate-to-Drain ("Miller") Charge		–	15	22	nC	(Independent of operating temperature)
$t_{d(on)}$	Turn-On Delay Time	ALL	–	14	21	ns	V_{DD} = 30V, I_D ≈ 30A, R_G = 12Ω
t_r	Rise Time	ALL	–	71	110	ns	R_D = 1.0Ω
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	35	53	ns	See Fig. 15
t_f	Fall Time	ALL	–	53	80	ns	(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die. Modified MOSFET symbol showing the internal inductances 
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad
C_{iss}	Input Capacitance	ALL	–	1300	–	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	–	650	–	pF	f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	–	pF	See Fig. 10

Source-Drain Diode Ratings and Characteristics



	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	—	—	30	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier
I_{SM}	Pulsed Source Current (Body Diode) ①	ALL	—	—	120	A	
V_{SD}	Diode Forward Voltage ④	ALL	—	—	1.6	V	$T_J = 25°C$, $I_S = 30A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	50	100	220	ns	$T_J = 25°C$, $I_F = 30A$, $di/dt = 100\ A/\mu s$
Q_{RR}	Reverse Recovery Charge	ALL	1.9	4.2	9.6	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$				

Thermal Resistance

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	ALL	—	—	1.7	K/W ⑤	
R_{thCS}	Case-to-Sink	ALL	—	0.50	—	K/W ⑤	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W ⑤	Typical socket mount

① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 5) Refer to current HEXFET reliability report

② @ $V_{DD} = 25V$, Starting $T_J = 25°C$, $L = 50\mu H$, $R_G = 25\Omega$, Peak $I_L = 21A$

③ $I_{SD} \leq 21A$ $di/dt \leq 200\ A/\mu s$, $V_{DD} \leq BV_{DSS}$, $T_J \leq 175°C$ Suggested $R_G = 12\Omega$

④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

⑤ K/W = °C/W
W/K = W/°C

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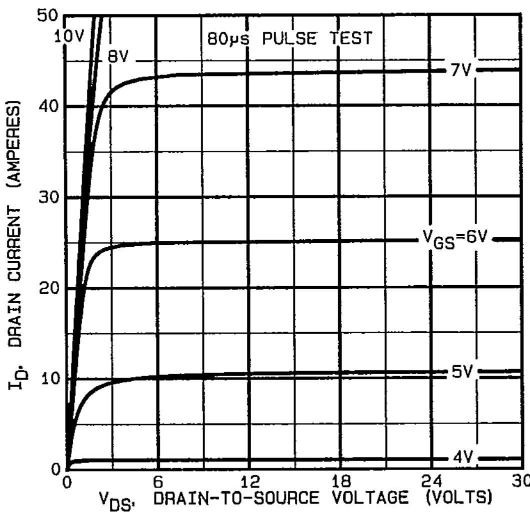

Fig. 1 — Typical Output Characteristics

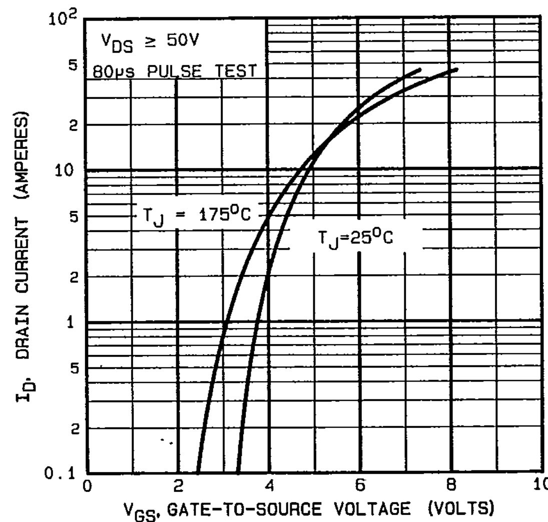

Fig. 2 — Typical Transfer Characteristics

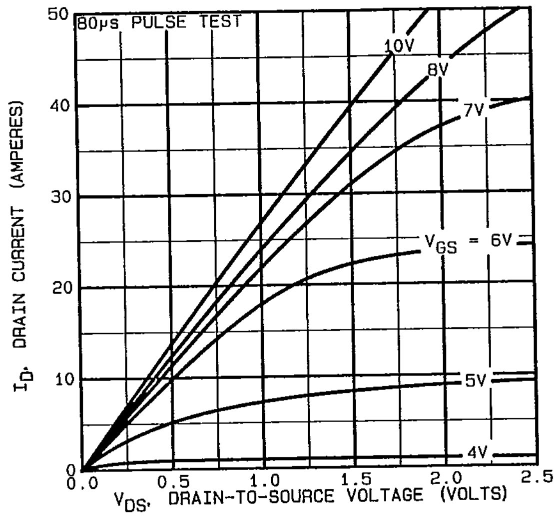

Fig. 3 — Typical Saturation Characteristics

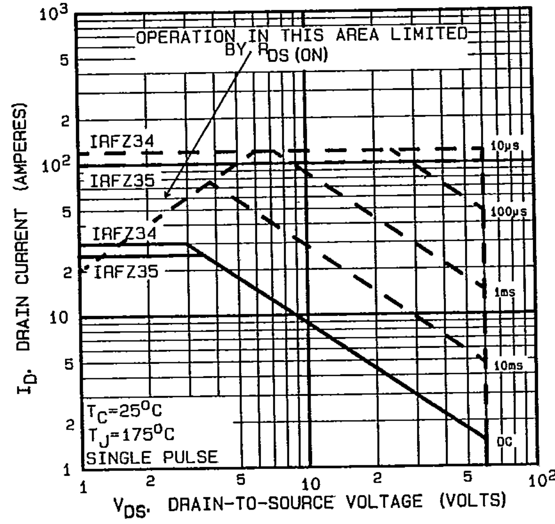

Fig. 4 — Maximum Safe Operating Area

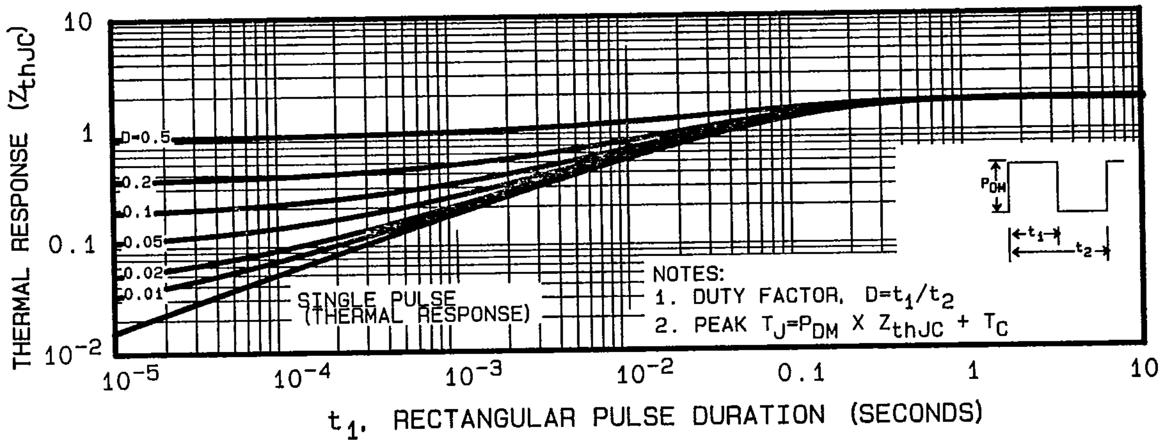

Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

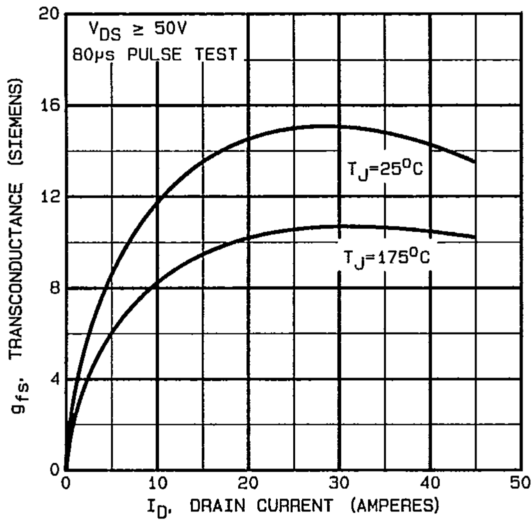

Fig. 6 — Typical Transconductance Vs. Drain Current

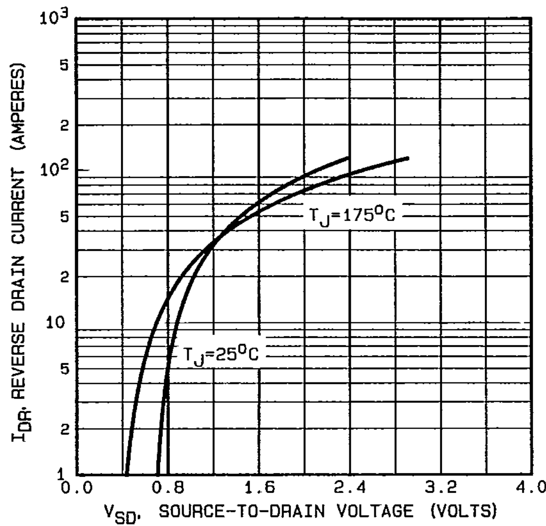

Fig. 7 — Typical Source-Drain Diode Forward Voltage

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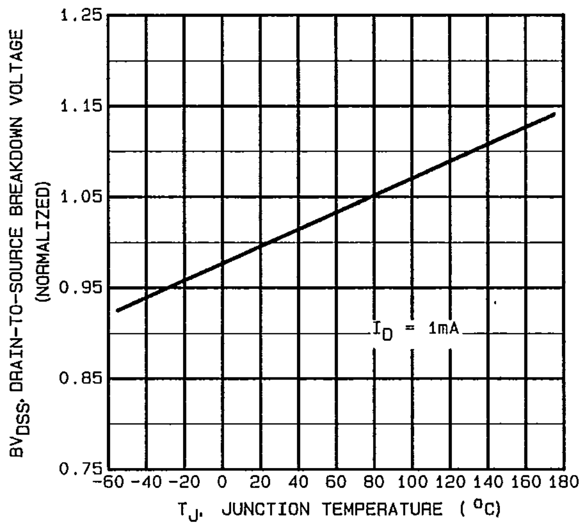

Fig. 8 — Breakdown Voltage Vs. Temperature

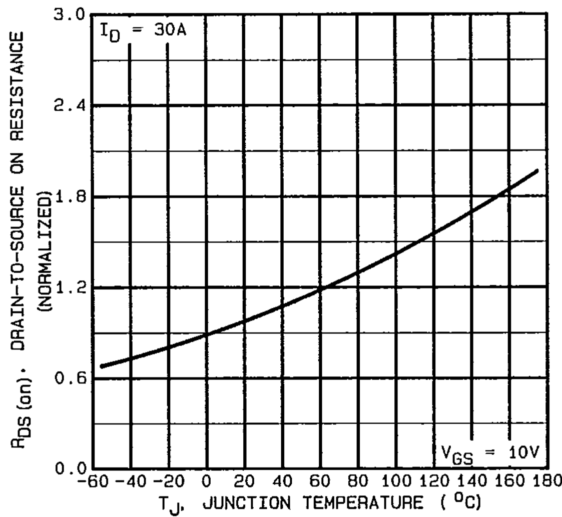

Fig. 9 — Normalized On-Resistance Vs. Temperature

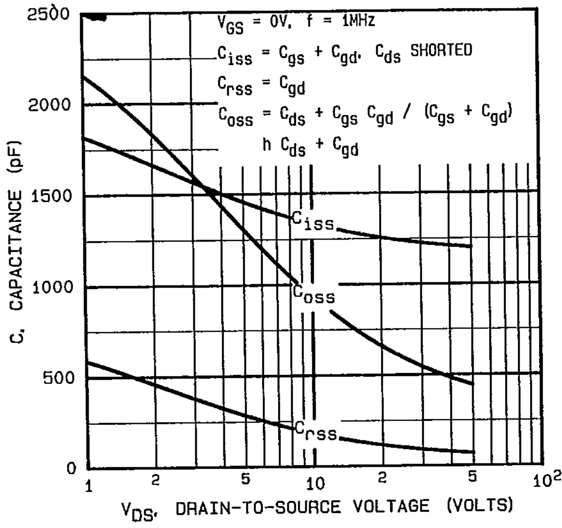

Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

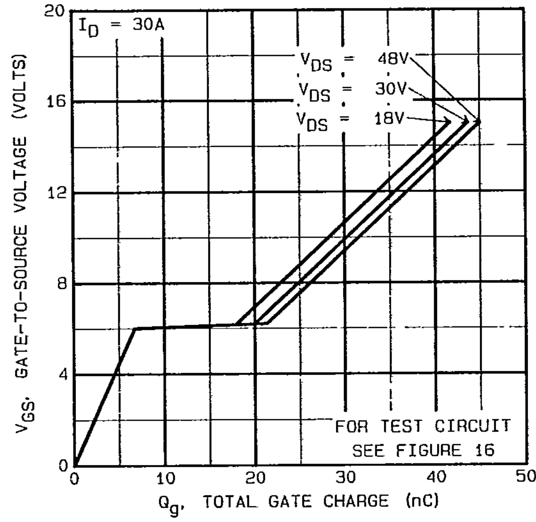

Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

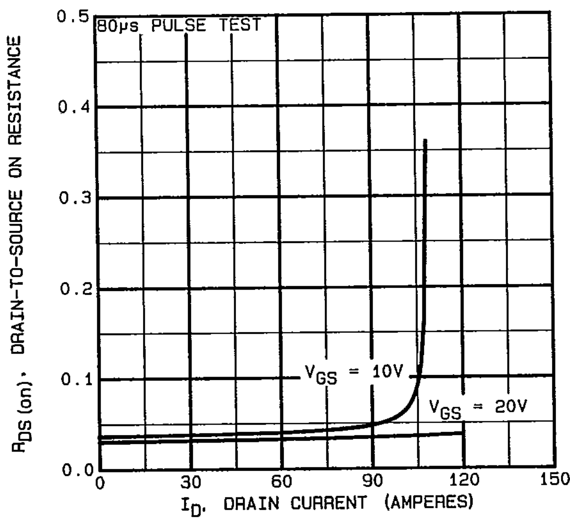

Fig. 12 — Typical On-Resistance Vs. Drain Current

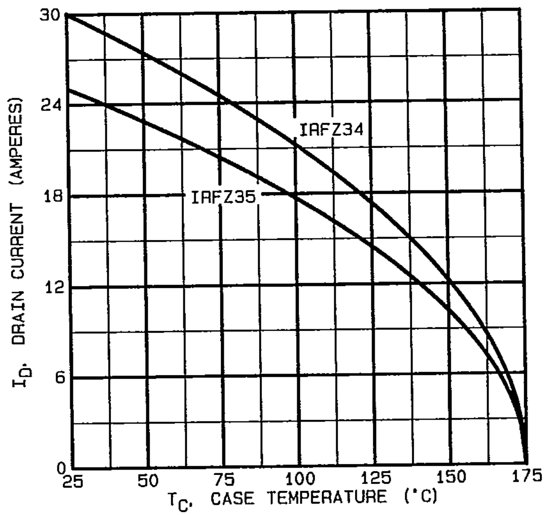

Fig. 13 — Maximum Drain Current Vs. Case Temperature

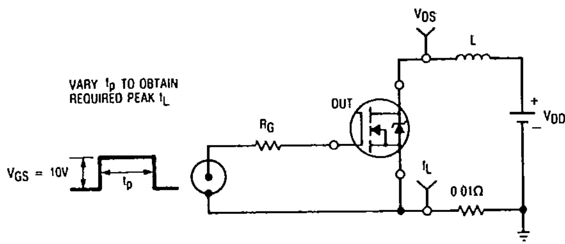

Fig. 14a — Unclamped Inductive Test Circuit

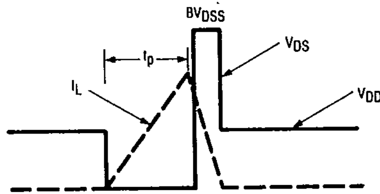

Fig. 14b — Unclamped Inductive Waveforms

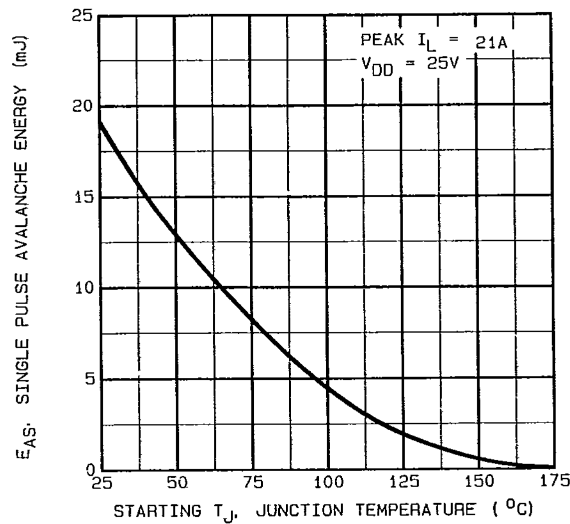

Fig. 14c — Maximum Avalanche Energy Vs. Starting Junction Temperature

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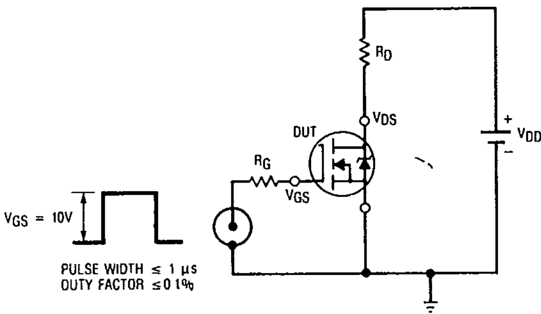

Fig. 15a — Switching Time Test Circuit

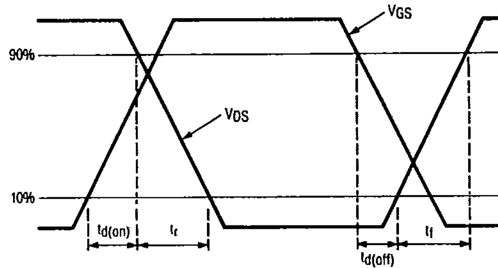

Fig. 15b — Switching Time Waveforms

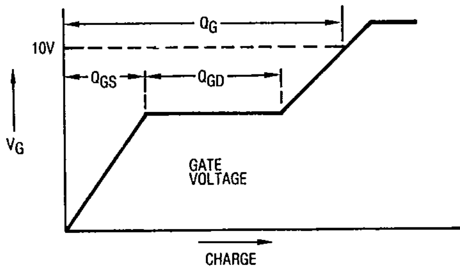

Fig. 16a — Basic Gate Charge Waveform

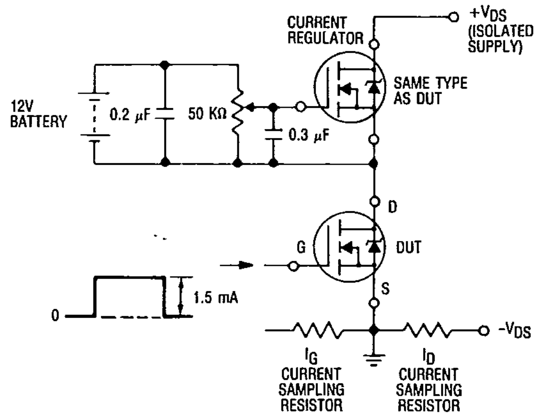

Fig. 16b — Gate Charge Test Circuit

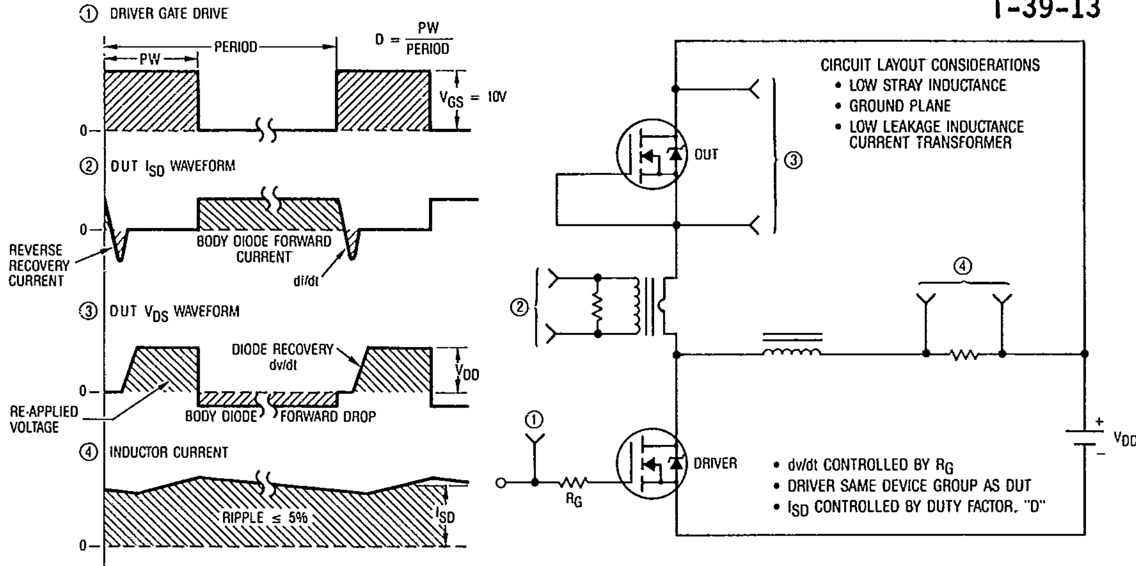

Fig. 17 — Peak Diode Recovery dv/dt Test Circuit

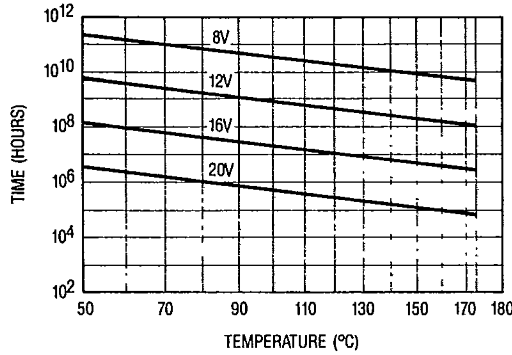

***Fig. 18 — Typical Time to Accumulated 1% Gate Failure**

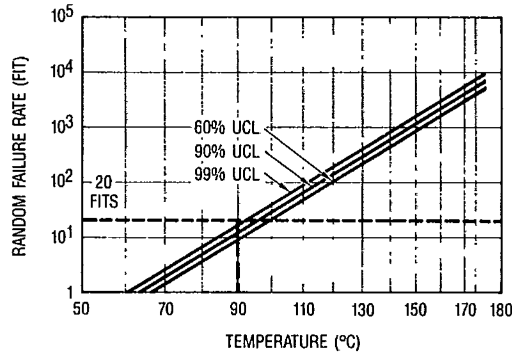

***Fig. 19 — Typical High Temperature Reverse Bias (HTRB) Failure Rate**

*The data shown is correct as of January 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.