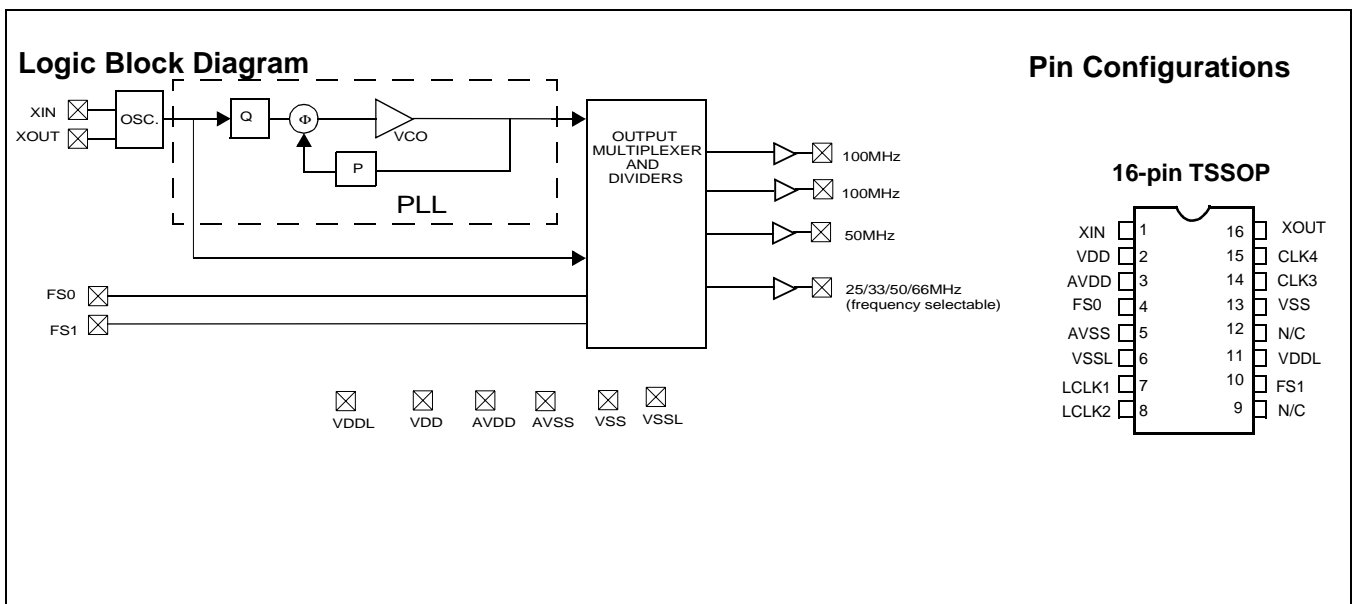




One-PLL Clock Generator

Features	Benefits
• Integrated phase-locked loop	Internal PLL with up to 333 MHz internal operation
• Low skew, low jitter, high accuracy outputs	Meets critical timing requirements in complex system designs
• 3.3V Operation with 2.5 V Output Option	Enables application compatibility

Part Number	Outputs	Input Frequency	Output Frequency Range
CY26114	4	25MHz Crystal Input	2 copies of 100MHz, 1 copy of 50MHz, 1 copy 25/33/50/66MHz (frequency selectable)



CLK4 Frequency Select Options

FS1	FS0	CLK 4	Units
0	0	25	MHz
0	1	33	MHz
1	0	50	MHz
1	1	66	MHz

**Pin Definitions**

Name	Pin Number	Description
XIN	1	Reference Crystal Input
V <sub>DD</sub>	2	Voltage Supply
AV <sub>DD</sub>	3	Analog Voltage Supply
FS0	4	Frequency Select 0
AV <sub>SS</sub>	5	Analog Ground
V <sub>SSL</sub>	6	LCLK Ground
LCLK1	7	100-MHz output clock at V <sub>DDL</sub> Level
LCLK2	8	100-MHz output clock at V <sub>DDL</sub> Level
N/C	9	No Connect
FS1	10	Frequency Select 1
V <sub>DDL</sub>	11	LCLK Voltage Supply (2.5V or 3.3V)
N/C	12	No Connect
VSS	13	Ground
CLK3	14	50-MHz output clock
CLK4	15	25/33/50/66-MHz clock output (frequency selectable)
XOUT	16	Reference Crystal Output

**Absolute Maximum Conditions**

Parameter	Description	Min.	Max.	Unit
V <sub>DD</sub>	Supply Voltage	-0.5	7.0	V
V <sub>DDL</sub>	I/O Supply Voltage		7.0	V
T <sub>J</sub>	Junction Temperature		125	°C
	Digital Inputs	AV <sub>SS</sub> - 0.3	AV <sub>DD</sub> + 0.3	V
	Digital Outputs referred to V <sub>DD</sub>	V <sub>SS</sub> - 0.3	V <sub>DD</sub> + 0.3	V
	Digital Outputs referred to V <sub>DDL</sub>	V <sub>SS</sub> - 0.3	V <sub>DDL</sub> + 0.3	V
	Electro-Static Discharge	2		kV

**Recommended Operating Conditions**

Parameter	Description	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Operating Voltage	3.0	3.3	3.6	V
V <sub>DDL</sub>	Operating Voltage	2.375	2.5	2.625	V
T <sub>A</sub>	Ambient Temperature	0		70	°C
C <sub>LOAD</sub>	Max. Load Capacitance			15	pF
f <sub>REF</sub>	Reference Frequency		25		MHz
t <sub>PU</sub>	Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

**Note:**

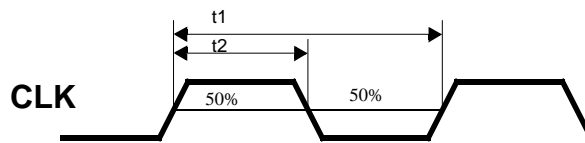
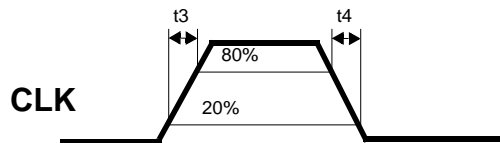
1. Float XOUT if XIN is externally driven.

**DC Electrical Characteristics**

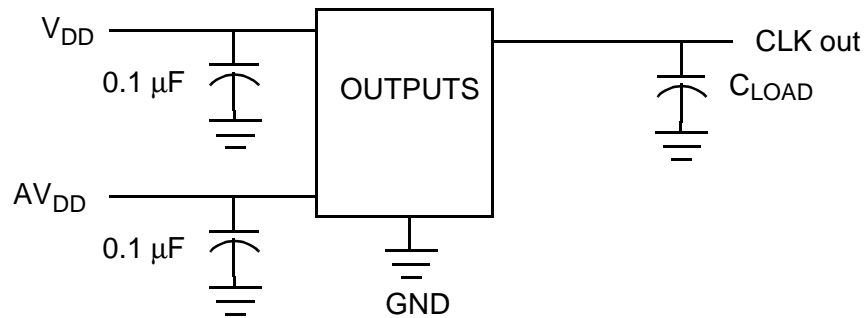
Parameter <sup>[2]</sup>	Name	Description	Min.	Typ.	Max.	Unit
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> - 0.5, V <sub>DD</sub> /V <sub>DDL</sub> = 3.3V	12	24		mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.5, V <sub>DD</sub> /V <sub>DDL</sub> = 3.3V	12	24		mA
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DDL</sub> - 0.5, V <sub>DDL</sub> = 2.5V	8	16		mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.5, V <sub>DDL</sub> = 2.5V	8	16		mA
V <sub>IH</sub>	Input High Voltage	CMOS levels, 70% of V <sub>DD</sub>	0.7			VDD
V <sub>IL</sub>	Input Low Voltage	CMOS levels, 30% of V <sub>DD</sub>			0.3	VDD
I <sub>VDD</sub>	Supply Current	AV <sub>DD</sub> /V <sub>DD</sub> Current			25	mA
I <sub>VDDL</sub>	Supply Current	V <sub>DDL</sub> Current (V <sub>DDL</sub> = 3.6V)			20	mA
I <sub>VDDL</sub>	Supply Current	V <sub>DDL</sub> Current (V <sub>DDL</sub> = 2.625V)			15	mA

**AC Electrical Characteristics**

Parameter <sup>[2]</sup>	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in Figure 1; t <sub>1</sub> /t <sub>2</sub> , 50% of V <sub>DD</sub>	45	50	55	%
t <sub>3</sub>	Rising Edge Rate	Output Clock Rise Time, 20% – 80% of V <sub>DD</sub> /V <sub>DDL</sub> = 3.3V	0.8	1.4		V/ns
t <sub>3</sub>	Rising Edge Rate	Output Clock Rise Time, 20% – 80% of V <sub>DDL</sub> = 2.5V	0.6	1.2		V/ns
t <sub>4</sub>	Falling Edge Rate	Output Clock Fall Time, 80% – 20% of V <sub>DD</sub> /V <sub>DDL</sub> = 3.3V	0.8	1.4		V/ns
t <sub>4</sub>	Falling Edge Rate	Output Clock Fall Time, 80% – 20% of V <sub>DDL</sub> = 2.5V	0.6	1.2		V/ns
t <sub>5</sub>	Skew	Delay between related outputs at rising edge			250	ps
t <sub>9</sub>	Clock Jitter	Peak to Peak period jitter			200	ps
t <sub>10</sub>	PLL Lock Time				3	ms


**Figure 1. Duty Cycle Definitions: DC = t<sub>2</sub>/t<sub>1</sub>.**

**Figure 2. Rise Time and Fall Time Definitions.**
**Note:**

- Not 100% tested.

**Test Circuit**

**Ordering Information**

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY26114ZC	Z16	16-Pin TSSOP	Commercial	3.3V



<b>Document Title: CY26114 One-PLL Clock Generator</b> <b>Document Number: 38-07098</b>				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	107333	08/28/01	CKN	New Data Sheet
*A	121867	12/14/02	RBI	Power up requirements added to Operating Conditions Information