Agilent HPFC-5000 Tachyon Fibre Channel Interface Controller

Product Brief

Description

Tachyon is a fundamental building block compatible with Agilent Technologies' Fibre Channel solution which includes interface controllers, physical link modules, adapters, switches and disk drives.

The Tachyon architecture supports both networking and mass storage connections to provide a low cost, high performance solution with low host overhead.

Internal Block Diagram

The Internal Block Diagram in Figure 1 below shows the high-level chip architecture for Tachyon.

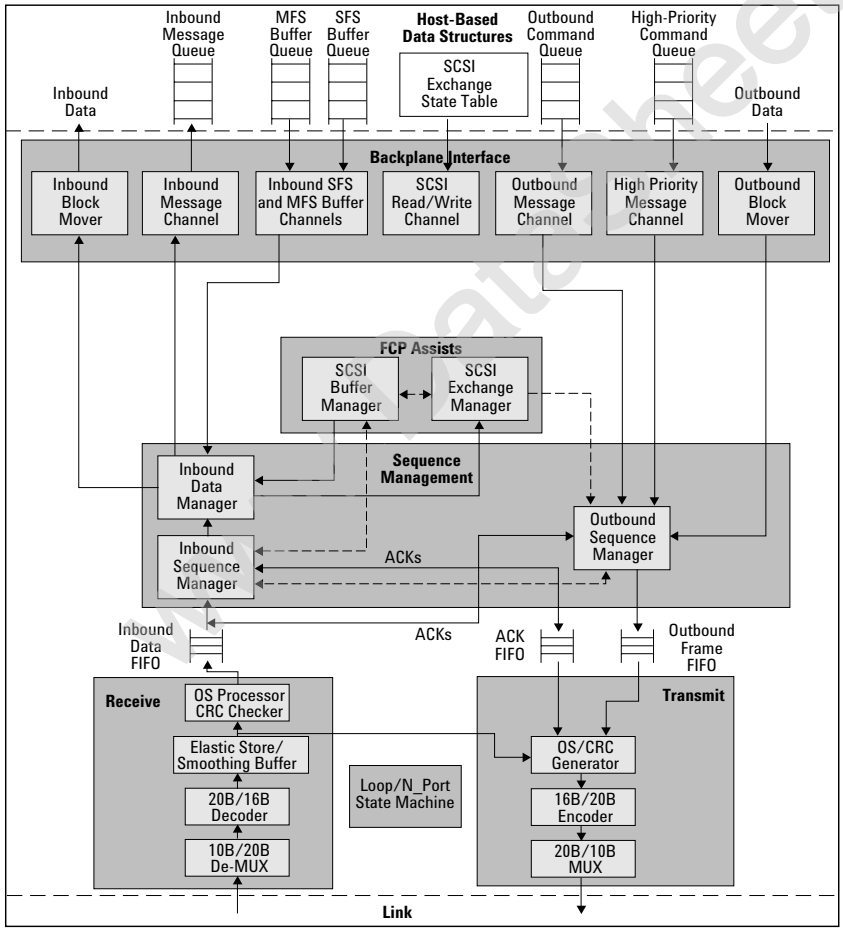

Figure 1.

Specifications

- **System clock frequency:**
  20–40 MHz backplane operation
- **Testability:**
  Full internal scan path
  IEEE Standard 1149.1 boundary scan
- **Packaging:**
  208-pin metal quad flat pack
- **Standards:**
  Intended to be compliant with ANSI standards and FCSI/FCA profile definitions

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Features

- Single chip Fibre Channel interface (no I/O processor required)
- Supports 1062, 531 and 266 Mbaud links
- Supports 3 topologies – direct connect, fabric and Fibre Channel Arbitrated Loop (FC-AL)
- Supports Fibre Channel Class 1, 2 and 3 services
- Supports up to 2 Kbyte frame payload for all classes of service
- Sequence segmentation/reassembly in hardware
- Automatic ACK frame generation and processing
- On-chip support of FCP for SCSI initiators and targets
- Supports up to 16384 concurrent SCSI I/O transactions
- Compliant with Internet MIB-II network management
- Direct interface to industry standard 10 and 20-bit Gigabit Link Module (GLM)
- Hardware assists for TCP/UDP/IP networking
- Parity protection on internal data path
- Eight internal DMA channels
- Full duplex internal architecture that allows Tachyon to process inbound and outbound data simultaneously

Pin-out Block Diagram

Figure 2 below shows the pin-out block diagram for Tachyon.

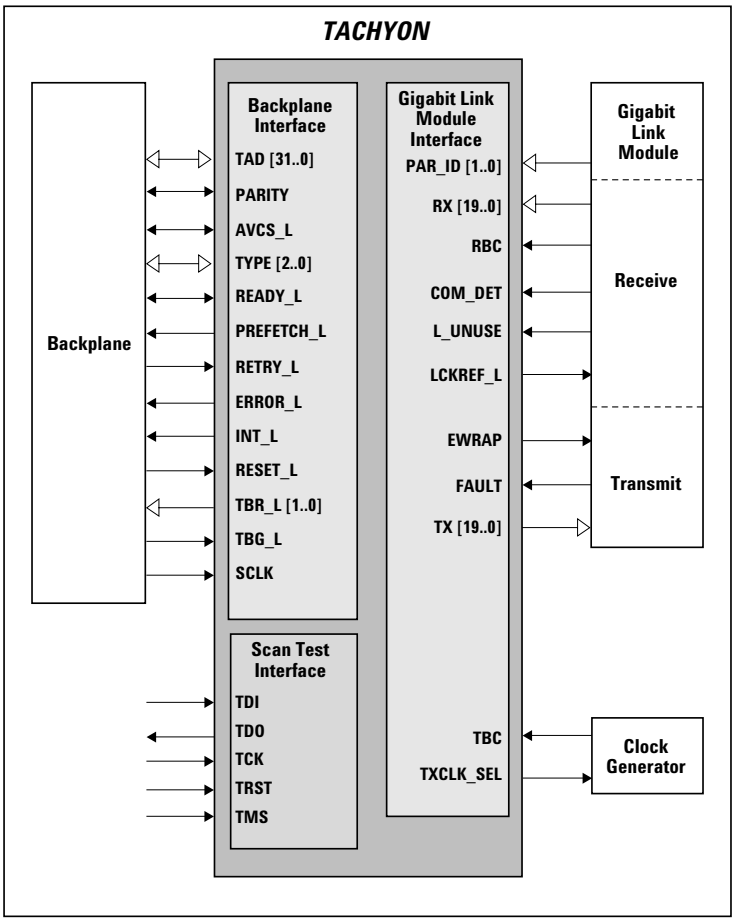

Figure 2.

System Adapter Card Block Diagram

Figure 3 below shows an example of a Tachyon on a generic host bus adapter.

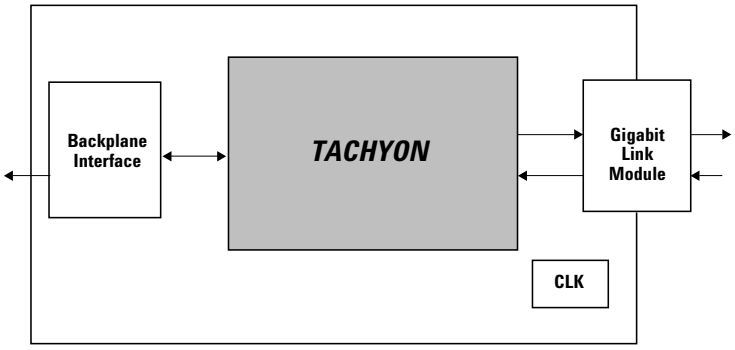

Figure 3.

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