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SSI 32H6240
Servo Motor Driver

Advance Information

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DESCRIPTION

The SSI 32H6240 Servo Motor Driver is a bipolar device intended for use in Winchester disk drive head positioning systems employing linear or rotary voice coil motors. When used in conjunction with a position controller, such as the SSI 32H6220 Servo Controllers, and a position reference, such as the SSI 32H567 Servo Demodulator, the device allows the construction of a high performance, dedicated surface head positioning system.

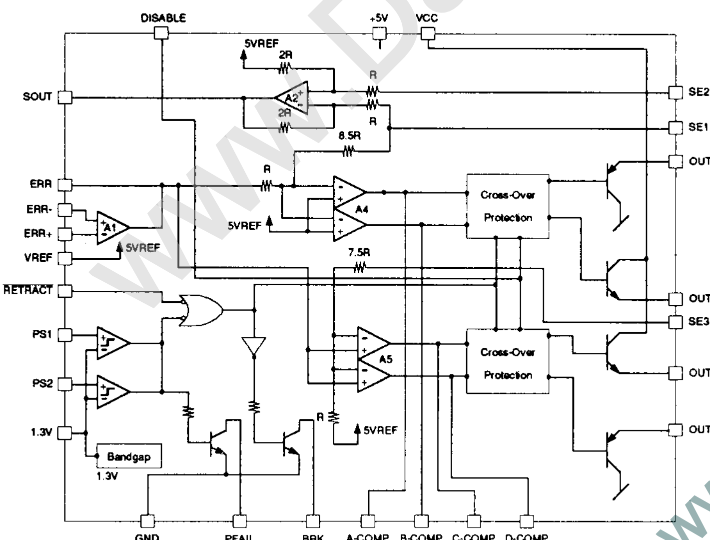
The SSI 32H6240 serves as a transconductance amplifier by driving 4 bipolar power transistors in an H–bridge configuration and performs motor current sensing by using an on-chip differential amplifier. In its linear tracking mode, class B operation is guaranteed by crossover protection circuitry, which ensures that only one transistor in each leg of the H-bridge is active. Automatic head retraction and spindle braking may be initiated by a low voltage condition or upon external command.

The SSI 32H6240 is implemented in an advanced bipolar process and dissipates less than (240 mW) from a 12V supply. The SSI 32H6240 is available in a 28-pin PLCC.

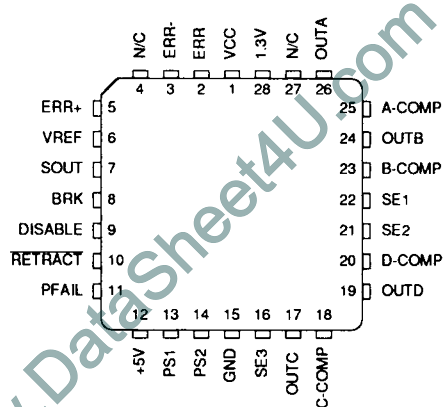
FEATURES

- **Predriver for linear and rotary voice coil motors**
- **Interfaces directly to Bipolar H-Bridge motor driver**
- **Class B linear mode and constant velocity retract mode**
- **Power transistor disable function**
- **Precision differential amplifier for motor current sensing**
- **On-chip precision power fail detect**
- **Automatic head retract and spindle braking signal on power failure**
- **External digital enable**
- **Servo loop parameters programmed with external components**
- **Advanced bipolar IC requires under (240 mW) from 12V supply**
- **Available in 28-pin PLCC packaging**
- **+5V, +12V operation**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

(Refer to block diagram and typical application Fig.2)

There are three modes of operation of the SSI 32H6240: Disable, Retract, and Linear. The circuit mode is controlled by the DISABLE , $\overline{\text{RETRACT}}$, PS1, and PS2 pins.

DISABLE mode turns off the output drivers. OUTA and OUTC are pulled to VCC through internal 1.5 kΩ resistors. OUTB and OUTD are pulled to GND through internal 1.5 kΩ resistors. Disable mode does not override Retract mode.

RETRACT mode turns off OUTB and OUTC. OUTD is turned on. OUTA is turned on in a special manner to force 1V at SE1. Retract mode does override Disable mode.

POWER FAIL mode occurs when either PS1 or PS2 fall below 1.3V. Power fail overrides Retract and Disable inputs and forces the chip into RETRACT mode.

When the $\overline{\text{RETRACT}}$ pin is pulled low the SSI 32H6240 will go into retract mode. The BRK pin will go high. When the DISABLE pin is pulled high it will cause all 4 bridge power transistors to turn off. PFAIL and BRK will remain low if PS1, PS2, and $\overline{\text{RETRACT}}$ pins do not change.

During linear mode operation an acceleration signal from the servo controller is applied through amplifier A1. Amplifier A1's three connections are available for connection to external loop compensation components. The ERR signal drives two precision amplifiers, each with a gain of 8.5. The first of these amplifiers is inverting, and is formed from opamp A4, an on-chip resistor divider, and an off-chip complementary Bipolar Power Transistor pair. The second amplifier is non-inverting and is formed in a similar manner from opamp A5. Feedback from external transistor's collectors on sense inputs SE1 and SE3 allows the amplifier's gains to be precisely set. The voice coil motor and a series current sense resistor are connected between SE1 and SE3. The output of the amplifiers will provide the base current for the external H-Bridge Bipolar Power Transistors. The chip is designed to work with external transistors with a minimum Beta of 40 and minimum f_T of 40 MHz. The base bias resistors for the external bridge transistors are internal to the IC.

Cross over protection circuitry between the outputs of A4 and A5 and the external power transistors ensure Class B operation by allowing only one transistor in each leg of the H-bridge to be in conduction. The crossover circuitry can also disable all Power Transistors simultaneously (to limit motor current or velocity) or apply a constant voltage across the motor (to retract the heads at a constant velocity.)

Motor current is sensed by a small resistor placed in series with the motor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 2 (A2 and associated resistors), whose inputs are SE1 and SE2. The resulting output voltage, SOUT, is proportional to motor current, and hence acceleration. This signal is externally fed back to A1 so that the signal ERR represents the difference between the desired acceleration (from the servo controller) and the actual motor acceleration. The total output offset current (Vin = Vref, Rsense = 0.5 Ω) is less than 5.5 mA.

The SSI 32H6240 has low voltage monitor circuitry that will detect a decrease in the voltage at PS1 and PS2 pins. The +5V and +12V power supplies are divided down by external resistors and then compared to an internal 1.25V ±5% reference. The power supply pin, VCC, should be connected to the disk drive's spindle motor so that its stored rotational energy may be used to hold up VCC briefly during a power failure. When a low voltage condition is detected on either the PS1 or PS2 pins the BIPOLAR drivers switch from linear operation to retract mode. In this mode a constant voltage is applied across the motor which will cause the heads to move at a constant speed. A mechanical stop must be provided for the heads when they reach a safe location. External current limiting circuitry is required for both the linear and retract modes of operation. An open collector output, PFAIL, which is low in the linear mode, will go high to indicate a power failure. This signal is gated with the $\overline{\text{RETRACT}}$ input signal to force the chip into the Retract mode during power failure and to signal a BRK spindle. A BRK spindle is signaled by forcing a High level on the BRK open collector output which is normally low in the Linear mode. The BRK pin is provided for spindle motor braking. An external RC delay may be used to defer braking until the heads are retracted.

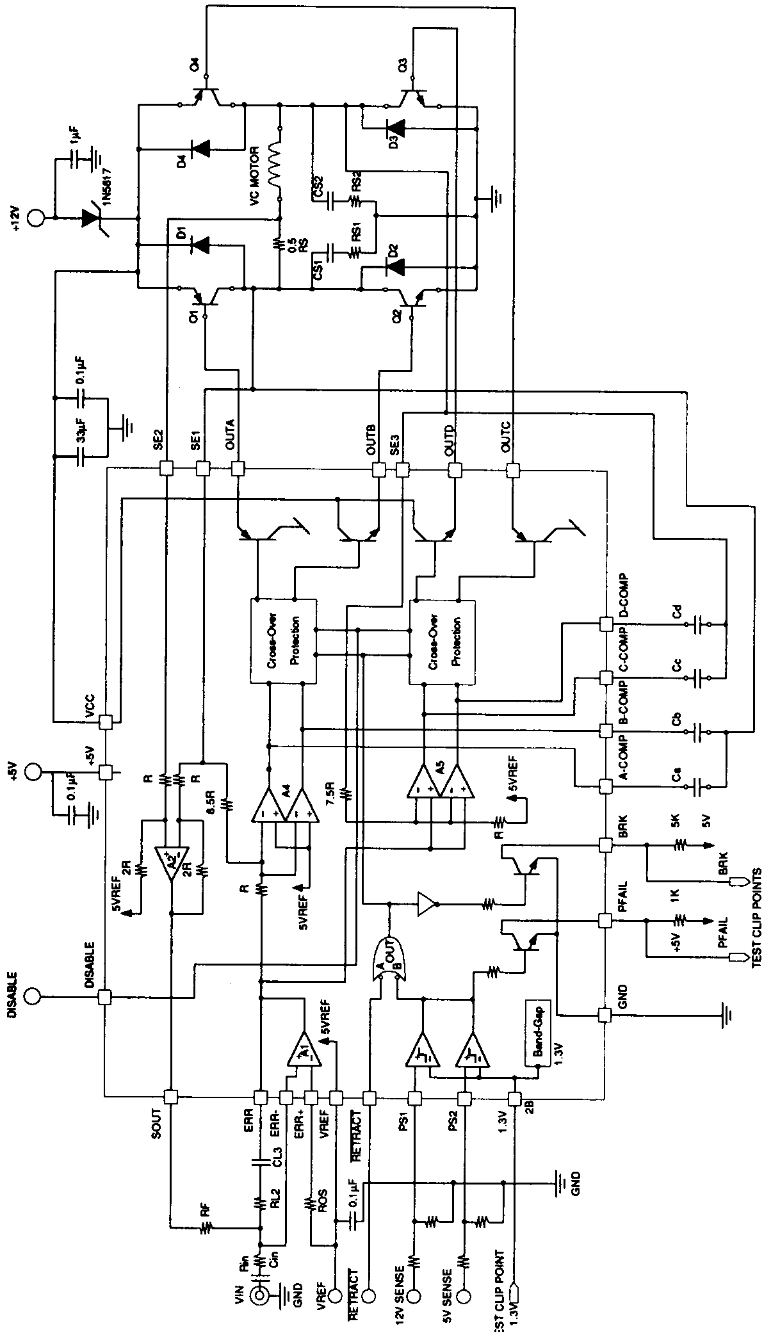


FIGURE 2: SSI 32H6240 Typical Application

PIN DESCRIPTION

POWER

NAME	TYPE	DESCRIPTION
VCC	-	POSITIVE SUPPLY - Usually taken from spindle motor supply. Spindle motor stored energy permits head retraction during power failure. If either a "Power Failure" or a "Retract" is asserted a forced head retraction occurs. Usually supplied through a power Schottky diode from Spindle Motor Supply.
+5V	I	5-volt power supply
VREF	I	REFERENCE VOLTAGE - 5.0V input. All analog signals are referenced to this input.
GND	-	GROUND

CONTROL

NAME	TYPE	DESCRIPTION
ERR	O	POSITION ERROR- Loop compensation amplifier output. This signal is amplified by the BIPOLAR drivers and applied to the motor by an external BIPOLAR H-bridge, as follows: SE3-SE1 = 17 (ERR-VREF)
ERR-	I	POSITION ERROR INVERTING INPUT - Inverting input to the loop compensation amplifier.
ERR+	I	POSITION ERROR NON-INVERTING INPUT - Non-inverting input to the loop compensation amplifier.
SOUT	O	MOTOR CURRENT SENSE OUTPUT - This output provides a voltage proportional to the voltage drop across the external current sense resistor, as follows: SOUT-VREF=4 (SE2-SE1)
BRK	O	BRAKE OUTPUT - Active high, open collector output which may be used to enable an external spindle motor braking transistor upon power failure. External resistor may be tied to +5 or +12V.
DISABLE	I	DISABLE DRIVERS INPUT – Logic level input. An input high level will cause all 4 bridge BIPOLAR Power Devices to turn off. DISABLE does not override retract.
$\overline{\text{RETRACT}}$	I	$\overline{\text{RETRACT}}$ INPUT – Logic level low will assert a forced head retraction. RETRACT will override DISABLE. $\overline{\text{RETRACT}}$ will continue to work at VCC=3.5V.
PS1	I	POWER SENSE 1 – 12V sense input to power fail comparator.
PS2	I	POWER SENSE 2 – 5V sense input to power fail comparator.
PFAIL	O	POWER FAIL – Power fail indicator open collector output. Floats if either supply goes below threshold.
1.3V	O	INTERNAL REFERENCE MONITOR - Used for testing purposes only.
A-COMP	O	AMPLIFIER A COMPENSATION - Compensation capacitor pin
B-COMP	O	AMPLIFIER B COMPENSATION - Compensation capacitor pin
C-COMP	O	AMPLIFIER C COMPENSATION - Compensation capacitor pin
D-COMP	O	AMPLIFER D COMPENSATION - Compensation capacitor pin

CONTROL (Continued)

NAME	TYPE	DESCRIPTION
SE2	I	MOTOR CURRENT SENSE INPUT - Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the motor. The inverting input of the differential amplifier is connected internally to SE1.

BIPOLAR DRIVE

SE3	I	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the non-inverting BIPOLAR driver amplifier. It is connected to one side of the motor. The gain to this point is: SE3-VREF = 8.5 (ERR-VREF)
SE1	I	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the inverting BIPOLAR driver amplifier. It is connected to the current sensing resistor which is in series with the motor. The gain to this point is: SE1 - VREF = -8.5 (ERR-VREF)
OUTA	O	PNP DRIVE (INVERTING) - Drive signal for a PNP power transistor connected between the current sense resistor and VCC. The PNP collector is also connected to SE1. Crossover protection circuitry ensures that the PNP and NPN devices driven by OUTA and OUTB are never simultaneously enabled.
OUTB	O	NPN DRIVE (INVERTING) - Drive signal for an NPN power transistor connected between the current sense resistor and GND. This NPN collector is also connected to SE1.
OUTC	O	PNP DRIVE (NON-INVERTING) - Drive signal for a PNP power transistor connected between one side of the motor and VCC. This PNP collector is connected to SE3. Crossover protection circuitry ensures that the PNP and NPN devices driven by OUTC and OUTD are never simultaneously enabled.
OUTD	O	NPN DRIVE (NON-INVERTING) - Drive signal for an NPN power transistor connected between one side of the motor and GND. This NPN collector is connected to SE3. Crossover protection circuitry ensures that the PNP and NPN devices driven by OUTC and OUTD are never simultaneously enabled.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicates where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC		0		16	V
VREF		0		10	V
+5V		0		7	V
SE1, SE2, SE3		-1.5		15	V
DISABLE, $\overline{\text{RETRACT}}$		-.3		+5V + .3	V
All other pins		-.3		VCC + .3	V
Storage temperature		-45		165	°C
Solder temperature	10 sec duration			260	°C

RECOMMENDED OPERATION CONDITIONS (Unless otherwise noted, the following conditions are valid throughout this document.)

VCC	Normal Mode	9	12	13.2	V
	Retract Mode	3.5V		13.2	V
+5V		4.5	5	5.5	V
VREF		4.5	5	5.5	V
Operating temperature		0		70	°C

DC CHARACTERISTICS

ICC, VCC current			13	20	mA
I5V, +5V Current			0.6	1	mA
IREF, VREF current			300		µA

A1, LOOP COMPENSATION AMPLIFIER

Input bias current				500	nA
Input offset voltage				3	mV
Voltage swing	About VREF		2		V
Common mode range	About VREF	±1			V
Load resistance	To VREF	4			kΩ
Gain			80		dB
Unity gain bandwidth			1		MHz
CMRR	f<20 kHz		60		dB
PSRR	f<20 kHz		60		dB

A2, CURRENT SENSE AMPLIFIER

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input impedance	SE1 to SE2	7.0	10		kΩ
Input offset voltage	SE1 = SE2 = VREF			2	mV
Output voltage swing		VREF-4		VCC-1.2	V
Common mode range		0		VCC-0.2	V
Load Resistance	To VREF	4			kΩ
Output impedance	f<40 kHz			20	Ω
Gain (SOUT-VREF)/(SE1-SE2)	VSE2 = VREF	1.95	2	2.05	V/V
Unity gain bandwidth			1		MHz
CMRR	f<20 kHz		52		dB
PSRR	f<20 kHz		60		dB

POWER SUPPLY MONITOR

1.3V pin voltage	1.3V pin open	1.18	1.25	1.31	V
PS1 threshold			1.25		V
PS2 threshold			1.25		V
PS1, PS2 Hysteresis			20		mV
PS1, PS2 Input Bias Current	PS1, PS2 = 1.3V		1		µA
PFAIL VOL	Linear mode IOC = 1mA			0.4	V
BRK VOL	Linear mode IOC = 1mA			0.4	V
PFAIL IOH	Retract mode VOH = 12V			10	µA
BRK IOH	Retract mode VOH = 12V			10	µA
DISABLE IIL	VIL = 0.8V		2	20	µA
$\overline{\text{RETRACT}}$ IIL	VIL = 0.8V		2	10	µA
DISABLE IIH	VIH = 2.4		1	10	µA
$\overline{\text{RETRACT}}$ IIH	VIH = 2.4		1	10	µA
DISABLE and $\overline{\text{RETRACT}}$ Threshold Voltage			1.4		V

BIPOLAR DRIVERS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SE3 Input Impedance	To VREF	10	25		kΩ
A Comp, C Comp Voltage Swing	w/ External Trans.	VCC - 1.4		VCC - .7	V
B comp, D Comp Voltage Swing	w/ External Trans.	0.7		1.4	V
Output Impedance A, B, C, D Comp	Output Off, No External Trans.		75		kΩ
Transconductance I (A, B, C, D Comp)/(ERR-VREF)			6		mA/V
Gain -(SE1-VREF)/(ERR-VREF) or (SE3-VREF)/(ERR-VREF)	Includes External Trans.	8	8.5	9	V/V
Offset Current (A2 Vos)	Rs = 0.5Ω Rf = Rin Vin = Vref		3.5		mA
Retract Motor Voltage (SE1-SE3)		0.7	1.3	1.7	V
Out B, Out D Source Current	Vout = 0.8V	20			mA
Out B, Out D Current Limit	Vcc = 10.8V, Out B, D = 0.8V Vcc = 12.0V, Out B, D = 0.8V	20 23	25 27	30 33	mA mA
Out A, Out C Sink Current	Vout = 11.2V	20			mA
B and D Output NPN Output Transistor Beta	Ic = 20mA Vce = 10V		20		V/V
A and C Output PNP Output Transistor Beta	Ic = 20mA Vce = 10V		10		V/V

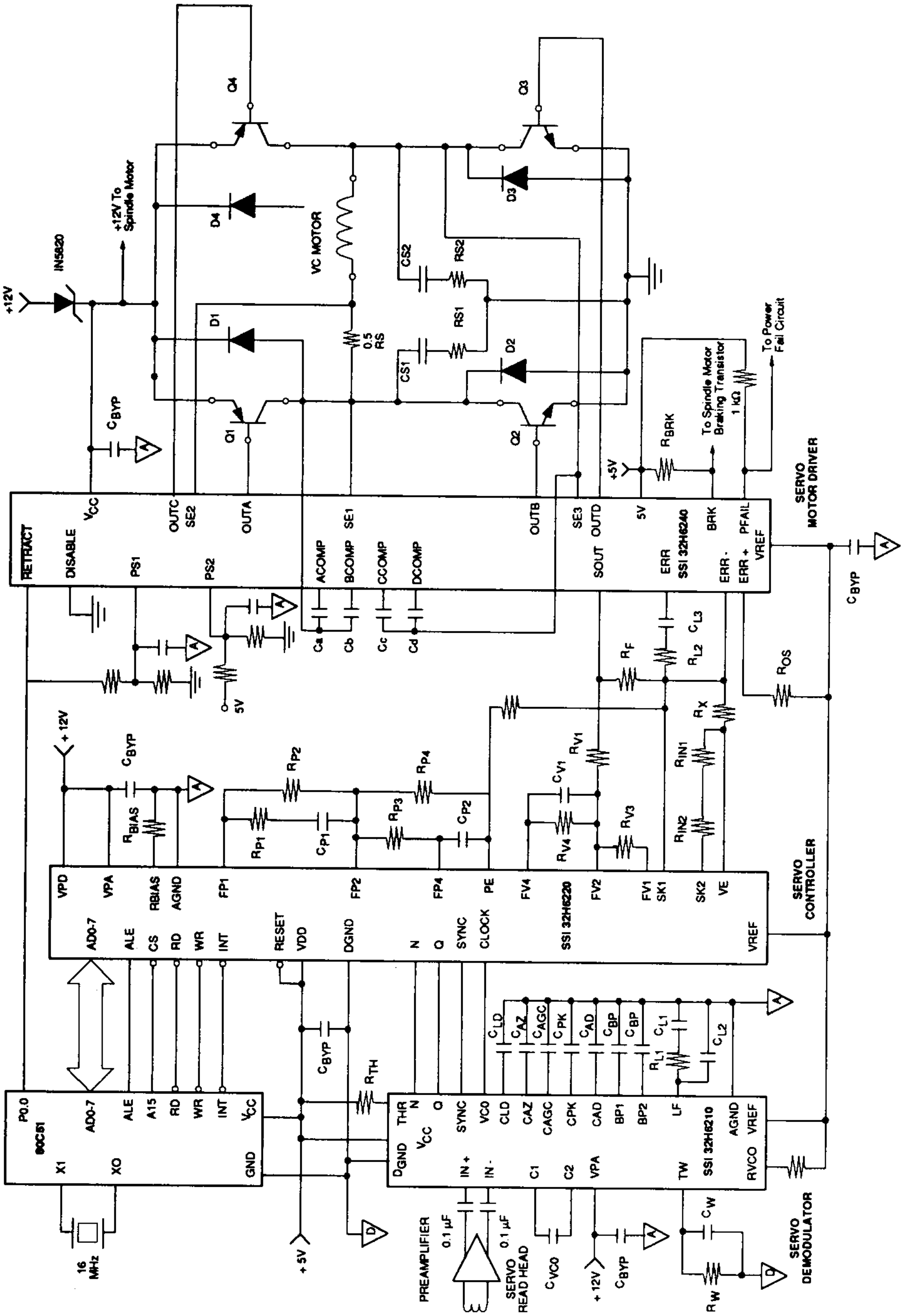
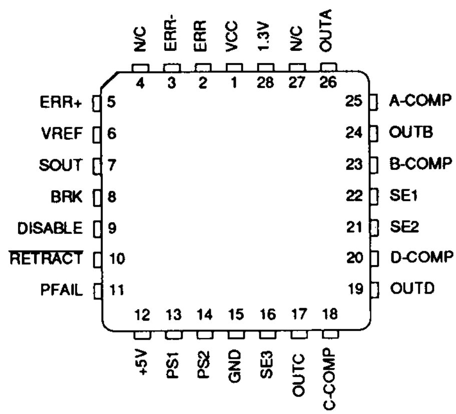


FIGURE 3: Complete Example of Servo Path Electronics using the SSI 32H6210/6220/6240 Chip Set

SSI 32H6240
Servo Motor Driver

PACKAGE PIN DESIGNATIONS
(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin PLCC

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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