

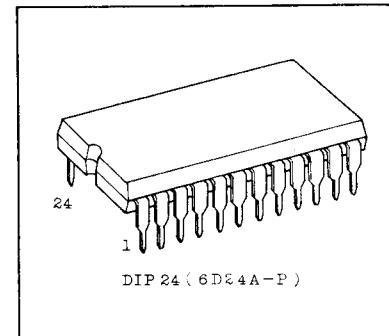
**TC5053P 4-DIGIT UP/DOWN DECADE COUNTER
TC5054P 4-DIGIT UP/DOWN DECADE COUNTER**

TC5053P/TC5054P is a 4-digit decimal up/down counter containing 7-segment decoder/driver.

The counter consists internally of a 4-digit latch, multiplexer, scan oscillating circuit, and decoder/ driver capable of directly driving LED.

The clock input is independently equipped with an up-clock and a down-clock. Each input has the function of a Schmitt trigger.

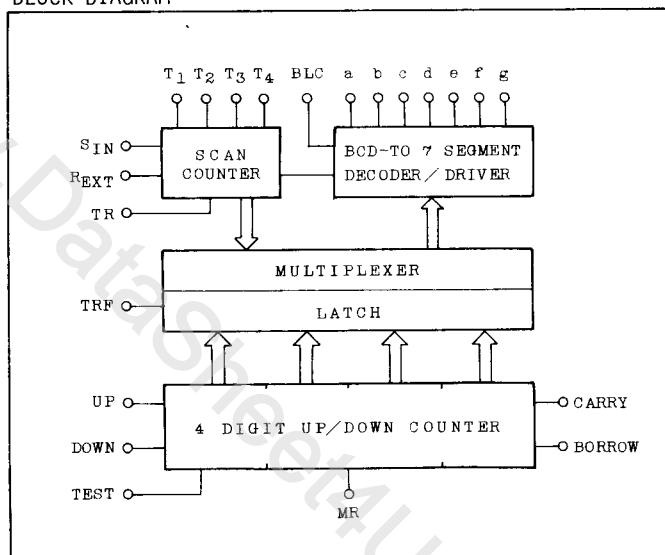
This type of up/down counter can be widely applied to counters, panelmeters, etc.



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V _{DD}	V _{SS} -0.5~V _{SS} +10	V
Input Voltage	V _{IN}	V _{SS} -0.5~V _{DD} +0.5	V
Output Voltage	V _{OUT}	V _{SS} -0.5~V _{DD} +0.5	V
DC Input Current	I _{IN}	±10	mA
Power Dissipation	P _D	300	mW
Storage Temperature Range	T _{STG}	-55~125	°C
Lead Temp./Time	T _{SOL}	260°C • 10sec	

BLOCK DIAGRAM



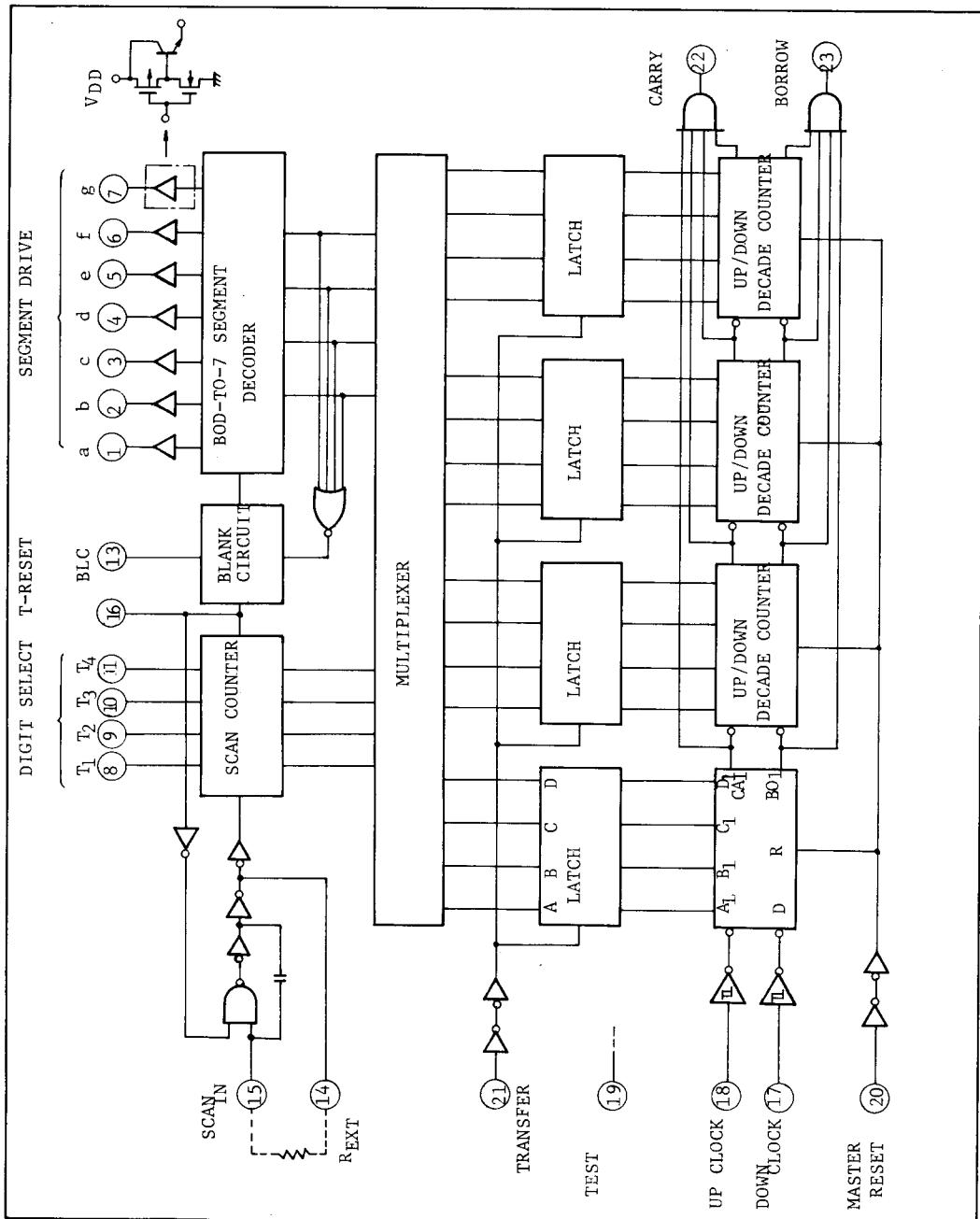
PIN ASSIGNMENT

(TOP VIEW)	
a	1
b	2
c	3
d	4
e	5
f	6
g	7
T ₁	8
T ₂	9
T ₃	10
T ₄	11
V _{SS}	12
	13
	14
	15
	16
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	24

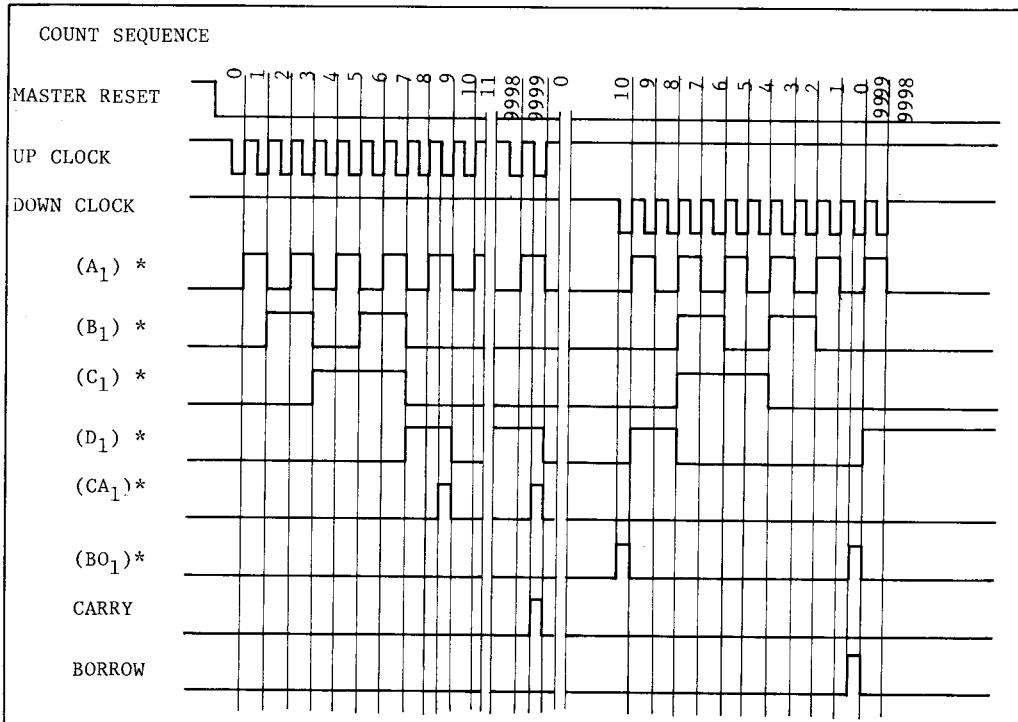
SEGMENT OUTPUTS MODE

TC5053P				
0	1	2	3	4
5	6	7	8	9
TC5054P				
0	1	2	3	4
5	6	7	8	9

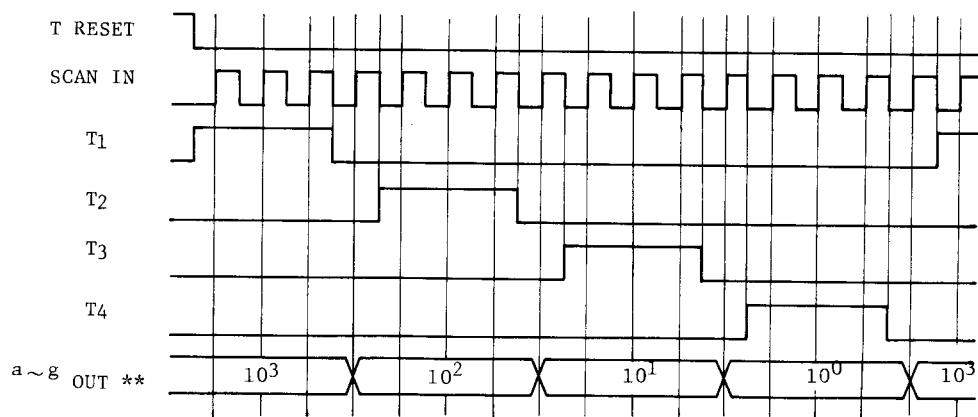
BLOCK DIAGRAM



TIMING CHART



SCAN SEQUENCE



** Required pull down Register

TC5053P, TC5054P

DESCRIPTION OF PIN FUNCTION

PIN NO.	SYMBOL	NAME	FUNCTION						
1	a	SEGMENT a	The segments a ~ g are the outputs that have converted the decimal up/down counter BCD outputs into 7-segment display element driving codes.						
2	b	" b							
3	c	" c							
4	d	" d	These segment signals are synchronous with SCAN inputs and are dynamically output from the higher order digit. Since they are designed so that I_{OH} is large, they can directly drive a cathod common type LED.						
5	e	" e							
6	f	" f							
7	g	" g							
8	T ₁	DIGIT SELECT 1	These are the outputs indicating the digits of the outputs a ~ g and correspond to the higher-order positions from T ₁ upward.						
9	T ₂	" 2							
10	T ₃	" 3	These outputs are automatically switched in order of T ₁ - T ₂ - T ₃ - T ₄ - T ₁ by giving clock to SCAN input.						
11	T ₄	" 4							
12	V _{SS}	V _{SS}	(GND)						
13	BLC	BLANKING CONTROL	<table border="1"> <tr> <td>"H"</td> <td>No 0 suppression</td> <td>The leading 0 suppression of the digits of more than the higher-order(N-1) can be made by connecting this terminal to T_n.</td> </tr> <tr> <td>"L"</td> <td>Leading zero suppression of All digits</td> <td></td> </tr> </table>	"H"	No 0 suppression	The leading 0 suppression of the digits of more than the higher-order(N-1) can be made by connecting this terminal to T _n .	"L"	Leading zero suppression of All digits	
"H"	No 0 suppression	The leading 0 suppression of the digits of more than the higher-order(N-1) can be made by connecting this terminal to T _n .							
"L"	Leading zero suppression of All digits								
14	R _{EXT}	REGISTER EXTERNAL	SCAN clock is produced by connecting a resistor between R _{EXT} and S _{IN} . In case S _{IN} is externally provided, R _{EXT} should be opened.						
15	S _{IN}	SCAN IN	This is a clock input of digit selection counter. If a resistor is connected between S _{IN} and R _{EXT} , SCAN Counter can make self-oscillation.(Pulse may be externally applied)						
16	TR	T-COUNTER RESET	Operation of SCAN counter can be stopped by "H" level. Whenever TR is fallen, SCAN counter starts scanning from T ₁ .						
17	DOWN	DOWN COUNT	The internal counter makes document at the rising edge of a pulse if the pulse is provided to the in a state where UP input is kept at "H" level.						
18	UP	UP COUNT	The internal counter makes up count at the rising edge of a pulse if the pulse is provided to the in a state where DOWN input is kept at "H" level.						
19	TEST	TEST	This set to "L" level. (When it is set to "H" level, counting varies with the rising or falling edge.)						
20	MR	MASTER RESET	A state of count is cleared to "0000" at the 'H' level.						
21	TRF	TRANSFER	In case of "H" level input, the counter contents are always being output through a multiplexer. In case of "L" level input, however, the counter contents before the change to "L" level are not changed by the change in counter contents because the previous contents remain kept in the latch circuit.						
22	CARRY	CARRY	In UP COUNT, when the COUNTER contents reaches "9999", "H" level is output as long as UP COUNTER input holds "L" level.						
23	BORROW	BORROW	In DOWN COUNT, when the COUNTER contents reaches "0000", "H" level is output as long as DOWN COUNTER input holds "L" level.						
24	V _{DD}	V _{DD}	(V _{DD})						

RECOMMENDED OPERATING CONDITION ($V_{SS}=0V$)

ITEM	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	8	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-30	-	85	°C
REXT EXTERNAL RESISTANCE	REXT		5K	-	1M	Ω

ELECTRICAL CHARACTERISTICS ($V_{SS}=0V$)

ITEM	SYMBOL	TEST CONDITION	V_{DD} (V)	-30°C		25°C		85°C		UNIT	
				MIN	MAX	MIN	TYP	MAX	MIN		
High Level Output Voltage	T1~T4,Carry,Borrow	$ I_{OUT} <1\mu A$ $V_{IN}=V_{SS}, V_{DD}$	5	4.95	-	4.95	-	-	4.95	-	
	a ~ g			4.0	-	4.0	4.5	-	4.0	-	
	REXT			4.95	-	4.95	-	-	4.95	-	
Low Level Output Voltage	T1~T4,Carry,Borrow	$ I_{OUT} <1\mu A$ $V_{IN}=V_{SS}, V_{DD}$	5	-	Q05	-	-	0.05	-	Q05	
	REXT			-	Q05	-	-	0.05	-	Q05	
High Level Output Current	T1~T4,Carry,Borrow	I_{OH} $V_{OH}=4.6V$ $V_{OH}=3.5V$ $V_{OH}=4.6V$	5	-0.2	-	-0.16	-	-	0.12	-	
	a ~ g			-20	-	-20	-	-	-15	-	
	REXT			-0.02	-	-0.02	-	-	0.01	-	
Low Level Output Current	T1~T4,Carry,Borrow	I_{OL} $V_{OL}=0.4V$	5	0.52	-	0.44	-	-	0.36	-	
	REXT			0.02	-	0.02	-	-	0.01	-	
Disable Current (a~g)	I_{DL}	$V_{OL}=0V$	8	-	-3.0	-	-10 ⁴	-	-	-3.0	μA
High Level Input Voltage	UP/DOWN CLOCK	V_{IH}	5	3.5	-	3.5	-	-	3.5	-	V
	OTHER			3.5	-	3.5	2.75	-	3.5	-	
Low Level Input Voltage	UP/DOWN CLOCK	V_{IL}	5	-	1.5	-	-	1.5	-	1.5	V
	OTHER			-	1.5	-	2.25	1.5	-	1.5	
High Level Input Current	I_{IH}	$V_{IH}=8V$	8	-	Q15	-	10 ⁵	Q15	-	1.0	μA
Low Level Input Current	I_{IL}	$V_{IL}=0V$	8	-	Q15	-	-10 ⁵	Q15	-	1.0	μA
Quiescent Current Consumption	I_{DD}	$V_{IN}=V_{SS}, V_{DD}$ OUTPUT OPEN	8	-	-	-	-	-	-	-	μA

SWITCHING CHARACTERISTICS ($T_a=25^\circ C$, $V_{SS}=0V$, $C_L=50pF$)

CHARACTERISTIC	SYMBOL	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_{TLH}	T1~T4, Carry, Borrow			-	70	180	ns
		a~g ($R_L=1k\Omega$)			-	40	100	
Output Fall Time	t_{THL}	T1~T4, Carry, Borrow			-	50	130	
Propagation Delay Time	t_{pLH}	CLOCK-a~g ($R_L=1k\Omega$, $T_1=H$)			-	5000	12000	ns
		CLOCK-Carry, Borrow			-	700	1500	
	t_{pHL}	SCAN-T1~T4			-	450	1000	
		SCAN-a~g ($R_L=1k\Omega$)			-	750	1700	
Max. Frequency	f_{CL-1^*}	CLOCK			2.0	4.0	-	MHz
	f_{CL-2^*}				0.7	1.4	-	
	$f_{CL-1^{**}}$	SCAN			2.0	4.0	-	
	$f_{CL-2^{**}}$				0.7	1.1	-	

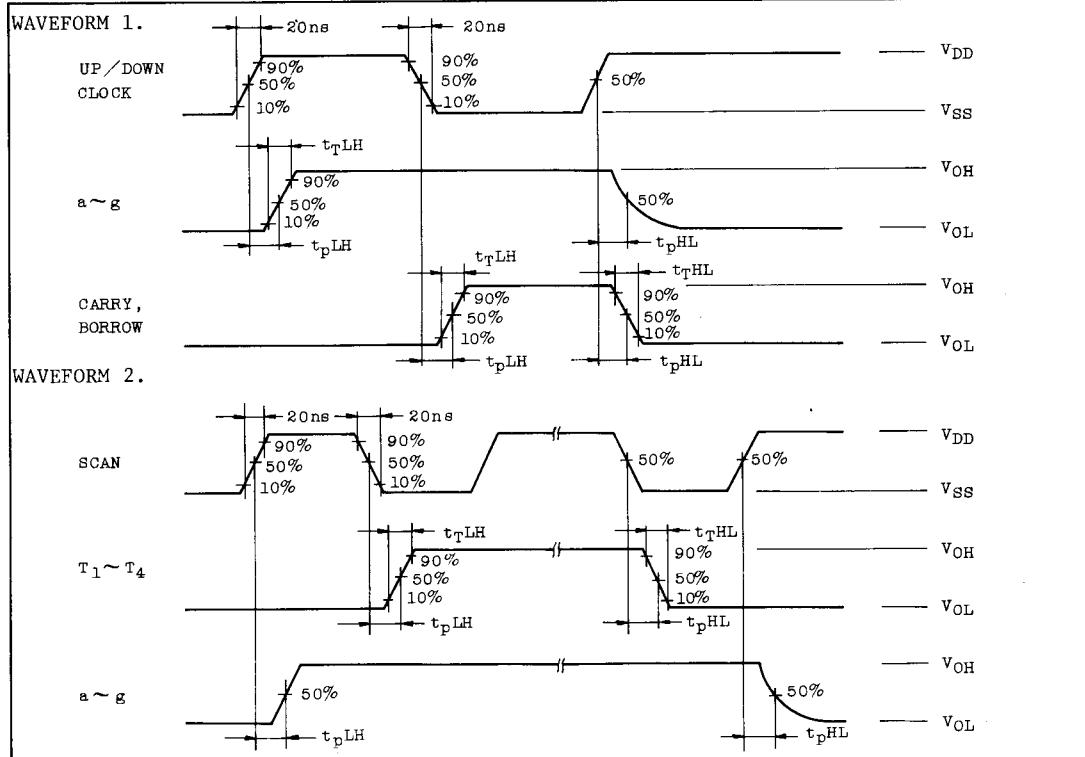
SWITCHING CHARACTERISTICS ($T_a=25^\circ C$, $V_{SS}=0V$, $C_L=50pF$) (Continued)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Min. Pulse Width	$t_w(MR)$	MASTER RESET	-	150	450	ns
	$t_w(TR)$	T-COUNTER RESET	-	100	300	
	$t_w(TRF)$	TRANSFER	-	50	200	
Minimum Removal Time	t_{rem}	MR-CLOCK	-	-100	250	ns
		TR-SCAN	-	250	750	
		TRF-CLOCK	-	100	400	
Max. Clock Rise Time Max. Clock Fall Time	t_{rCL} t_{fCL}	UP/DOWN CLOCK	No Limit			μs
Input Capacitance	C_{IN}	except SCAN	-	5	7.5	pF

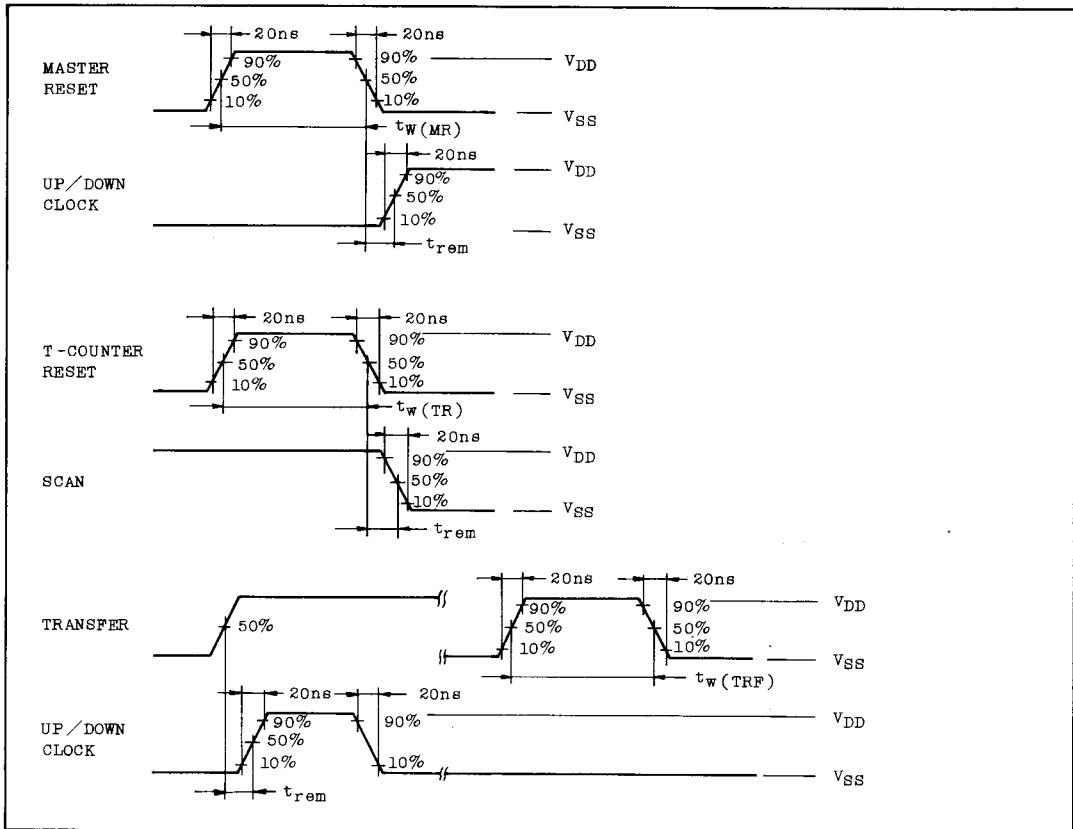
* Counter operation : f_{CL-1} , CARRY, BORROW operation : f_{CL-2}

** Leading zero suppression : f_{CL-2} , No zero suppression : f_{CL-1}

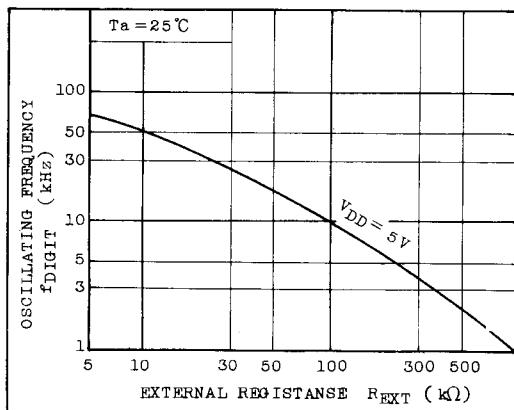
SWITCHING TIME TEST WAVEFORMS



SWITCHING TIME TEST WAVEFORMS (Continued)



$f_{DIGIT} = R_{EXT} \text{ (TYP.)}$



$I_{DDopr} = f_{IN} \text{ (TYP.)}$

